



Integrated Device Technology, Inc.

# FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273T/AT/CT

## FEATURES:

- Std., A, and C speed grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH} = 3.3\text{V}$  (typ.)
  - $V_{OL} = 0.3\text{V}$  (typ.)
- High drive outputs (-15mA IOH, 48mA IOL)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

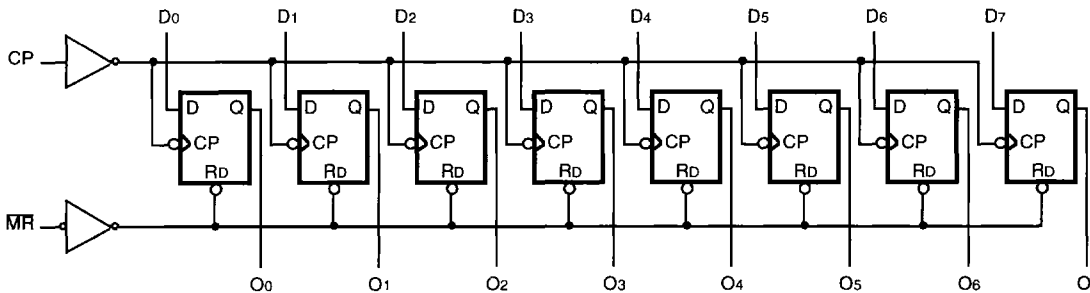
## DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

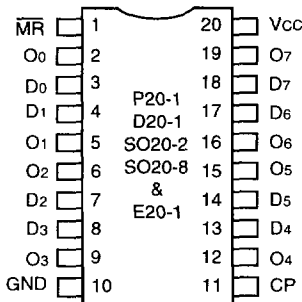
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

## FUNCTIONAL BLOCK DIAGRAM



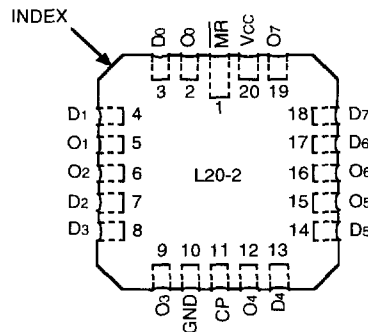
2568 drw 03

## PIN CONFIGURATIONS



2568 drw 01

DIP/SOIC/QSOP/CERPACK  
TOP VIEW



2568 drw 02

LCC  
TOP VIEW

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1996

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**PIN DESCRIPTION**

Pin Names	Description
DN	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
ON	Data Outputs

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**FUNCTION TABLE<sup>(1)</sup>**

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	DN	ON
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

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**NOTE:**

- 1. H = HIGH voltage level steady state
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
- L = LOW voltage level steady state
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
- X = Don't Care
- ↑ = LOW-to-HIGH Clock Transition

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	-0.5 to V <sub>CC</sub> +0.5	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	-60 to +120	-60 to +120	mA

2568 l-k 03

**NOTES:**

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating *only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.* Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- 2. Input and V<sub>CC</sub> terminals only.
- 3. Outputs and I/O terminals only.

**CAPACITANCE (TA = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
COU	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

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**NOTE:**

- 1. This parameter is measured at characterization but not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ; Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$		-60	-120	-225	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -6\text{mA MIL.}$ $I_{OH} = -8\text{mA COM'L.}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$	2.0	3.0	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 32\text{mA MIL.}$ $I_{OL} = 48\text{mA COM'L.}$	—	0.3	0.5	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND}$ or $V_{CC}$		—	0.01	1	mA

**NOTES:**

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test parameter for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .



**POWER SUPPLY CHARACTERISTICS**

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{MR}$ = V <sub>CC</sub> One Input Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{MR}$ = V <sub>CC</sub> One Bit Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	1.5	3.5	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.5	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{MR}$ = V <sub>CC</sub> Eight Bits Toggling at f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND	—	3.8	7.3 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	6.0	16.3 <sup>(5)</sup>	

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

2568 tbl 06

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

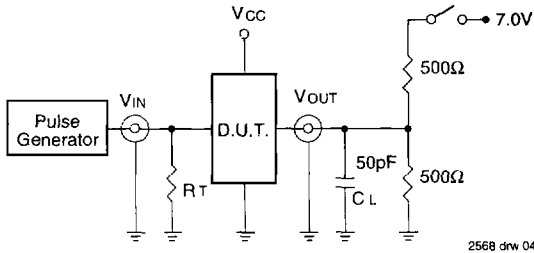
Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT273T				IDT54/74FCT273AT				IDT54/74FCT273CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH	Propagation Delay CP to ON	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
tPHL	Propagation Delay MR to ON		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
tsu	Set-up Time HIGH or LOW DN to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW DN to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tw	MR Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
tREM	Recovery Time MR to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2568 tbi 07

**TEST CIRCUITS AND WAVEFORMS**  
**TEST CIRCUITS FOR ALL OUTPUTS**



2568 drw 04

**SWITCH POSITION**

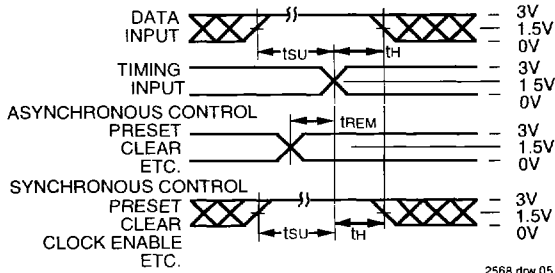
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2568 Ink 08

**DEFINITIONS:**

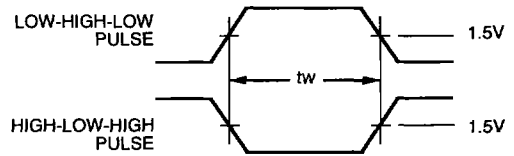
$C_L$  = Load capacitance: includes jig and probe capacitance.  
 $R_T$  = Termination resistance: should be equal to Zour of the Pulse Generator.

**SET-UP, HOLD AND RELEASE TIMES**



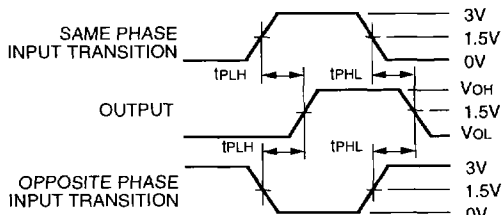
2568 drw 05

**PULSE WIDTH**



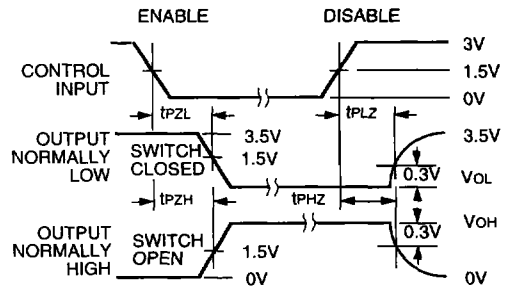
2568 drw 06

**PROPAGATION DELAY**



2568 drw 07

**ENABLE AND DISABLE TIMES**

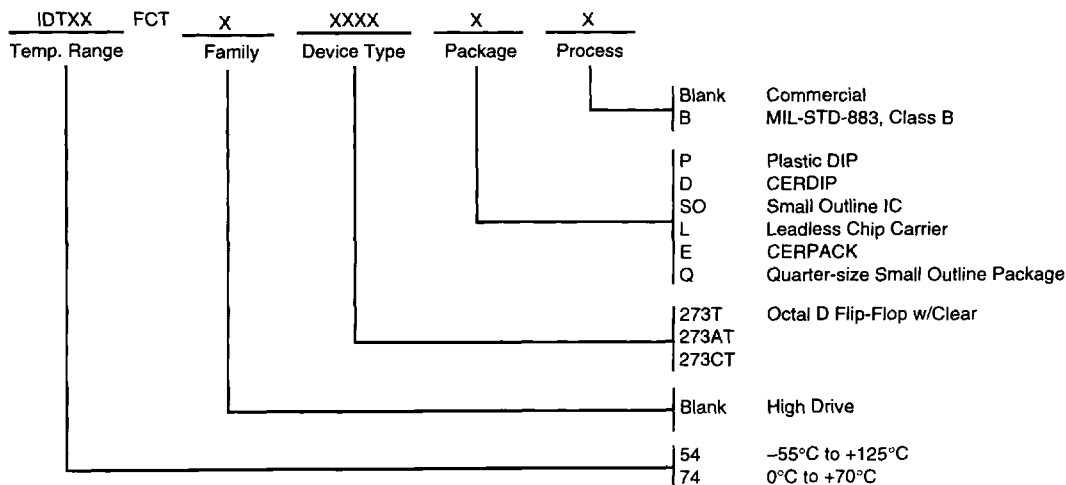


2568 drw 08

**NOTES:**

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $t_r \leq$  2.5ns;  $t_f \leq$  2.5ns

**ORDERING INFORMATION**



2568 drw 09

