TC74LVQ245F/FW/FS

Octal Bus Transceiver

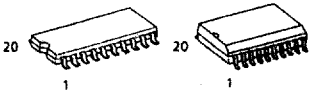
The TC74LVQ245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

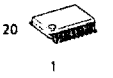
The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



F (SOP20-P-300)
Weight : 0.22g (TYP.)

FW (SOL20-P-300)
Weitht : 0.46g (TYP.)



FS (SSOP20-P-225A)
Weight : 0.09g (TYP.)

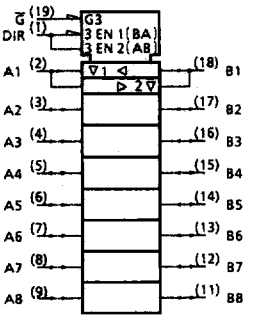
Features

- High Speed: t_{pd} = 5.8ns (Typ.) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max.) at Ta = 25°C
- Input Voltage Level:
  - V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  - V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 12mA (Min.)
- Balanced Propagation Delays: $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74HC245

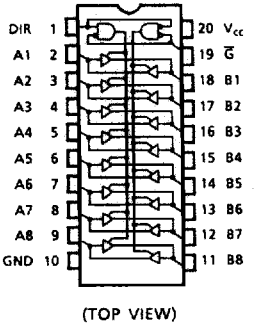
Application Notes

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.



IEC Logic Symbol



(TOP VIEW)

Pin Assignment

Truth Table

Inputs		Outputs	Function	
$\overline{G}$	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High Impedance	

X: Don't Care
Z: High Impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Bus I/O Voltage	$V_{I/O}$	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 ~ 3.6	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0 ~ V_{CC}	V
Bus I/O Voltage	$V_{I/O}$	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 100	ns/V

DC Electrical Characteristics

Parameter	Symbol	Test Condition			Ta = 25°C			Ta = -40 ~ 85°C		Unit
				V_{CC} (V)	Min	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}			3.0	2.0	–	–	2.0	–	V
Low-Level Input Voltage	V_{IL}			3.0	–	–	0.8	–	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	3.0	2.9	3.0	–	2.9	–	V
			I_{OH} = -12mA	3.0	2.58	–	–	2.48	–	V
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	–	0.0	0.1	–	0.1	V
			I_{OL} = 12mA	3.0	–	–	0.36	–	0.44	V
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND		3.6	–	–	±0.5		±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	–	–	4.0	–	40.0	μA

AC Electrical Characteristics (Input $t_r = t_f$ = 3ns, C_L = 50pF, R_L = 500Ω)

Parameter	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Min	Typ.	Max.	Ta = -40 ~ 85°C Min.	Max.	Unit
Propagation Delay Time	t_{pLH}		2.7	–	8.0	14.1	1.0	17.0	ns
	t_{pHL}		3.3±0.3	–	6.7	10.0	1.0	11.5	ns
Output Enable Time	t_{pZL}		2.7	–	10.7	18.3	1.0	20.0	ns
	t_{pZH}		3.3±0.3	–	8.9	13.0	1.0	14.0	ns
Output Disable Time	t_{pLZ}		2.7	–	7.9	20.4	1.0	22.0	ns
	t_{pHZ}		3.3±0.3	–	6.6	14.5	1.0	15.0	ns
Output to Output Skew	t_{osLH}	(Note 1)	2.7	–	–	1.5	–	1.5	ns
	t_{osHL}	(Note 1)	3.3±0.3	–	–	1.5	–	1.5	ns
Input Capacitance	C_{IN}	DIR, $\overline{G}$ (Note 2)		–	5	10	–	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		–	13	–	–	–	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		–	38	–	–	–	pF

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption. Average operating current can be obtained by the equation:

I_{CC} (opr) = C_{PD} • V_{CC} • f_{IN} + I_{CC}/8 (per bit)

Noise Characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC}	Typ.	Max.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.6	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.6	-1.0	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	–	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	–	0.8	V

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