Signetics

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Status	Product Specification
FAST Products	

FAST 74F175
Flip-Flop

Quad D Flip-Flop

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175	140MHz	25mA

FEATURES

- **Four edge-triggered D-type flip-flops**
- **Buffered common clock**
- **Buffered asynchronous Master Reset**
- **True and complementary outputs**
- **Industrial temperature range available (-40°C to +85°C)**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
16-Pin Plastic DIP	N74F175N	I74F175N
16-Pin Plastic SO	N74F175D	I74F175D

DESCRIPTION

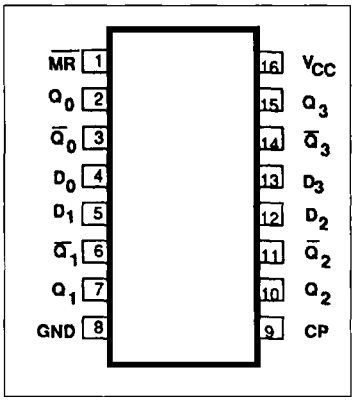
The 74F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously. The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. All Q outputs will be forced Low independently of clock or data inputs by Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required and the CP and $\overline{MR}$ are common to all storage elements.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

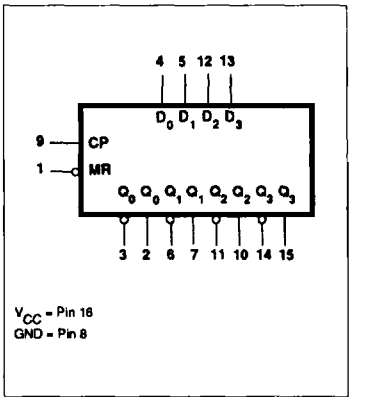
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

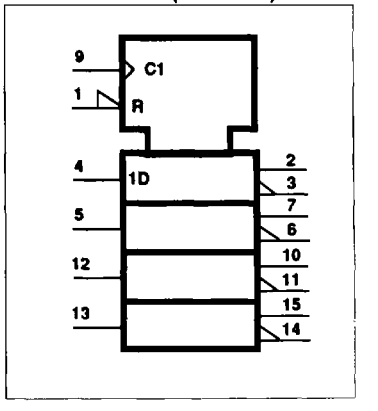
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	140		100		100		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	4.0 4.0	7.5 9.5	3.5 4.0	8.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	13.0	4.5	13.0	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	9.0	4.0	11.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		3.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	4.0 5.0			4.0 5.0		4.0 6.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width Low	Waveform 3	5.0			5.0		5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		6.0		ns