54F/74F13

Dual 4-Input NAND Schmitt Trigger

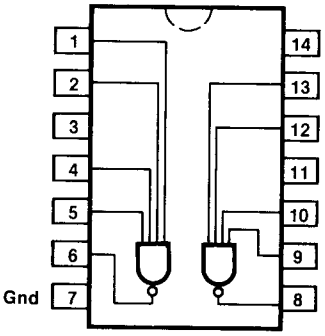
Description

The 'F13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional NAND gates.

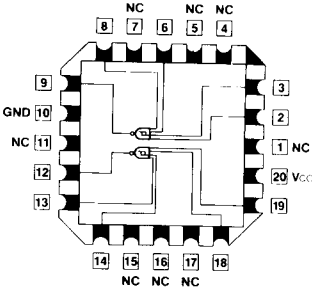
Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800 mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

Ordering Code: See Section 5

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A,B,C,D	Inputs	0.5/0.375
O	Outputs	25/12.5

Function Table

Inputs				Outputs
A	B	C	D	O
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions	
		Min	Typ	Max			
I_{CCH}	Power Supply Current		4.5	8.5	mA	Outputs HIGH	V_{CC} = Max
I_{CCL}			7.0	10.0		Outputs LOW	

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay		7.0 13.5						ns	3-1 3-3