National Semiconductor

MICROCIRCUIT DATA SHEET

MNNS41256L35-X REV 0A0

Original Creation Date: 11/28/95
Last Update Date: 02/05/97
Last Major Revision Date: 11/28/95

256K Static RAM (32K x 8 bit)

General Description

NS41256L35 is a high performance, low power version CMOS static RAM organized as 32,768 X 8 bits with 35nS address to access time. The NS41256 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible.

Industry Part Number

NS41256L35

NS Part Numbers

NS41256L35E/883
NS41256L35J/883

Prime Die

PDM41256V

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

Truth Table:

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	HI-Z	STANDBY
L	H	L	DOUT	READ
X	L	L	DIN	WRITE
H	H	L	HI-Z	OUTPUT DISABLE

Note: H=Vih, L=Vil, X=Dont care

Applications

Graphic Notes: * = This note does not apply for this device.

*1. The parameter is tested with CL = 5pF as shown in Fig. 2. Transition is measured ±200mV from steady state voltage.

*2. At any given temperature and voltage condition, tHZCE is less than tLZCE.

*3. This parameter is sampled.

*4. $\overline{WE}$ is high for a READ cycle.

5. The device is continously selected. All the Chip Enables are held in their active state. Applies to READ cycle 1.

6. The address is valid prior to or coincident with the latest occuring Chip Enable. Applies to READ cycle 2.

*7. Vcc = 5V ±10%.

(Absolute Maximum Ratings)

(Note 1)

Terminal Voltage with Respect to GND (VTERM)	-0.5V to +7.0V
Temperature Under Bias (TBIAS)	-65 C to +135 C
Storage Temperature (TSTG)	-65 C to +150 C
Power Dissipation (PT)	1.0W
DC Output Current (IOUT)	50mA

Note 1: Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

DC Supply Voltage (VCC)	4.5V to 5.5V
DC Supply Voltage (GND)	0V
Operating Temperature Range Ambient	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc=5.0V ±10%, TA=-55 C to +125 C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
ILI	Input Leakage Current	Vcc=Max., Vin=Gnd to Vcc			-5	5	uA	1, 2, 3
ILO	Output Leakage Current	Vcc=Max., $\overline{CE}$=Vih, Vout=Gnd to Vcc			-5	5	uA	1, 2, 3
Vih	Input High Voltage				2.2	6.0	V	1, 2, 3
Vil	Input Low Voltage		6		-0.5	0.8	V	1, 2, 3
Vol	Output Low Voltage	Iol=8mA, Vcc=Min.				0.4	V	1, 2, 3
		Iol=10mA, Vcc=Min.				0.5	V	1, 2, 3
Voh	Output High Voltage	Ioh=-4mA, Vcc=Min.			2.4		V	1, 2, 3

DC PARAMETERS: Power Supply Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc=5V ±10%

Icc	Operating Current	$\overline{CE}$=Vil, f=fmax=1/trc, Vcc=Max., Iout=0mA				130	mA	1, 2, 3
ISB	Standby Current	$\overline{CE}$=Vih, f=fmax=1/trc, Vcc=Max.				30	mA	1, 2, 3
ISB1	Full Standby Current	$\overline{CE}$≥Vcc-0.2V, f=0, Vcc=Max., Vin≥Vcc-0.2V or ≤0.2V				10	mA	1, 2, 3

Electrical Characteristics

AC PARAMETERS: ELECTRICAL CHARACTERISTICS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V ±10%, TA=-55 C to +125 C, Input pulse levels=Gnd to 3.0V, Input rise and fall times=5nS, Input timing reference levels=1.5V, Output reference levels=1.5V, Output load for 12-35nS speed grades=See fig. 1 & 2.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tRC	Read Cycle Time				35		nS	9, 10, 11
tAA	Address Access Time					35	nS	9, 10, 11
tACE	Chip Enable Access Time					35	nS	9, 10, 11
tOH	Output Hold from Address Change				3		nS	9, 10, 11
tLZCE	Chip Enable to Output in Low Z		3, 4, 5		5		nS	9, 10, 11
tHZCE	Chip Disable to Output in High Z		3, 4, 5			10	nS	9, 10, 11
tPU	Chip Enable to Power Up Time		4		0		nS	9, 10, 11
tPD	Chip Disable to Power Down Time		4			35	nS	9, 10, 11
tAOE	Output Enable Access Time					15	nS	9, 10, 11
tLZOE	Output Enable to Output in Low Z		4, 5		0		nS	9, 10, 11
tHZOE	Output Disable to Output in High Z		4, 5			10	nS	9, 10, 11
tWC	Write Cycle Time				35		nS	9, 10, 11
tCW	Chip Enable to end of Write				20		nS	9, 10, 11
tAW	Address Valid to end of Write				20		nS	9, 10, 11
tAS	Address Setup Time				0		nS	9, 10, 11
tAH	Address Hold from end of Write				0		nS	9, 10, 11
tWP	Write Pulse Width				20		nS	9, 10, 11
tDS	Data Setup Time				12		nS	9, 10, 11
tDH	Data Hold Time				0		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS: ELECTRICAL CHARACTERISTICS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc=5V ±10%, TA=-55 C to +125 C, Input pulse levels=Gnd to 3.0V, Input rise and fall times=5nS, Input timing reference levels=1.5V, Output reference levels=1.5V, Output load for 12-35nS speed grades=See fig. 1 & 2.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tLZWE	Write Disable to Output in Low Z		4, 5		0		nS	9, 10, 11
tHZWE	Write Enable to Output in High Z		4, 5			8	nS	9, 10, 11

AC PARAMETERS: Capacitance

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: TA=+25 C, f=1.0Mhz

Cin	Input Capacitance		7			8	pF	9, 10, 11
Cout	Output Capacitance		7			8	pF	9, 10, 11

Data Retention Electrical Characteristics: DC

Vdr	Vcc for Retention Data				2		V	1, 2, 3
Iccdr	Data Retention Current (15-35nS)	$\overline{CE}$≥Vcc-0.2V, Vin≥Vcc-0.2V or ≤0.2V, Vcc=2V				500	uA	1, 2, 3
Iccdr	Data Retention Current	$\overline{CE}$≥Vcc-0.2V, Vin≥Vcc-0.2V or ≤0.2V, Vcc=3V				750	uA	1, 2, 3

Data Retention Electrical Characteristics: AC

tCDR	Chip Deselect to Data Retention Time				0		nS	9, 10, 11
tR	Operation Recovery Time		4		tRC		nS	9, 10, 11

Note 1: The device is continously selected. All the Chip Enables are held in their active state.
Note 2: The address is valid prior to or coincident with the latest occuring Chip Enable.
Note 3: At any given temperature and voltage condition, tHZCE is less than tLZCE.
Note 4: This parameter is sampled.
Note 5: The parameter is tested with CL=5pF as shown in Figure 2. Transition is measured ±200mV from steady state voltage.
Note 6: Vil(Min)=-3.0V for pulse width less than 20nS.
Note 7: This parameter is determined by device characterization but is not production tested.

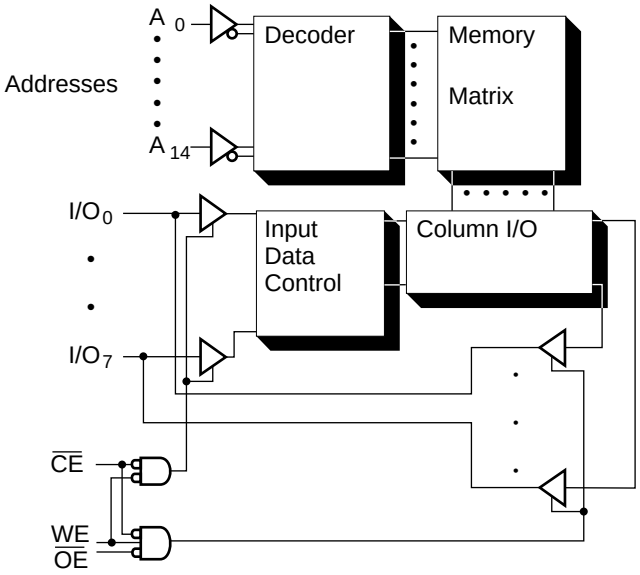
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
AN00012A	BLOCK DIAGRAM - NS41256
AN00016A	FIGURE 1 - OUTPUT LOAD EQUIVALENT
AN00017A	FIGURE 2 - OUTPUT LOAD EQUIVALENT
AN00019A	FIGURE 4 - CAPACITIVE LOADING GRAPH
AN00020A	READ CYCLE 1 (APPLICATION NOTES)
AN00022A	READ CYCLE 2 (APPLICATION NOTES)
AN00025A	WRITE CYCLE 1 - WRITE ENABLE CONTROLLED
AN00027A	WRITE CYCLE 2 - CHIP ENABLE CONTROLLED
AN00029A	LOW VCC DATA RETENTION WAVEFORM
P000141A	CERDIP (J), 28 LEAD, 300 MIL (PIN OUT)
P000142A	CERAMIC LCC (E), 32 LEAD, 450 X 550 MIL (PIN OUT)

See attached graphics following this page.

AN00012A

Functional Block Diagram



NS41256

AN00016A

Output Load Equivalent

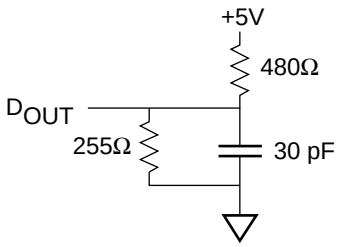


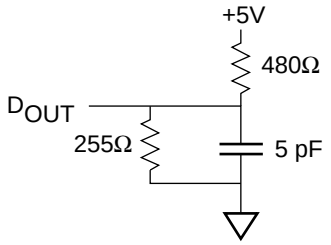
FIG. 1

AN00017A

FIG. 2

Output Load Equivalent

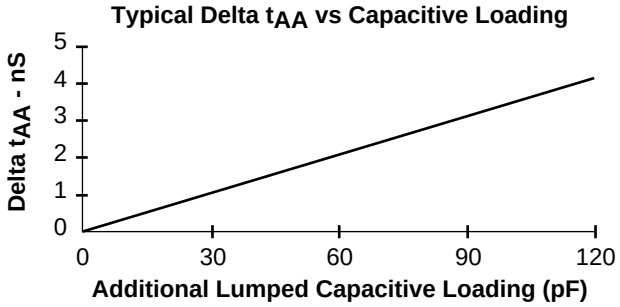
(for tLZCE, tHZWE, tLZWE, tHZWE, tLZOE, tHZOE)



NS41024
NS41096
NS41256
NS4A024
NS4A028
NS4M096
NS4R024

AN00019A

FIG. 4

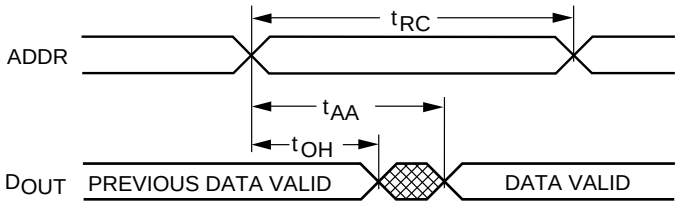


NS41256
NS41257
NS41258
NS4A024
NS4A028

AN00020A

Read Cycle #1

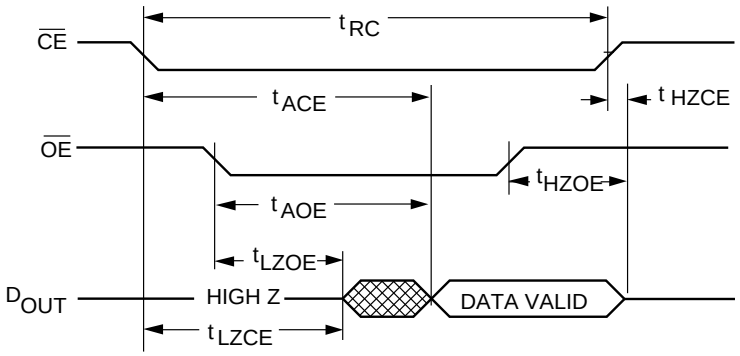
Notes : 4,5,6 apply



NS41024
NS41096
NS41256
NS41257
NS41258
NS4A024
NS4A028
NS4M096
NS4R024

AN00022A

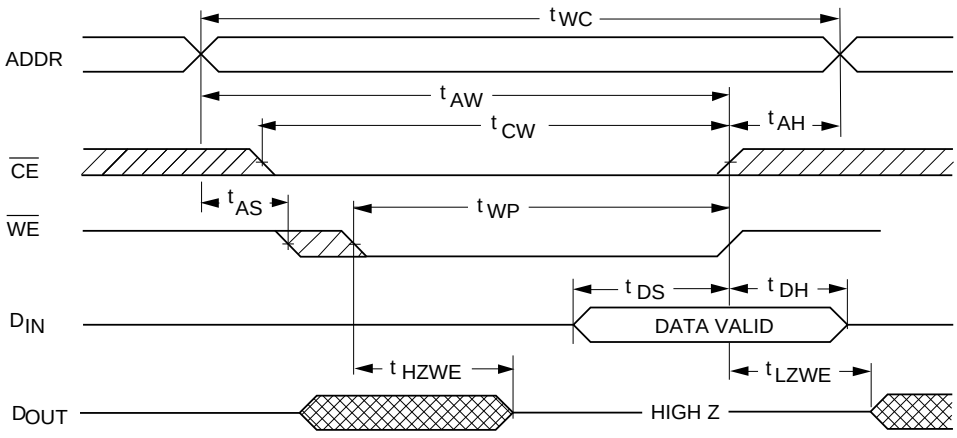
Read Cycle #2 Notes 2,4,6 & 7



NS41096
NS41256
NS4M096

AN00025A

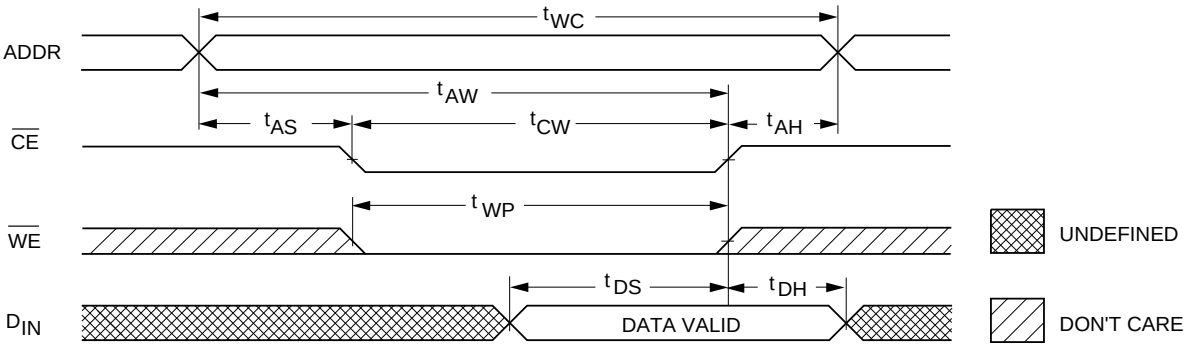
Write Cycle #1 (write enable controlled)



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

AN00027A

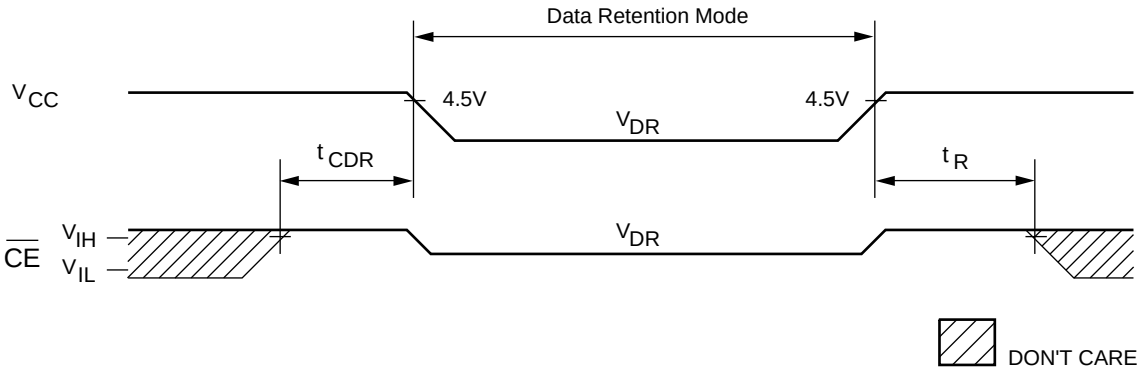
Write Cycle #2 (chip enable controlled)



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

AN00029A

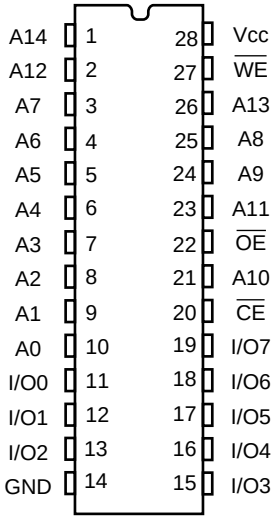
Low Vcc Data Retention Waveform



NS41096
NS41256
NS41257
NS41258
NS4A028
NS4M096

P000141A

Pin Configuration
CERDIP (J Suffix)
28LD (pinout)

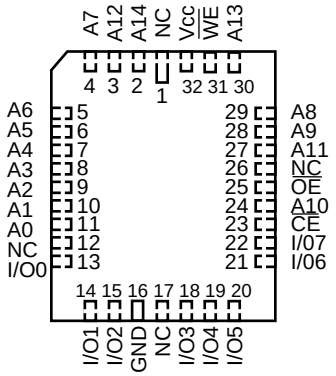


NS41256

P000142A

Pin Configuration

LCC (E Suffix) 32LD (pinout)



NS41256