



Integrated Device Technology, Inc.

HIGH-PERFORMANCE IDT54/74FCT821/2821AT/BT/CT/DT CMOS BUS IDT54/74FCT823/2823AT/BT/CT/DT INTERFACE REGISTERS IDT54/74FCT825/2825AT/BT/CT

FEATURES:

- **Common features:**
 - A, B, C and D speed grades
 - Low input and output leakage $\leq 1\mu\text{A}$ (max.)
 - CMOS power levels
 - True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
 - Meets or exceeds JEDEC standard 18 specifications
 - Product available in Radiation Tolerant and Radiation Enhanced versions
 - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
 - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT821/823/825T:**
 - High drive outputs (-15mA IOH, 48mA IOL)
 - Power off disable outputs permit "live insertion"
- **Features for FCT2821/2823/2825T:**
 - Balanced Output Drivers: $\pm 24\text{mA}$ (commercial), $\pm 16\text{mA}$ (military)
 - Reduced system switching noise

bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT821/2821AT/BT/CT/DT are buffered, 10-bit wide versions of the popular '374 function. The IDT54/74FCT823/2823AT/BT/CT/DT are 9-bit wide buffered registers with Clock Enable (EN) and Clear (CLR) – ideal for parity bus interfacing in high-performance microprogrammed systems. The IDT54/74FCT825/2825AT/BT/CT are 8-bit buffered registers with all the '823 controls plus multiple enables ($\overline{OE}1, \overline{OE}2, \overline{OE}3$) to allow multi-user control of the interface, e.g., \overline{CS} , DMA and RD/ \overline{WR} . They are ideal for use as an output port requiring high IOH/IOL.

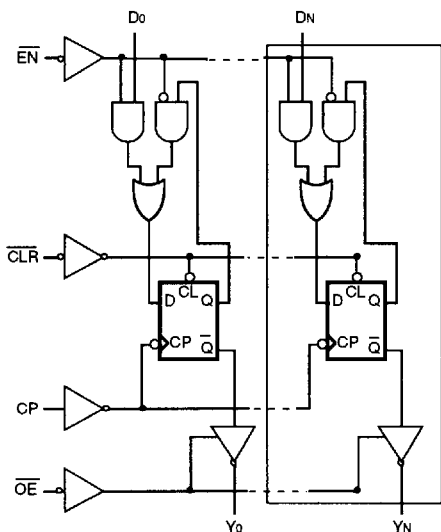
The IDT54/74FCT8xx high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

The IDT54/74FCT2821AT/BT/CT/DT, IDT54/74FCT2823AT/BT/CT/DT, IDT54/74FCT2825AT/BT/CT have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT54/74FCT2xxxT parts are plug-in replacements for IDT54/74FCTxxxT parts.

DESCRIPTION:

The IDT54/74FCT8xx series is built using an advanced dual metal CMOS technology. The IDT54/74FCT820 series

FUNCTIONAL BLOCK DIAGRAM



2567 drw 01

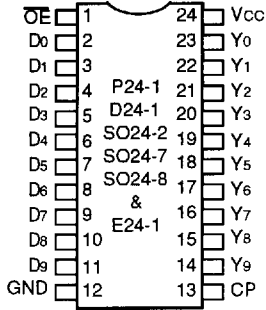
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

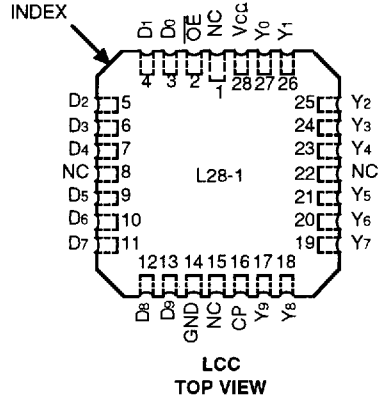
APRIL 1994

PIN CONFIGURATIONS

FCT821/2821T 10-BIT REGISTER



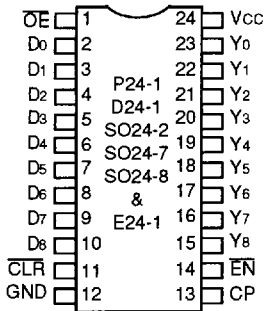
**DIP/SOIC/SSOP/QSOP/CERPACK
 TOP VIEW**



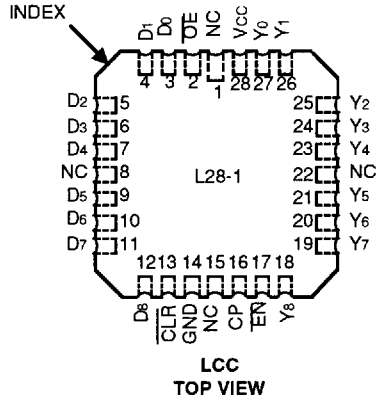
**LCC
 TOP VIEW**

2567 drw 02

FCT823/2823T 9-BIT REGISTER



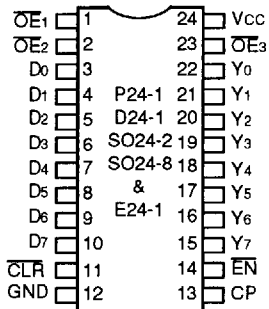
**DIP/SOIC/SSOP/QSOP/CERPACK
 TOP VIEW**



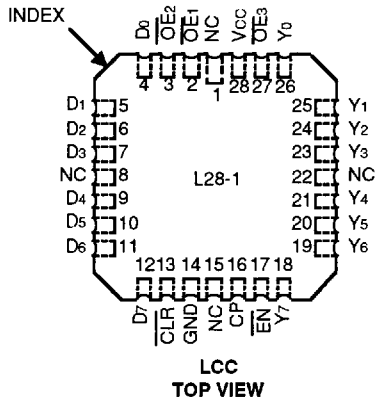
**LCC
 TOP VIEW**

2567 drw 03

FCT825/2825T 8-BIT REGISTER



**DIP/SOIC/SSOP/QSOP/CERPACK
 TOP VIEW**



**LCC
 TOP VIEW**

2567 drw 04

PIN DESCRIPTION

Names	I/O	Description
D _i	I	The D flip-flop data inputs.
CLR	I	When the clear input is LOW and \overline{OE} is LOW, the Q _i outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y _i	O	The register 3-state outputs.
EN	I	Clock Enable. When the clock enable is LOW, data on the D _i input is transferred to the Q _i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q _i outputs do not change state, regardless of the data or clock input transitions.
\overline{OE}	I	Output Control. When the \overline{OE} input is HIGH, the Y _i outputs are in the high-impedance state. When the \overline{OE} input is LOW, the TRUE register data is present at the Y _i outputs.

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FUNCTION TABLE⁽¹⁾

Inputs					Internal/Outputs		Function
\overline{OE}	CLR	EN	D _i	CP	Q _i	Y _i	
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE:

- 1. H = HIGH
- L = LOW
- X = Don't Care
- NC = No Change
- ↑ = LOW-to-HIGH Transition
- Z = High Impedance

2567 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

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NOTES:

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- 2. Input and V_{CC} terminals only.
- 3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- 1. This parameter is measured at characterization but not tested.

2567 lmk 06

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	V _{CC} = Max.	V _I = 2.7V	—	—	±1	μA
I _{IL}	Input LOW Current ⁽⁴⁾		V _I = 0.5V	—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output pins) ⁽⁴⁾	V _{CC} = Max.	V _O = 2.7V	—	—	±1	μA
I _{OZL}			V _O = 0.5V	—	—	±1	
I _I	Input HIGH Current ⁽⁴⁾	V _{CC} = Max., V _I = V _{CC} (Max.)		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾		-60	-120	-225	mA
V _H	Input Hysteresis	—		—	200	—	mV
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC}		—	0.01	1	mA

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OUTPUT DRIVE CHARACTERISTICS FOR FCT821/823/825T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -6mA MIL. I _{OH} = -8mA COM'L.	2.4	3.3	—	V
			I _{OH} = -12mA MIL. I _{OH} = -15mA COM'L.	2.0	3.0	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL. I _{OL} = 48mA COM'L.	—	0.3	0.5	V
I _{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	V _{CC} = 0V, V _{IN} or V _O ≤ 4.5V		—	—	±1	μA

2567 Ink 08

OUTPUT DRIVE CHARACTERISTICS FOR FCT2821/2823/2825T

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
			I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is ±5μA at TA = -55°C.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \overline{EN} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \overline{EN} = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	1.5	3.5	mA
					FCT2xxxT	—	0.6	
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	FCTxxxT	—	2.0	5.5	
					FCT2xxxT		1.1	
			$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	FCTxxxT	—	3.8	7.3 ⁽⁵⁾	
					FCT2xxxT	—	1.5	
		$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	FCTxxxT	—	6.0	16.3 ⁽⁵⁾		
			FCT2xxxT	—	3.8	13.0 ⁽⁵⁾		

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT821/823/825AT FCT2821/2823/2825AT				FCT821/823/825BT FCT2821/2823/2825BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Yi (OE = LOW)	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tSU	Set-up Time HIGH or LOW Di to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW Di to CP		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW EN to CP		4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW EN to CP		2.0	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Yi		1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tREM	Recovery Time CLR to CP		6.0	—	7.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tW	CLR Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time OE to Yi	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time OE to Yi	CL = 5pF ⁽⁴⁾ RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT821/823/825CT FCT2821/2823/2825CT				FCT821DT FCT2821DT		FCT823DT FCT2823DT		Unit
			Com'l.		Mil.		Com'l.		Com'l.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay CP to Y _i (OE = LOW)	CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.2	1.5	5.0	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	1.5	8.5	
tsu	Set-up Time HIGH or LOW DI to CP	CL = 50pF RL = 500Ω	3.0	—	3.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW DI to CP		1.5	—	1.5	—	1.0	—	1.0	—	ns
tsu	Set-up Time HIGH or LOW EN to CP		3.0	—	3.0	—	3.0	—	3.0	—	ns
th	Hold Time HIGH or LOW EN to CP		0	—	0	—	0	—	0	—	ns
tPHL	Propagation Delay, CLR to Y _i		1.5	8.0	1.5	8.5	1.5	5.0	1.5	5.0	ns
tREM	Recovery Time CLR to CP		6.0	—	6.0	—	3.0	—	3.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	6.0	—	3.0	—	3.0	—	ns
tw	CLR Pulse Width LOW ⁽³⁾		6.0	—	6.0	—	3.0	—	3.0	—	ns
tPZH tPZL	Output Enable Time OE to Y _i	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	1.5	4.8	ns
		CL = 300pF ⁽⁴⁾ RL = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	1.5	9.0	
tPHZ tPLZ	Output Disable Time OE to Y _i	CL = 50pF ⁽⁴⁾ RL = 500Ω	1.5	6.0	1.5	6.0	1.5	4.0	1.5	4.0	ns
		CL = 50pF RL = 500Ω	1.5	6.5	1.5	6.5	1.5	4.0	1.5	4.0	

NOTES:

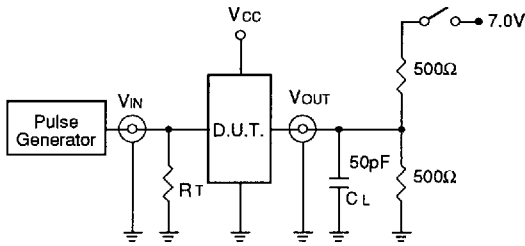
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

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6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2567 drw 05

SWITCH POSITION

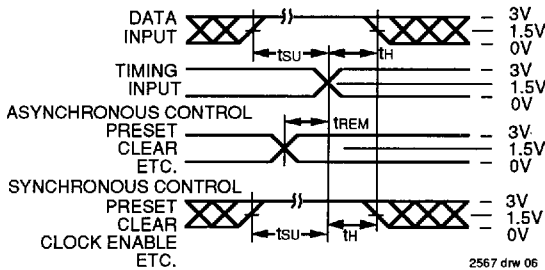
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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DEFINITIONS:

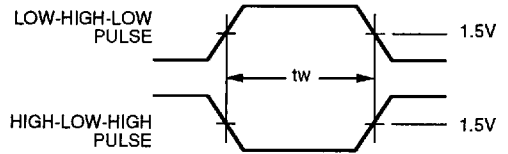
CL = Load capacitance; includes jig and probe capacitance.
RT = Termination resistance; should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



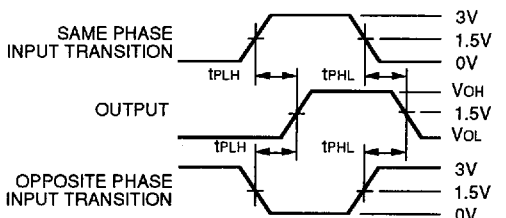
2567 drw 06

PULSE WIDTH



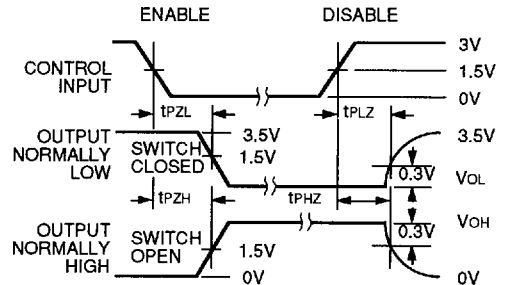
2567 drw 07

PROPAGATION DELAY



2567 drw 08

ENABLE AND DISABLE TIMES

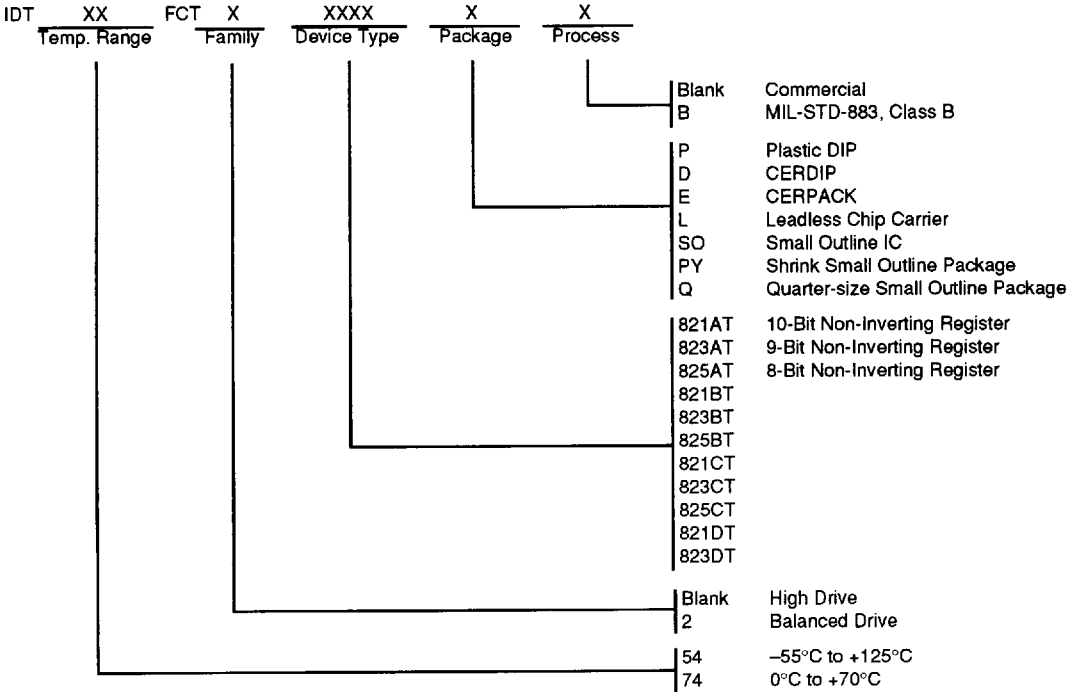


2567 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate \leq 1.0MHz; $t_f \leq$ 2.5ns; $t_r \leq$ 2.5ns

ORDERING INFORMATION



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