Signetics

FAST 74F259
Latch

FAST Products

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common reset input**
- **Useful as a 1-of-8 active-High decoder**

DESCRIPTION

The 74F259 addressable latch has four distinct modes of operation which are selectable by controlling the Master Reset ($\overline{MR}$) and Enable ($\overline{E}$) inputs (see Function Table). In the addressable latch mode, data at the Data inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the Enable should be held High (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}=\overline{E}=$Low), addressed outputs will follow the level of the Data input, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F259	7.5ns	31mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0°C$ to +70°C
16-Pin Plastic DIP	N74F259N
16-Pin Plastic SO	N74F259D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

| PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D	Data input	1.0/1.0	20μA/0.6mA
A_0, A_1, A_2	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}$	Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset inputs (active Low)	1.0/1.0	20μA/0.6mA
$Q_0 - Q_7$	Data outputs	50/33	1.0mA/20mA

NOTE:
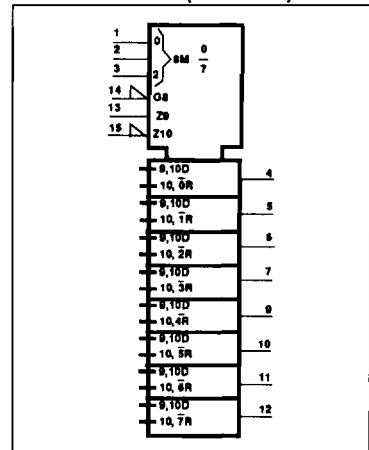One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
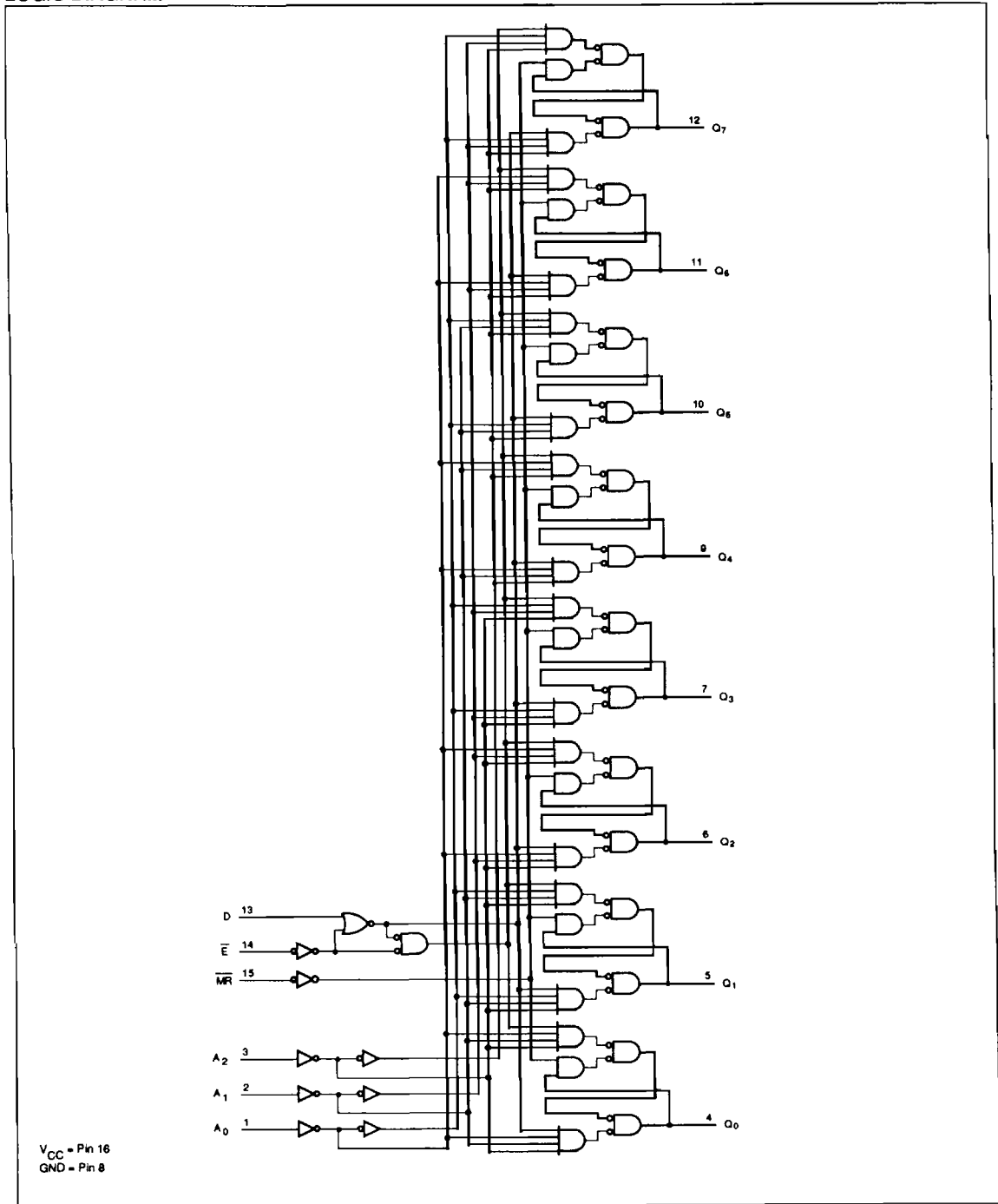
PIN CONFIGURATION

TOP VIEW

LOGIC SYMBOL

V_{CC} = Pin 16
GND = Pin 8
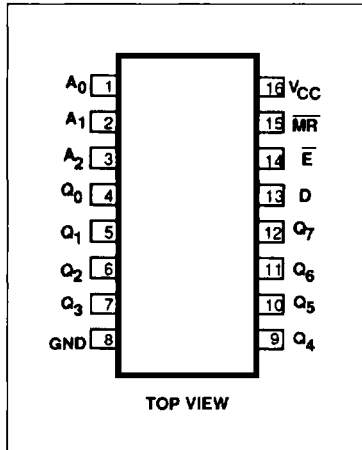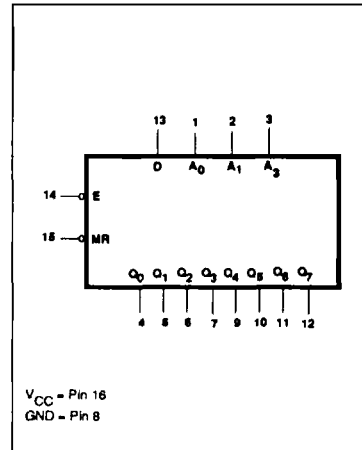
LOGIC SYMBOL(IEEE/IEC)

Latch

LOGIC DIAGRAM

V$_{CC}$ = Pin 16
GND = Pin 8

Latch

FUNCTION TABLE

INPUTS						OUTPUTS								OPERATING MODE
$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Master Reset
L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L	
L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L	Demultiplex
L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L	(active-High decoder
•	•	•	•	•	•	•	•	•	•	•	•	•	•	when D=H)
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d	
H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7	Store (do nothing)
H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7	
H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7	
H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7	Addressable
•	•	•	•	•	•	•	•	•	•	•	•	•	•	Latch
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d	

H = High voltage level
L = Low voltage level
X = Don't care
d = High or Low data one setup time prior to the Low-to-High Enable transition
q = Lower case letters indicate the state of the referenced output established during the last
    cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
		V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
		V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				-0.6	mA
I_{OS}	Short circuit output current[3]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX		24	46	mA
		I_{CCL}			37	75	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 1	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	10.0 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	12.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 2	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 10.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	7.0	9.0	4.5	10.0	ns

AC SETUP REQUIREMENTS

| SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			$T_A = +25°C$ $V_{CC} = 5V$ $C_L = 50pF$ $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF$ $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 4	3.0 6.5			3.0 7.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n to $\overline{E}^1$	Waveform 5	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n to $\overline{E}^2$	Waveform 5	0 0			0 0		ns
$t_w(L)$	$\overline{E}$ Pulse width, Low	Waveform 1	7.5			8.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	3.0			3.0		ns

NOTES:
1. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time before the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
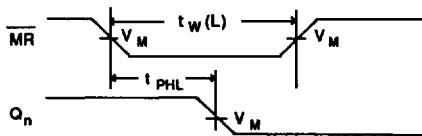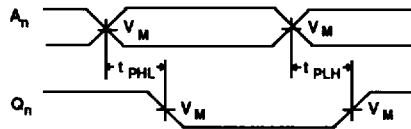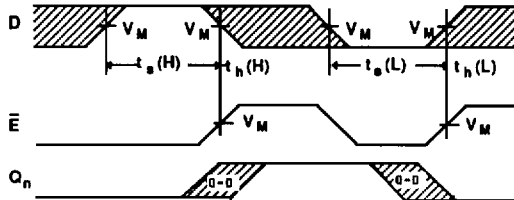
Latch
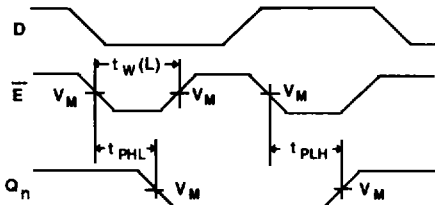
AC WAVEFORMS

Waveform 1. Propagation Delay, Enable Input To Output, Enable Pulse Width

Waveform 2. Propagation Delay Address To Output

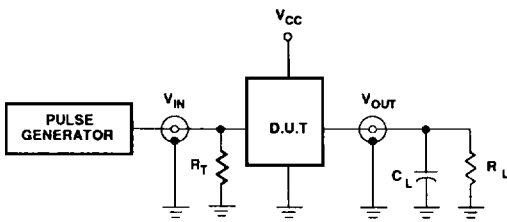Waveform 3. Master Reset Pulse Width And Master Reset to Output Delay

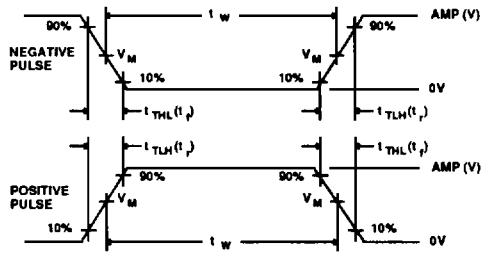Waveform 4. Data Setup And Hold Times
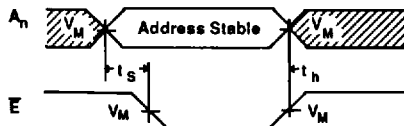
Waveform 5. Address Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

Test Circuit For Totem-Pole Outputs

$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns