3-17V 1A Step-Down Converter in 2x2 WSON Package

Check for Samples: TPS62160, TPS62161, TPS62162, TPS62163

FEATURES

- **DCS-Control™ Topology**
- **Input Voltage Range: 3 to 17 V**
- **Up to 1A Output Current**
- **Adjustable Output Voltage from 0.9 to 6 V**
- **Fixed Output Voltage Versions**
- **Seamless Power Save Mode Transition**
- **Typically 17µA Quiescent Current**
- **Power Good Output**
- **100% Duty Cycle Mode**
- **Short Circuit Protection**
- **Over Temperature Protection**
- **Available in a 2 × 2 mm, WSON-8 Package**

APPLICATIONS

- **Standard 12V Rail Supplies**
- **POL Supply from Single or Multiple Li-Ion Battery**
- **LDO Replacement**
- **Embedded Systems**
- **Digital Still Camera, Video**
- **Mobile PC's, Tablet, Modems**

DESCRIPTION

The TPS6216X family is an easy to use synchronous step down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.25MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology.

With its wide operating input voltage range of 3V to 17V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12V intermediate power rails. It supports up to 1A continuous output current at output voltages between 0.9V and 6V (with 100% duty cycle mode).

Power sequencing is also possible by configuring the Enable and open-drain Power Good pins.

In Power Save Mode, the devices show quiescent current of about 17µA from VIN. Power Save Mode, entered automatically and seamlessly if load is small, maintains high efficiency over the entire load range. In Shutdown Mode, the device is turned off and shutdown current consumption is less than 2µA.

The device, available in adjustable and fixed output voltage versions, is packaged in an 8-pin WSON package measuring 2 × 2 mm (DSG).

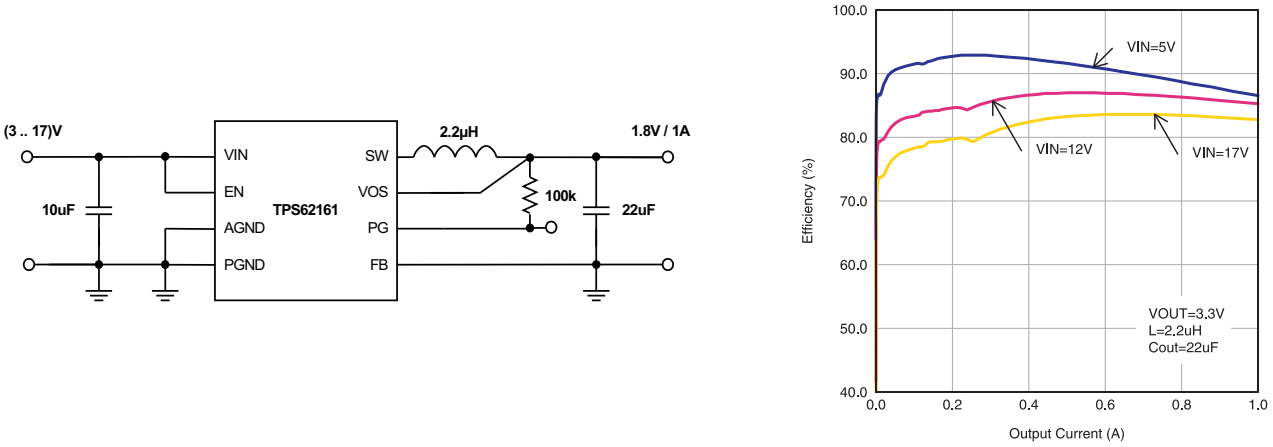


Figure 1. Typical Application and Efficiency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	OUTPUT VOLTAGE	PART NUMBER(2)	PACKAGE	ORDERING	PACKAGE MARKING
-40°C to 85°C	adjustable	TPS62160	8-Pin WSON	TPS62160DSG	QTV
	1.8 V	TPS62161		TPS62161DSG	QUB
	3.3 V	TPS62162		TPS62162DSG	QUC
	5.0 V	TPS62163		TPS62163DSG	QUD
	adjustable	TPS62160(3)	8-Pin MSOP	TPS62160DGK	62160

(1) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.
(2) Contact the factory to check availability of other fixed output voltage versions.
(3) Product preview. Contact the factory to check availability of this package version.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Pin voltage range(2)	VIN	–0.3 to 20	V
	EN	–0.3 to V_{IN}+0.3	
	SW(3)	-0.3 to V_{IN}+0.3	V
	FB, PG, VOS	–0.3 to 7	V
Power Good sink current	PG	10	mA
Temperature range	Operating junction temperature range, T_J	–40 to 125	°C
	Storage temperature range, T_{stg}	–65 to 150	
ESD rating(4)	HBM Human body model	2	kV
	CDM Charge device model	0.5	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) This is a DC voltage rating.
(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS6216X DSG (8) PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	61.8	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	61.3	
θ_{JB}	Junction-to-board thermal resistance	15.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	15.4	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance	8.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply Voltage, V_{IN}	3		17	V
Operating free air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

over free-air temperature range (T_A=-40°C to +85°C), typical values at V_{IN}=12V and T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input Voltage Range (1)		3		17	V
I_Q	Operating Quiescent Current	EN=High, I_{OUT}=0mA, device not switching		17	25	µA
I_{SD}	Shutdown Current (2)	EN=Low		1.5	4	µA
V_{UVLO}	Undervoltage Lockout Threshold	Falling Input Voltage	2.6	2.7	2.82	V
		Hysteresis		180		mV
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, PG)						
V_{EN_H}	High Level Input Threshold Voltage (EN)		0.9			V
V_{EN_L}	Low Level Input Threshold Voltage (EN)				0.3	V
I_{LKG_EN}	Input Leakage Current (EN)	EN=V_{IN} or GND		0.01	1	µA
V_{TH_PG}	Power Good Threshold Voltage	Rising (%V_{OUT})	92	95	98	%
		Falling (%V_{OUT})	87	90	93	
V_{OL_PG}	Power Good Output Low	I_{PG}=-2mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current (PG)	V_{PG}=1.8V		1	400	nA
POWER SWITCH						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN}≥6V		300	600	mΩ
		V_{IN}=3V		430		
	Low-Side MOSFET ON-Resistance	V_{IN}≥6V		120	200	mΩ
		V_{IN}=3V		165		
I_{LIMF}	High-Side MOSFET Forward Current Limit (3)	V_{IN}=12V, T_A=25°C	1.45	1.95	2.45	A

(1) The device is still functional down to Under Voltage Lockout (see parameter V_{UVLO}).
(2) Current into VIN pin.
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit And Short Circuit Protection section).

ELECTRICAL CHARACTERISTICS (continued)

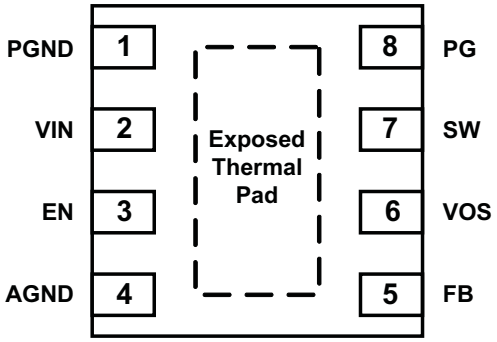
over free-air temperature range (T_A=-40°C to +85°C), typical values at V_{IN}=12V and T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
VREF	Internal Reference Voltage(4)			0.8		V
I_{LKG_FB}	Pin Leakage Current (FB)	V_{FB}=1.2V		5	400	nA
V_{OUT}	Output Voltage Range (TPS62160)	$V_{IN} \geq V_{OUT}$	0.9		6.0	V
	Initial Output Voltage Accuracy(5)	PWM mode operation, $V_{IN} \geq V_{OUT}$+1V	–3		3	%
		Power Save Mode operation(6)	-3.5		4	
	DC Output Voltage Load Regulation(7)	V_{IN}=12V, V_{OUT}=3.3V, PWM mode operation		0.05		% / A
	DC Output Voltage Line Regulation (7)	3V ≤ V_{IN} ≤ 17V, V_{OUT}=3.3V, I_{OUT}= 0.5A, PWM mode operation		0.02		% / V

(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For fixed voltage versions, the (internal) resistive feedback divider is included.
(6) In Power Save Mode, increased voltage ripple has to be considered.
(7) Line and load regulation are depending on external component selection and layout (see Figure 13 and Figure 14).

DEVICE INFORMATION

DSG PACKAGE
(TOP VIEW)

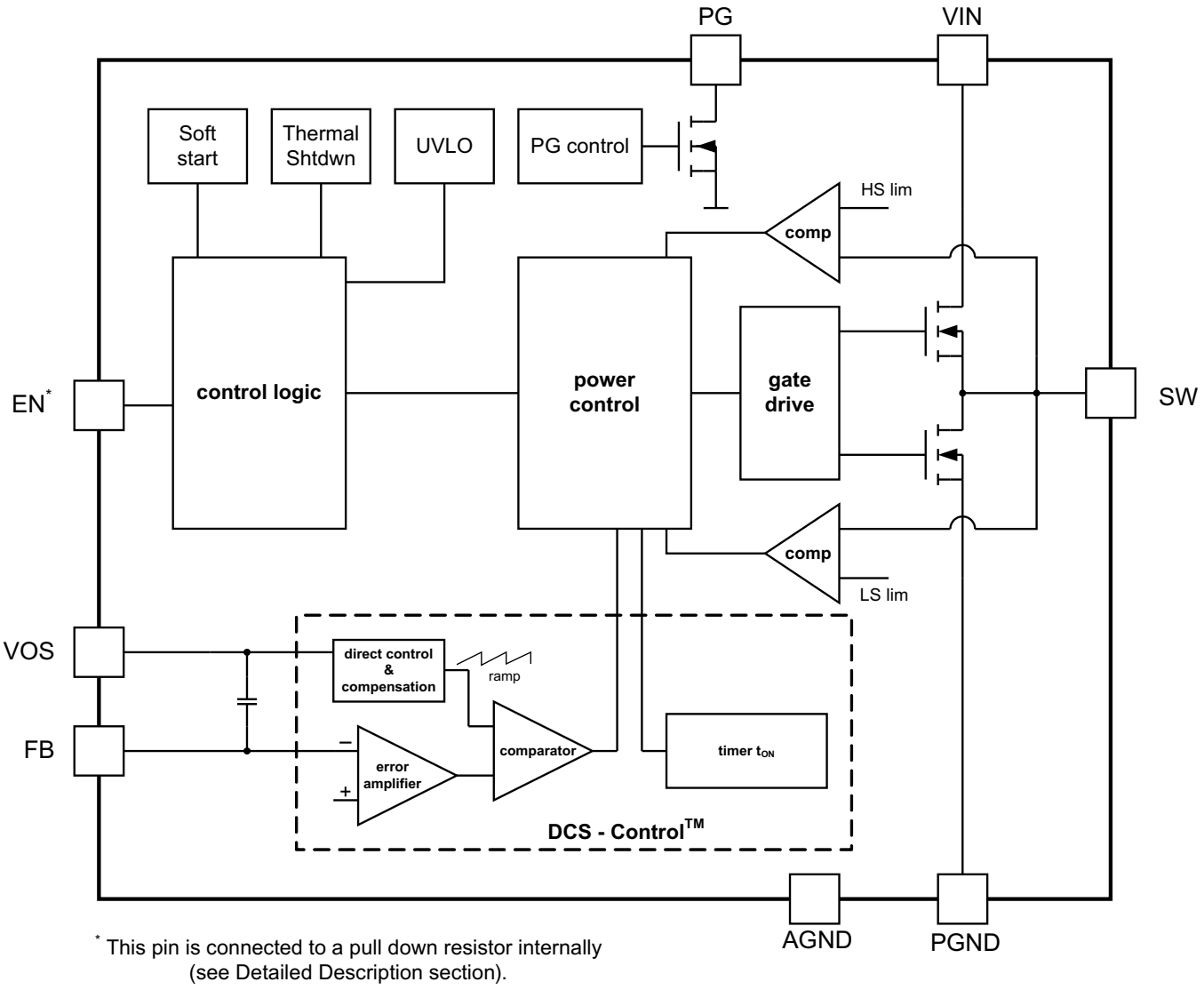


Terminal Functions

PIN(1)		I/O	DESCRIPTION
NAME	NO.		
PGND	1		Power ground
VIN	2	I	Supply voltage
EN	3	I	Enable input (High = enabled, Low = disabled)
AGND	4		Analog Ground
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	I	Output voltage sense pin and connection for the control loop circuitry.
SW	7	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad			Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see DETAILED DESCRIPTION and APPLICATION INFORMATION sections.

FUNCTIONAL BLOCK DIAGRAM



* This pin is connected to a pull down resistor internally (see Detailed Description section).

Figure 2. TPS62160 (adjustable output voltage)

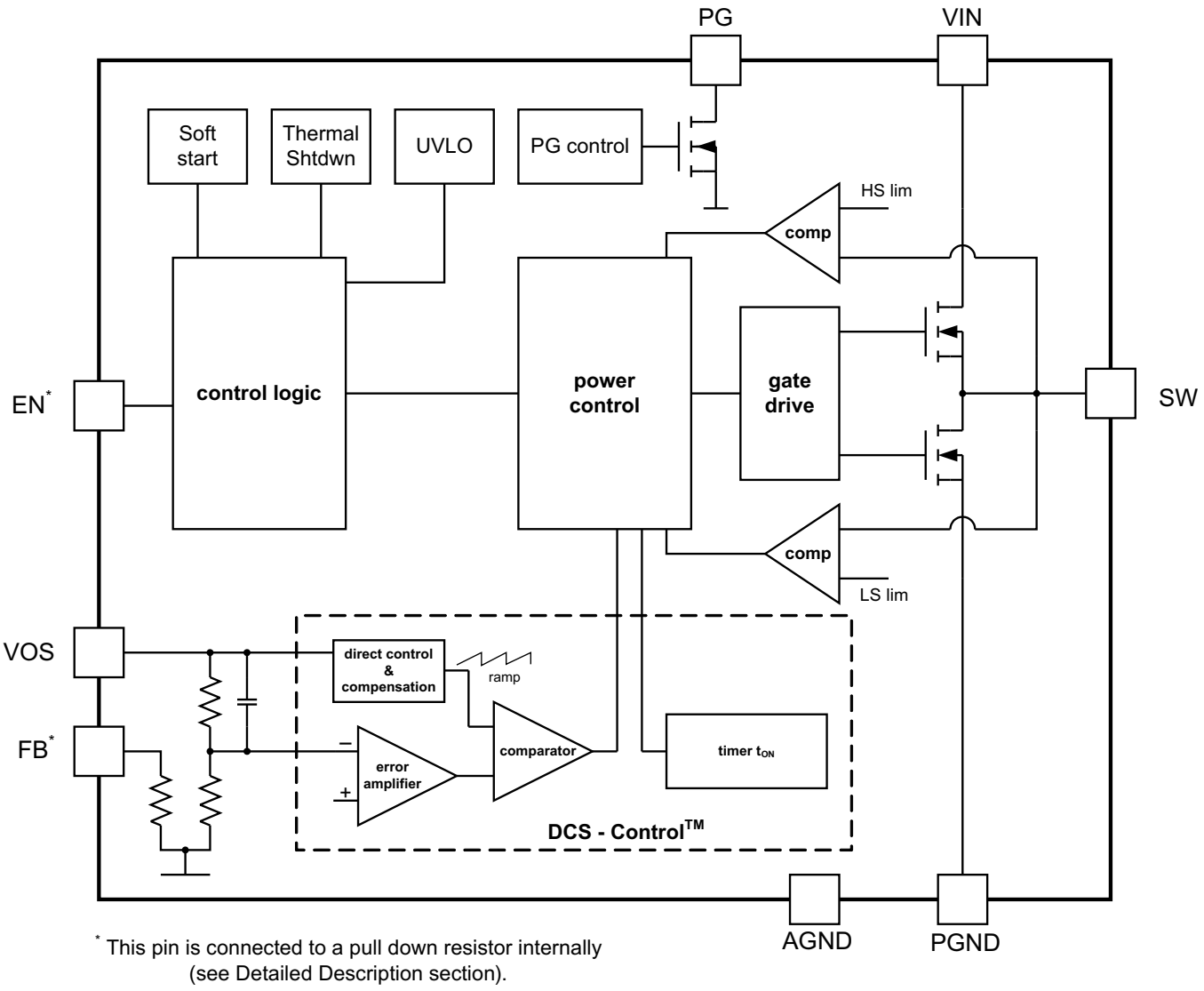


Figure 3. TPS62161/2/3 (fixed output voltage)

PARAMETER MEASUREMENT INFORMATION

List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17V, 1A Step-Down Converter, WSON	TPS62160DSG, Texas Instruments
L1	2.2uH, 1.4A, 3 x 2.8 x 1.2 mm	VLF3012ST-2R2M1R4, TDK
Cin	10µF, 25V, Ceramic	Standard
Cout	22µF, 6.3V, Ceramic	Standard
R1	depending on Vout	
R2	depending on Vout	
R3	100kΩ, Chip, 0603, 1/16W, 1%	Standard

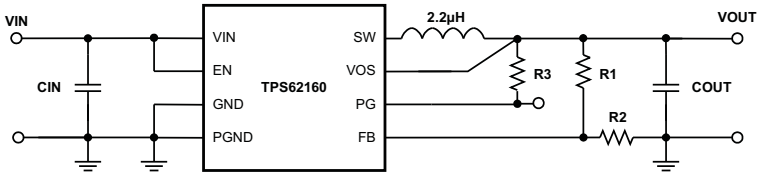


Figure 4. Measurement Setup

TYPICAL CHARACTERISTICS

Table of Graphs

DESCRIPTION		FIGURE
Efficiency	vs Output Current, vs Input Voltage	5 - 12
Output voltage	vs Output current (Load regulation)	13
	vs Input Voltage (Line regulation)	14
Switching Frequency	vs Input Voltage	15
	vs Output Current	16
Quiescent Current	vs Input Voltage	17
Shutdown Current	vs Input Voltage	18
Power FET RDS(on)	vs Input Voltage (High-Side, Low-Side)	19, 20
Output Voltage Ripple	vs output Current	21
Maximum Output Current	vs Input Voltage	22
Waveforms	PWM-PSM-PWM Mode Transition	23, 24
	Load Transient Response	25 - 28
	Startup	29, 30
	Typical Power Save Mode Operation	31
	Typical PWM Mode Operation	32

EFFICIENCY vs OUTPUT CURRENT

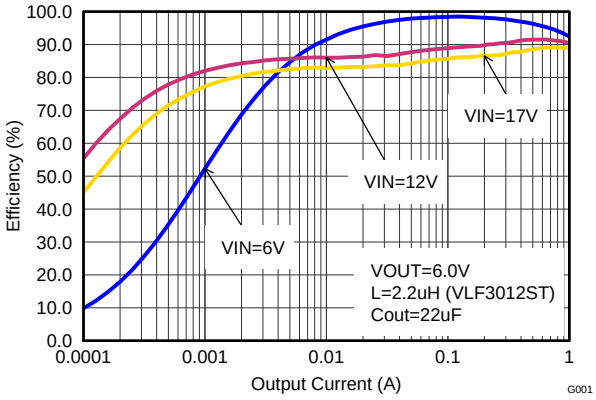


Figure 5. Vout=6V

EFFICIENCY vs INPUT VOLTAGE

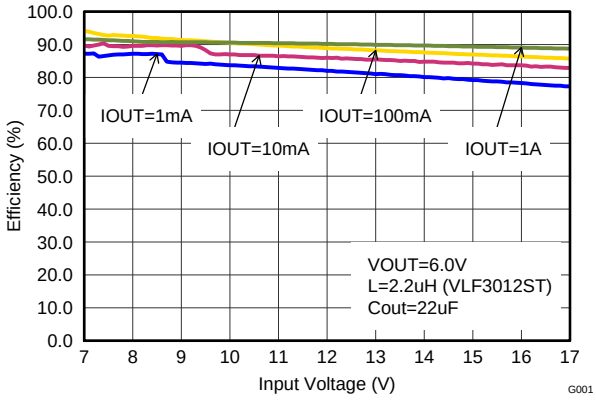


Figure 6. Vout=6V

EFFICIENCY vs OUTPUT CURRENT

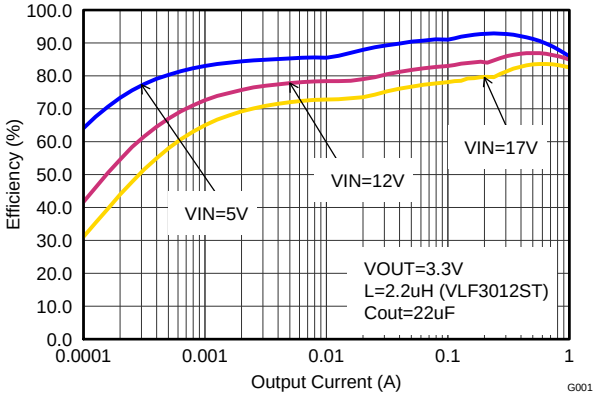


Figure 7. Vout=3.3V

EFFICIENCY vs INPUT VOLTAGE

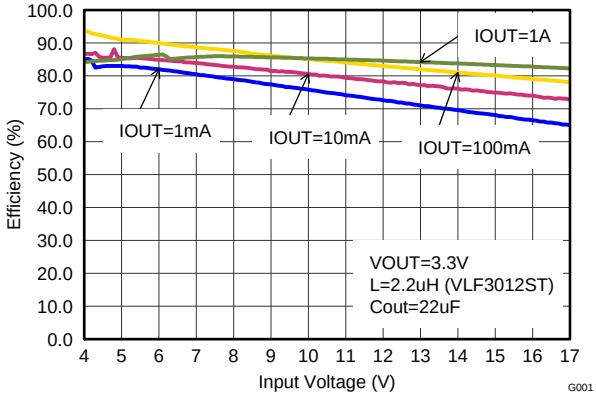


Figure 8. Vout=3.3V

EFFICIENCY vs OUTPUT CURRENT

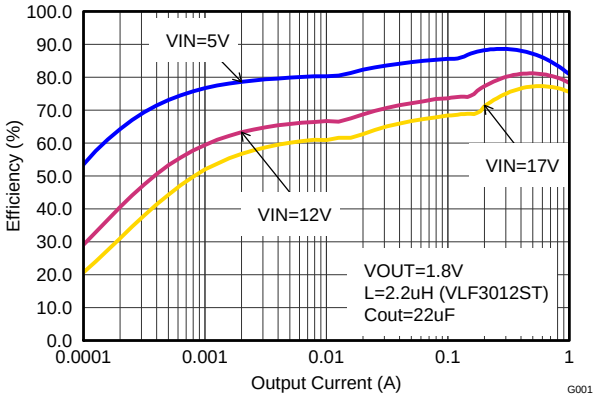


Figure 9. Vout=1.8V

EFFICIENCY vs INPUT VOLTAGE

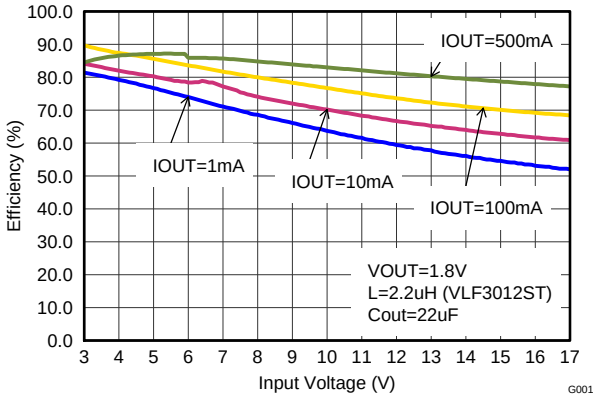


Figure 10. Vout=1.8V

EFFICIENCY vs OUTPUT CURRENT

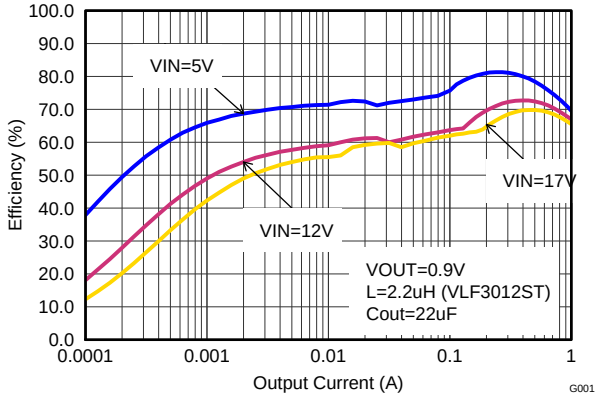


Figure 11. Vout=0.9V

EFFICIENCY vs INPUT VOLTAGE

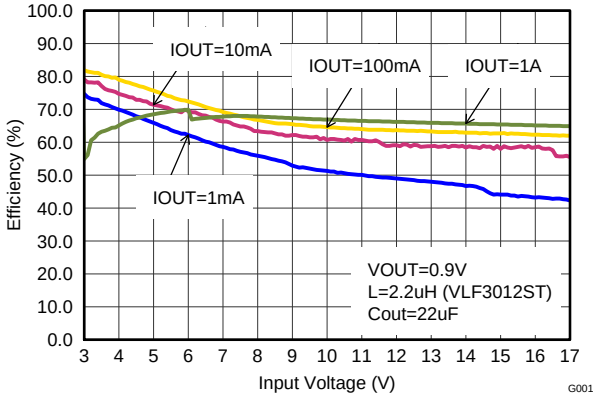


Figure 12. Vout=0.9V

OUTPUT VOLTAGE vs OUTPUT CURRENT

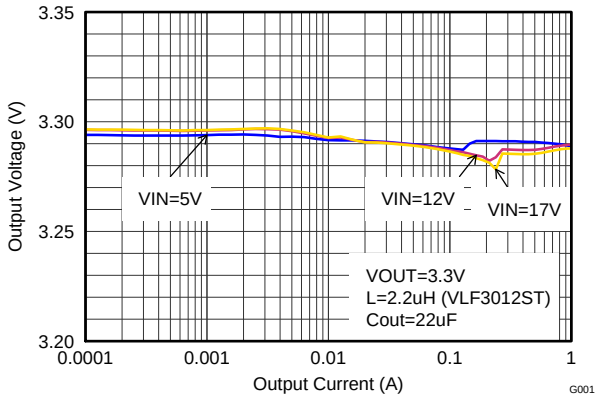


Figure 13. Output Voltage Accuracy (Load Regulation)

OUTPUT VOLTAGE vs INPUT VOLTAGE

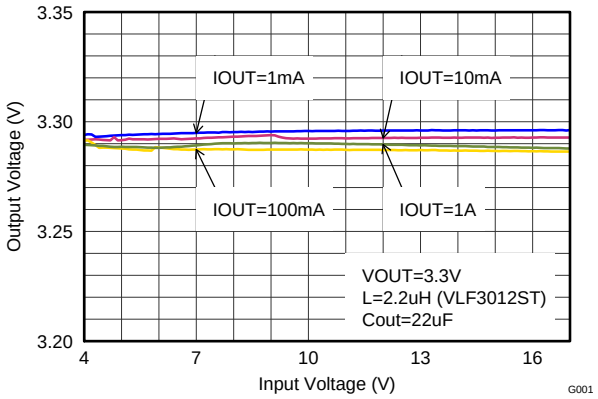


Figure 14. Output Voltage Accuracy (Line Regulation)

SWITCHING FREQUENCY vs OUTPUT CURRENT

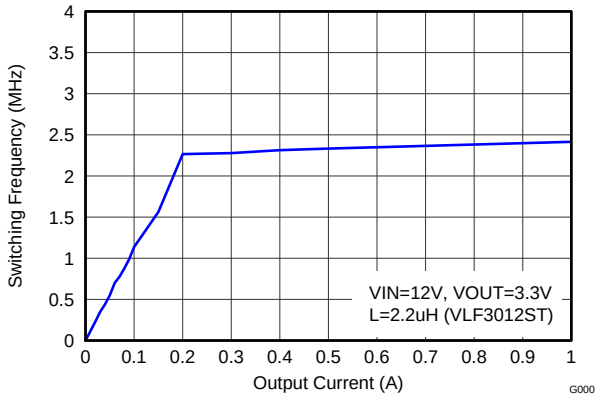


Figure 15. Switching Frequency

SWITCHING FREQUENCY vs INPUT VOLTAGE

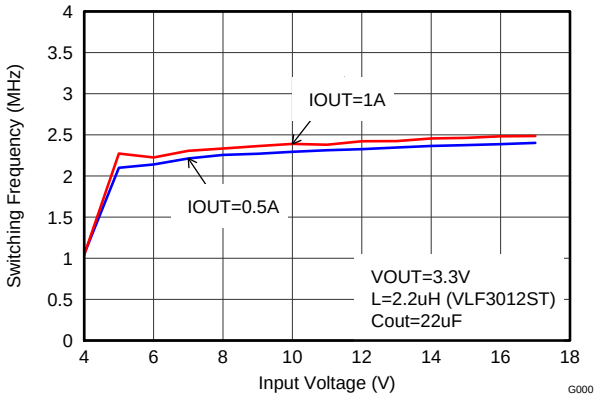


Figure 16. Switching Frequency

INPUT CURRENT vs INPUT VOLTAGE

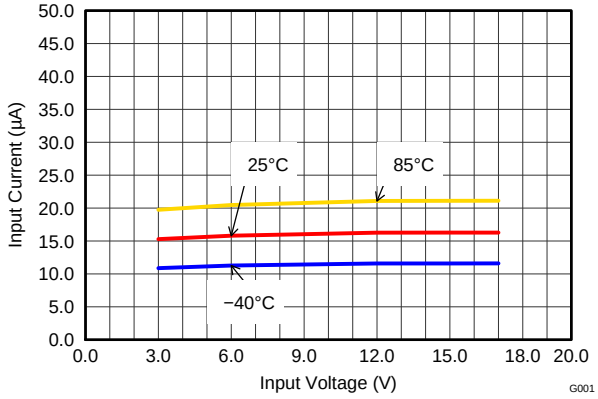


Figure 17. Quiescent Current

INPUT CURRENT vs INPUT VOLTAGE

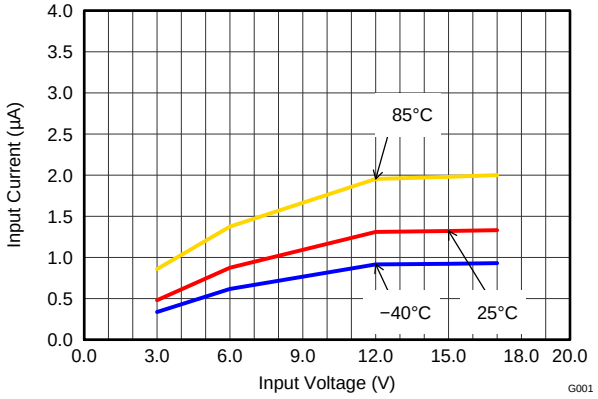


Figure 18. Shutdown Current

STATIC DRAIN-SOURCE-RESISTANCE (R_{DSon}) vs INPUT VOLTAGE

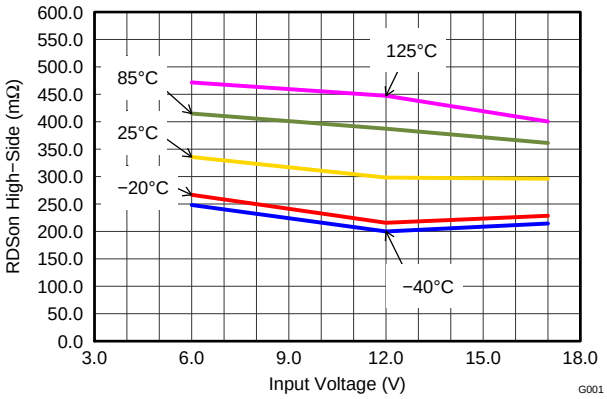


Figure 19. High-Side Switch

STATIC DRAIN-SOURCE-RESISTANCE (R_{DSon}) vs INPUT VOLTAGE

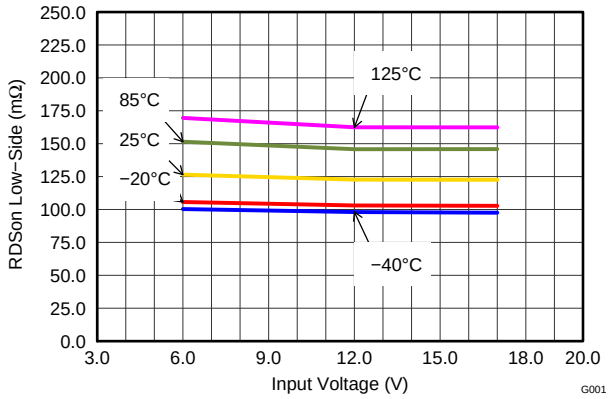


Figure 20. Low-Side Switch

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

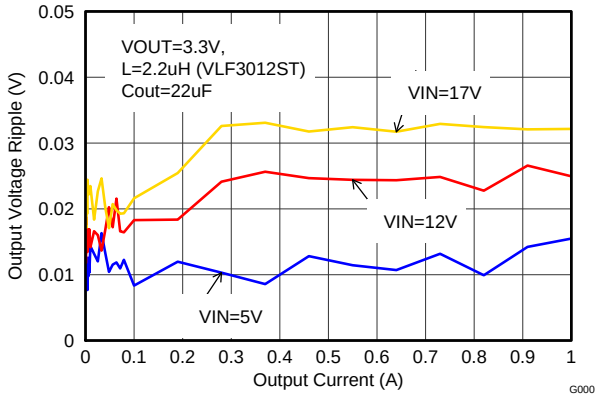


Figure 21. Output Voltage Ripple

OUTPUT CURRENT vs INPUT VOLTAGE

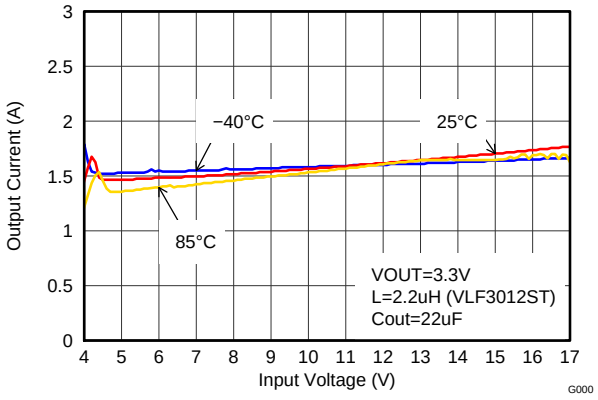


Figure 22. Maximum Output Current

OUTPUT VOLTAGE vs TIME

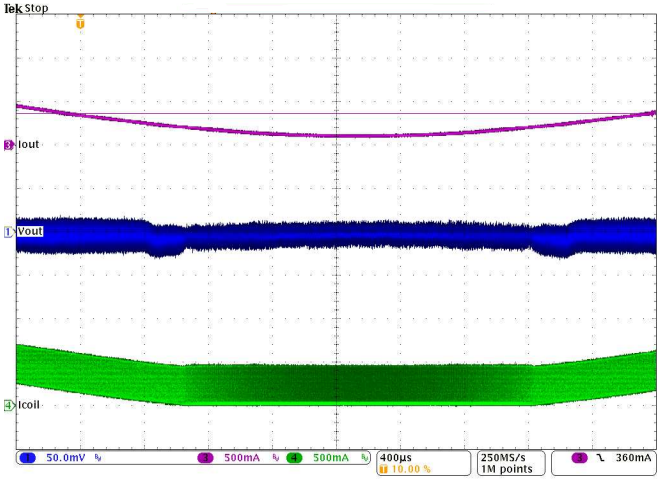


Figure 23. PWM to PSM Mode Transition

OUTPUT VOLTAGE vs TIME

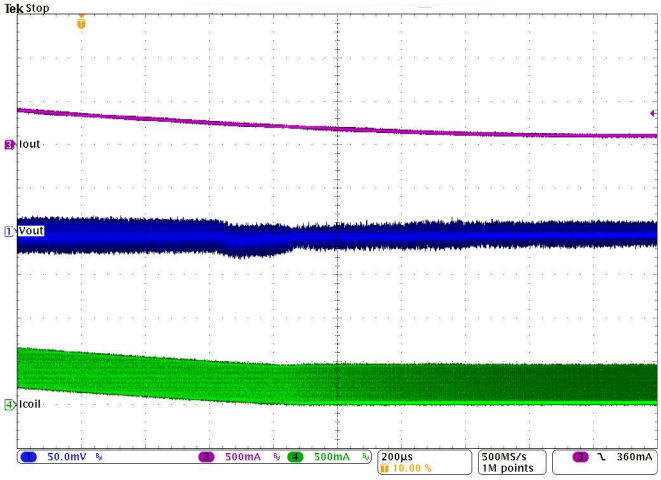


Figure 24. PSM to PWM Mode Transition

TRANSIENT RESPONSE vs TIME

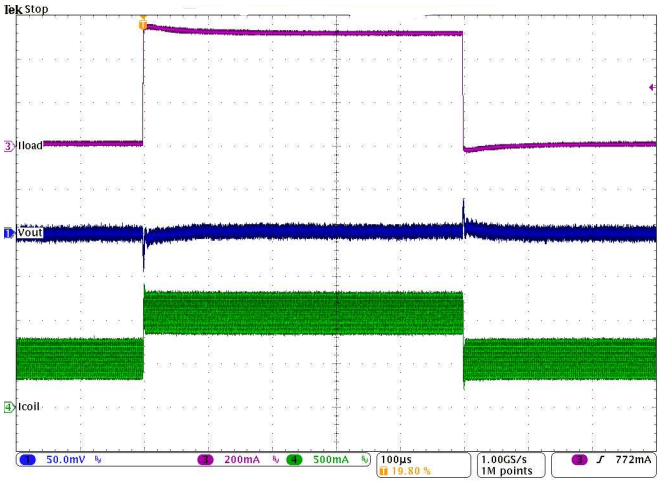


Figure 25. Load Transient Response in PWM mode (500mA to 1A)

TRANSIENT RESPONSE vs TIME

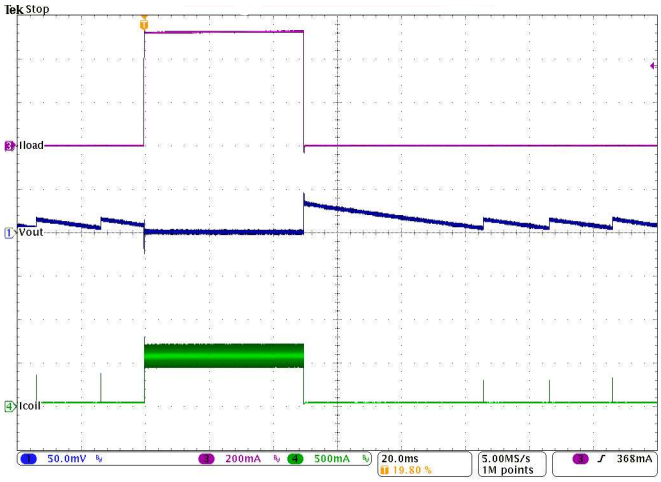


Figure 26. Load Transient Response from Power Save Mode (100mA to 500mA)

TRANSIENT RESPONSE
vs
TIME

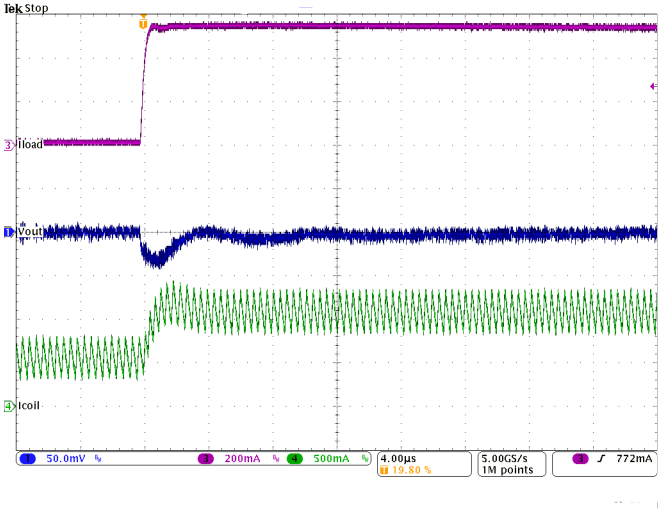


Figure 27. Load Transient Response in PWM mode (500mA to 1A), rising edge

TRANSIENT RESPONSE
vs
TIME

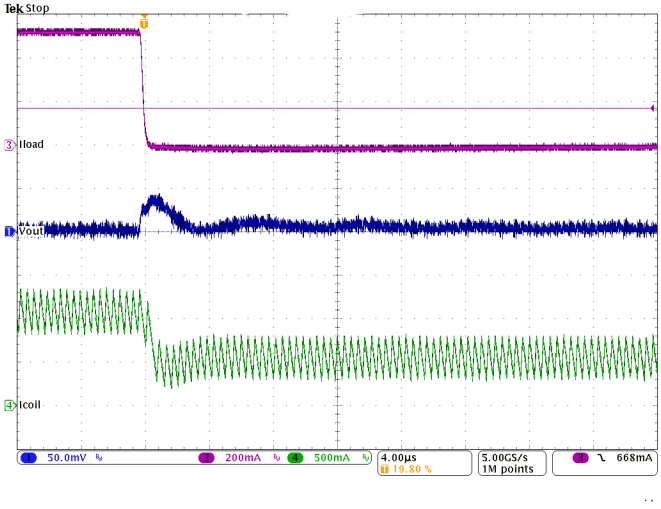


Figure 28. Load Transient Response in PWM mode (500mA to 1A), falling edge

STARTUP TO VOUT=3.3V
vs
TIME

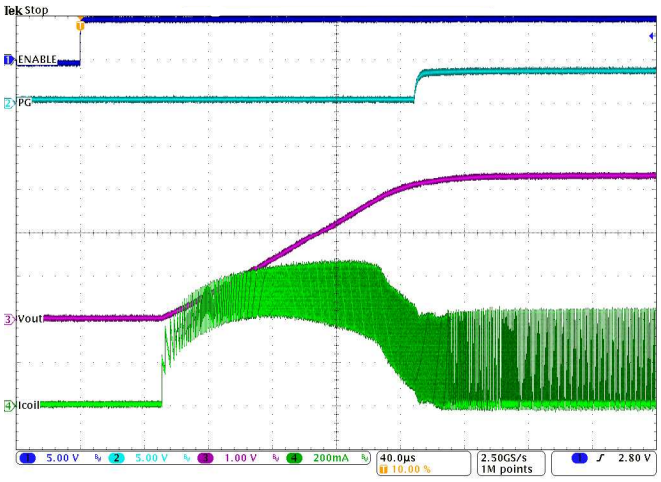


Figure 29. Startup with Iout=100mA

STARTUP TO VOUT=3.3V
vs
TIME

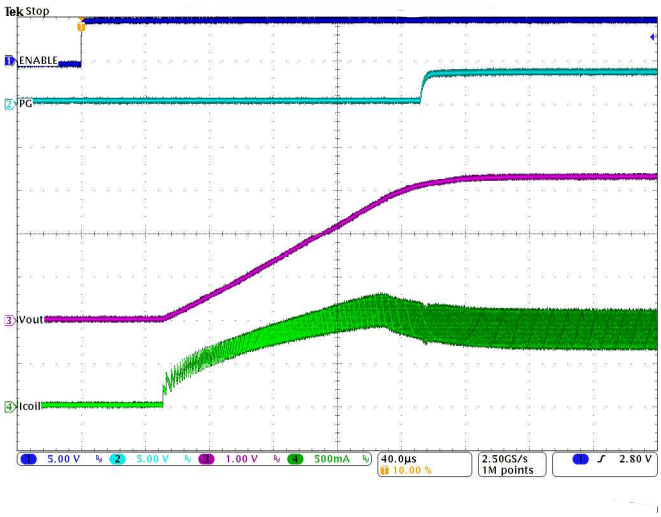


Figure 30. Startup with Iout=1A

PSM MODE OPERATION
vs
TIME

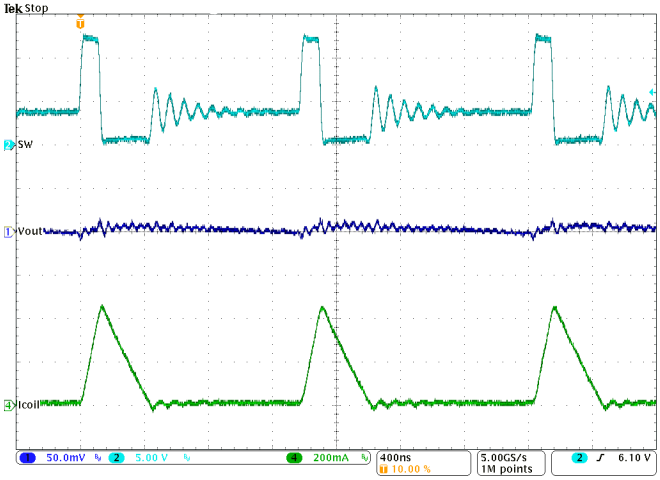


Figure 31. Typical Operation in Power Save Mode (Iout=66mA)

PWM MODE OPERATION
vs
TIME

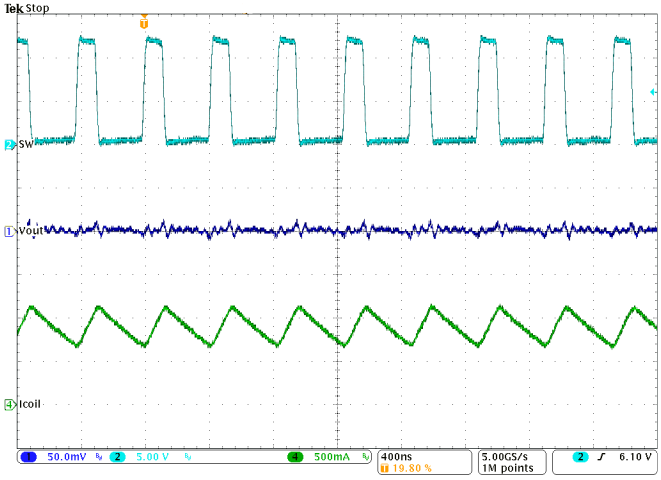


Figure 32. Typical Operation in PWM Mode (Iout=1A)

DETAILED DESCRIPTION

Device Operation

The TPS6216X synchronous switched mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 1A.

The TPS6216X family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

Pulse Width Modulation (PWM) Operation

The TPS6216X operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25MHz. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

Power Save Operation

The TPS6216X's built in Power Save Mode will be entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

TPS6216X includes a fixed on-time circuitry. This on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 420ns \tag{1}$$

For very small output voltages, the on-time increases beyond the result of Equation 1, to stay above an absolute minimum on-time, $t_{ON(min)}$, which is around 80ns to limit switching losses. The peak inductor current in PSM can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above V_{OUT}, the TPS6216X won't enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D=Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, e.g. for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \quad (3)$$

where

I_{OUT} is the output current,
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET and
R_L is the DC resistance of the inductor used.

Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is Low, an internal pull-down resistor of about 400kΩ is connected and keeps it Low, to avoid bouncing. To avoid ON/OFF oscillations, a minimum slew rate of about 50mV/µs is recommended for the EN signal.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

Softstart

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50µs and V_{OUT} rises with a slope of about 25mV/µs. See Figure 29 and Figure 30 for typical startup operation.

The TPS6216X can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

Current Limit And Short Circuit Protection

The TPS6216X devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET will be turned off. Avoiding shoot through current, the low-side FET will be switched on to sink the inductor current. The high-side FET will turn on again, only if the current in the low-side FET has decreased below the low side current limit threshold.

The output current of the device is limited by the current limit (see ELECTRICAL CHARACTERISTICS). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \quad (4)$$

where

I_{LIMF} is the static current limit, specified in the electrical characteristic table,
L is the inductor value,
V_L is the voltage across the inductor and
t_{PD} is the internal propagation delay.

The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF\_HS} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \quad (5)$$

Care on the current limit has to be taken if the input voltage is high and very small inductances are used.

Power Good (PG)

The TPS6216X has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7V). It can sink 2mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown.

Under Voltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180mV.

Thermal Shutdown

The junction temperature (Tj) of the device is monitored by an internal temperature sensor. If Tj exceeds 160°C (typ), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When Tj decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

APPLICATION INFORMATION

The following information is intended to be a guideline through the individual power supply design process.

Programming The Output Voltage

While the output voltage of the TPS62160 is adjustable, the TPS62161/2/3 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9V to 6V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6. It is recommended to choose resistor values which allow a cross current of at least 2uA, meaning the value of R2 shouldn't exceed 400kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin to about 7.4V.

External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6216X is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see Output Filter And Loop Stability section). Table 1 can be used to simplify the output filter component selection.

Table 1. Recommended LC Output Filter Combinations(1)

	10µF	22µF	47µF	100µF	200µF	400µF
1µH						
2.2µH		√(2)	√	√	√	
3.3µH		√	√	√	√	
4.7µH						

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.
(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in SLVA463.

Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \tag{8}$$

where

I_L(max) is the maximum inductor current,
ΔI_L is the Peak to Peak Inductor Ripple Current,
L(min) is the minimum effective inductor value and
f_{SW} is the actual PWM Switching Frequency.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6216X and are recommended for use:

Table 2. List of Inductors

Type	Inductance [µH]	Current [A](1)	Dimensions [L x B x H] mm	MANUFACTURER
VLF3012ST-2R2M1R4	2.2µH, ±20%	1.9A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2µH, ±20%	1.9A	3.0 x 2.5 x 1.2	TDK
VLS252012T-2R2M1R3	2.2uH, ±20%	1.3A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2µH, ±20%	1.9A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3µH, ±20%	1.6A	3.0 x 3.0 x 1.2	Coilcraft
LPS3015-332ML_	3.3uH, ±20%	1.4A	3.0 x 3.0 x 1.4	Coilcraft
NR3015T-2R2M	2.2uH, ±20%	1.5A	3.0 x 3.0 x 1.5	Taiyo Yuden
744025003	3.3uH, ±20%	1.5A	2.8 x 2.8 x 2.8	Wuerth
PSI25201B-2R2MS	2.2uH, ±20%	1.3A	2.0 x 2.5 x 1.2	Cyntec

(1) I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

TPS6216X can be run with an inductor as low as 2.2µH. However, for applications with low input voltages, 3.3µH is recommended, to allow the full output current. The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \tag{9}$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

Capacitor Selection

Output Capacitor

The recommended value for the output capacitor is 22uF. The architecture of the TPS6216X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

Input Capacitor

For most applications, 10µF will be sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

Output Filter And Loop Stability

The devices of the TPS6216X family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 10:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{10}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 1 and are recommended for use. Different values may work, but care has to be taken on the loop stability which will be affected. More information including a detailed L-C stability matrix can be found in SLVA463.

The TPS6216X devices, both fixed and adjustable versions, include an internal 25pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 11 and Equation 12:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25pF} \tag{11}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{12}$$

Though the TPS6216X devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in SLVA289 and SLVA466.

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see DC Bias effect NOTE in Capacitor Selection section).

Layout Considerations

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6216X demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

Provide low inductive and resistive paths to ground for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high dv/dt signals (e.g. SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission (e.g. feedback divider) should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the VIN and PGND pin of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors, R_1 and R_2, should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and even more to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load.

A single point grounding scheme should be implemented with all grounds (AGND, PGND and the thermal pad) connecting at the IC's exposed thermal pad. See Figure 33 for the recommended layout of the TPS6216X. More detailed information can be found in the EVM Users Guide, SLVU483.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the Exposed Thermal Pad can be connected to a floating circuit board trace, the device will have better thermal performance if it is connected to a larger ground plane. The Exposed Thermal Pad is electrically connected to AGND.

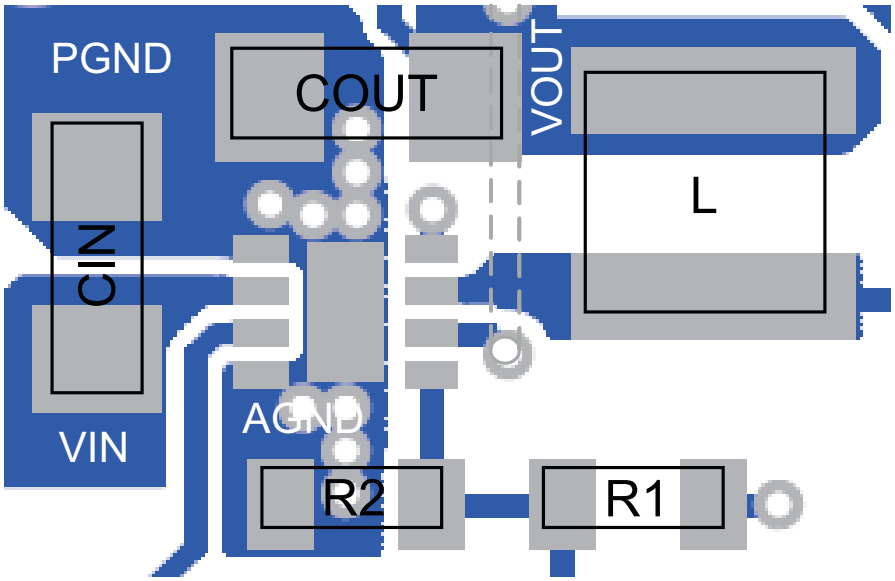


Figure 33. Layout Example

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the Exposed Thermal Pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS6216X is designed for a maximum operating junction temperature (T_j) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

Typical Applications

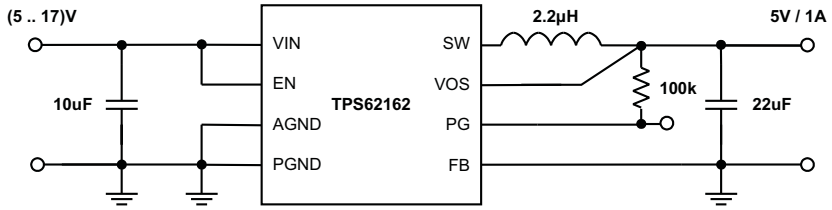


Figure 34. 5V/1A Power Supply

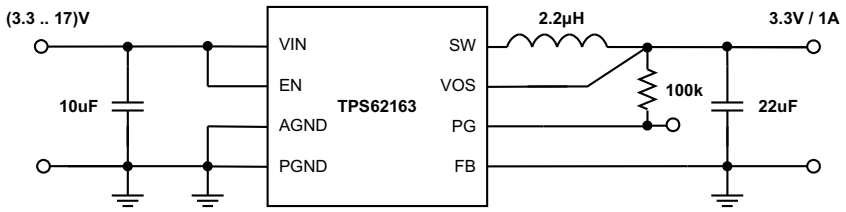


Figure 35. 3.3V/1A Power Supply

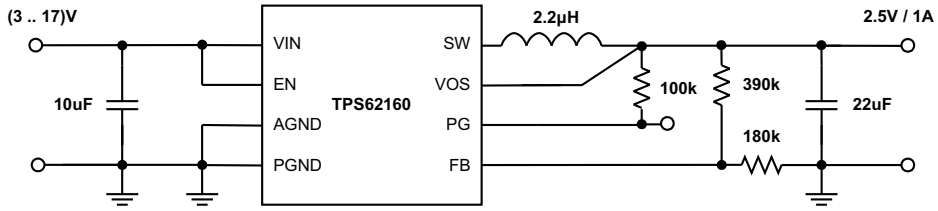


Figure 36. 2.5V/1A Power Supply

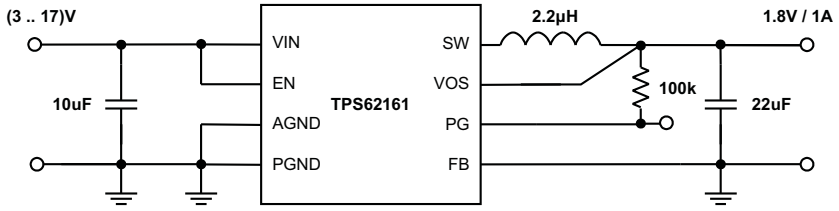


Figure 37. 1.8V/1A Power Supply

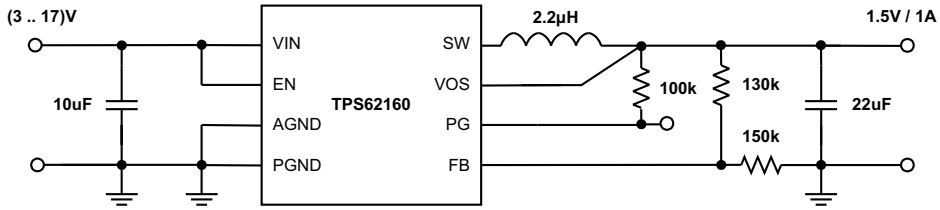


Figure 38. 1.5V/1A Power Supply

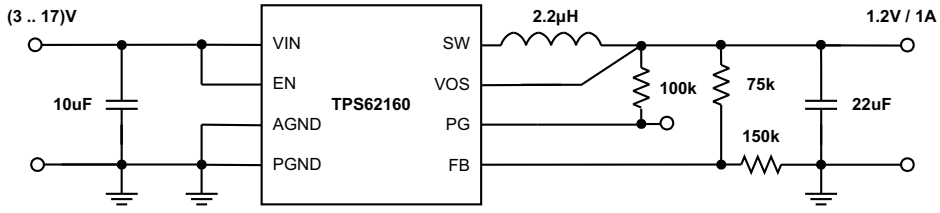


Figure 39. 1.2V/1A Power Supply

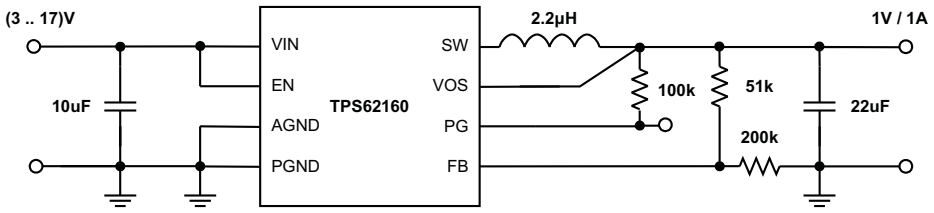


Figure 40. 1V/1A Power Supply

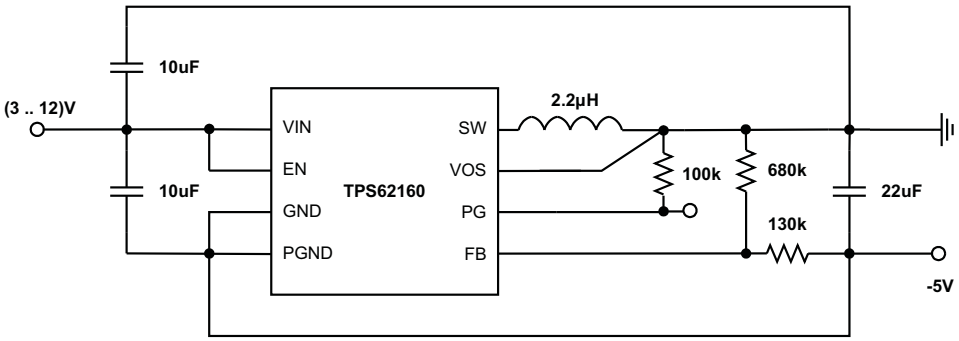


Figure 41. -5V Inverting Power Supply

The TPS6216X can be used as inverting power supply by rearranging external circuitry as shown in Figure 41. As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17V.

In inverting operation mode, the output current capability is reduced by the input to output voltage conversion ratio:

$$I_{OUT} = \frac{V_{IN}}{V_{OUT}} \cdot I_{IN} \cdot \eta \tag{13}$$

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22uF is recommended. A detailed design example is given in SLVA469.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS62160DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	62160	Samples
TPS62160DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	62160	Samples
TPS62160DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTV	Samples
TPS62160DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QTV	Samples
TPS62161DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUB	Samples
TPS62161DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUB	Samples
TPS62162DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUC	Samples
TPS62162DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUC	Samples
TPS62163DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUD	Samples
TPS62163DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	QUD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

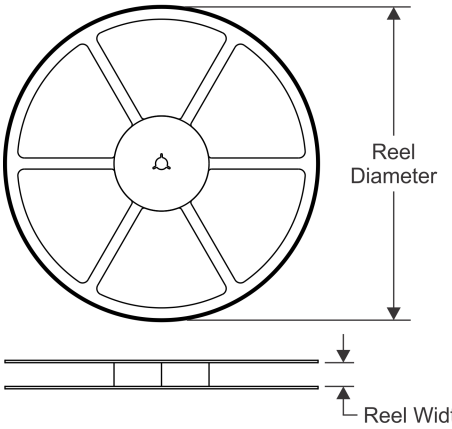
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

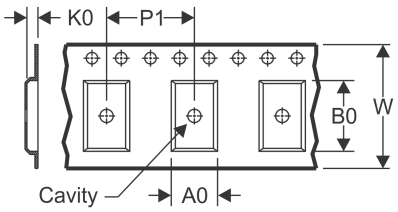
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

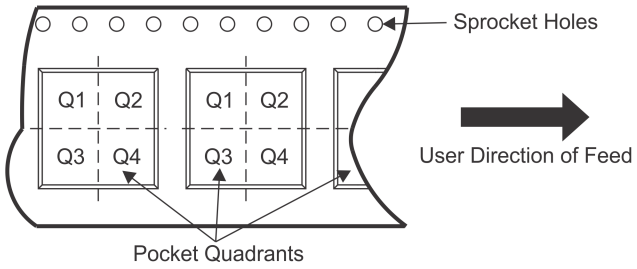


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

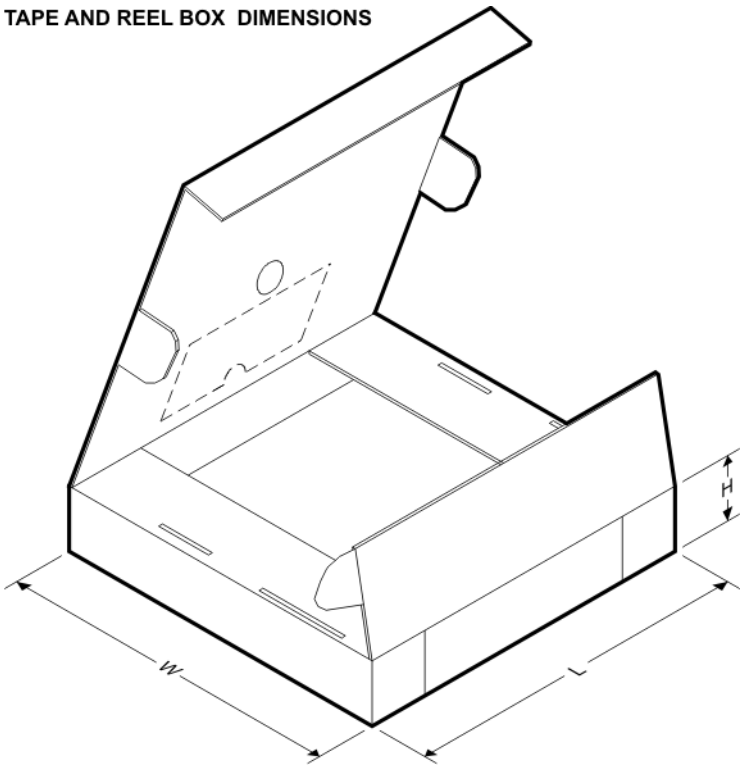
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62160DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62160DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62160DSGR	WSON	DSG	8	3000	180.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62160DSGT	WSON	DSG	8	250	180.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62161DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62161DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62162DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62163DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62163DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

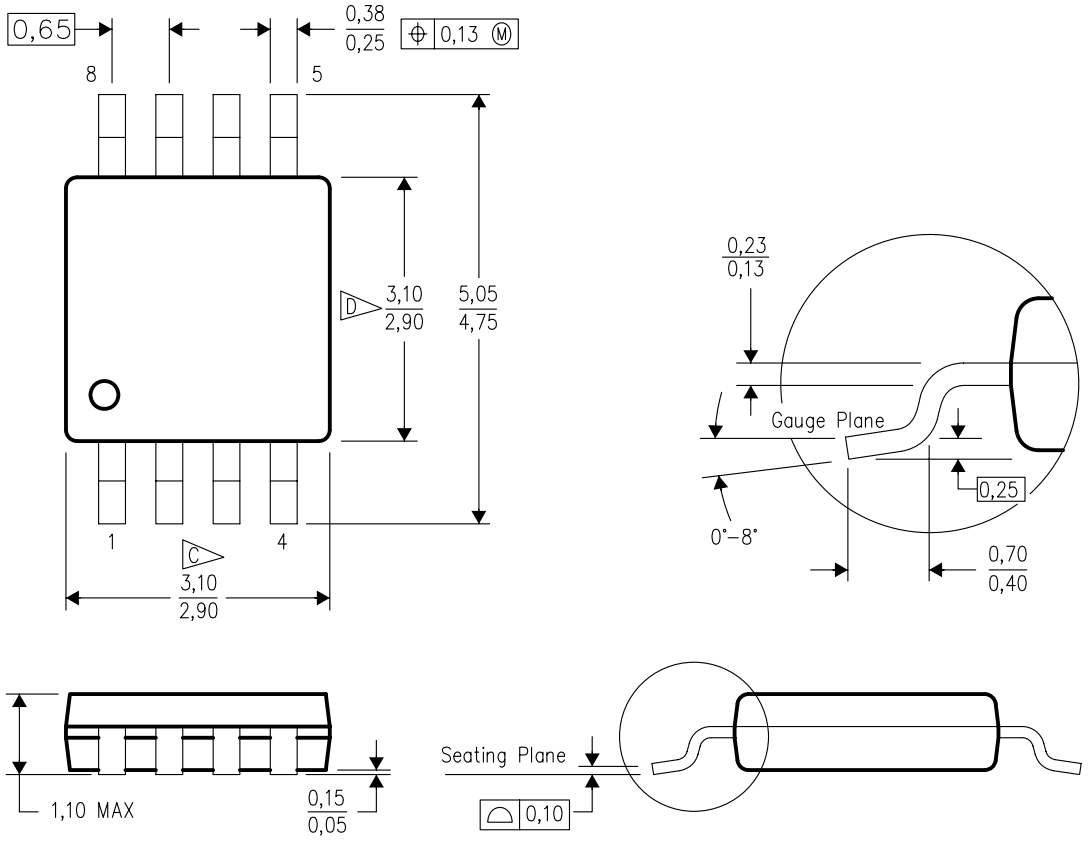
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62160DGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
TPS62160DGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
TPS62160DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62160DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62161DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62161DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62162DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62162DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62163DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62163DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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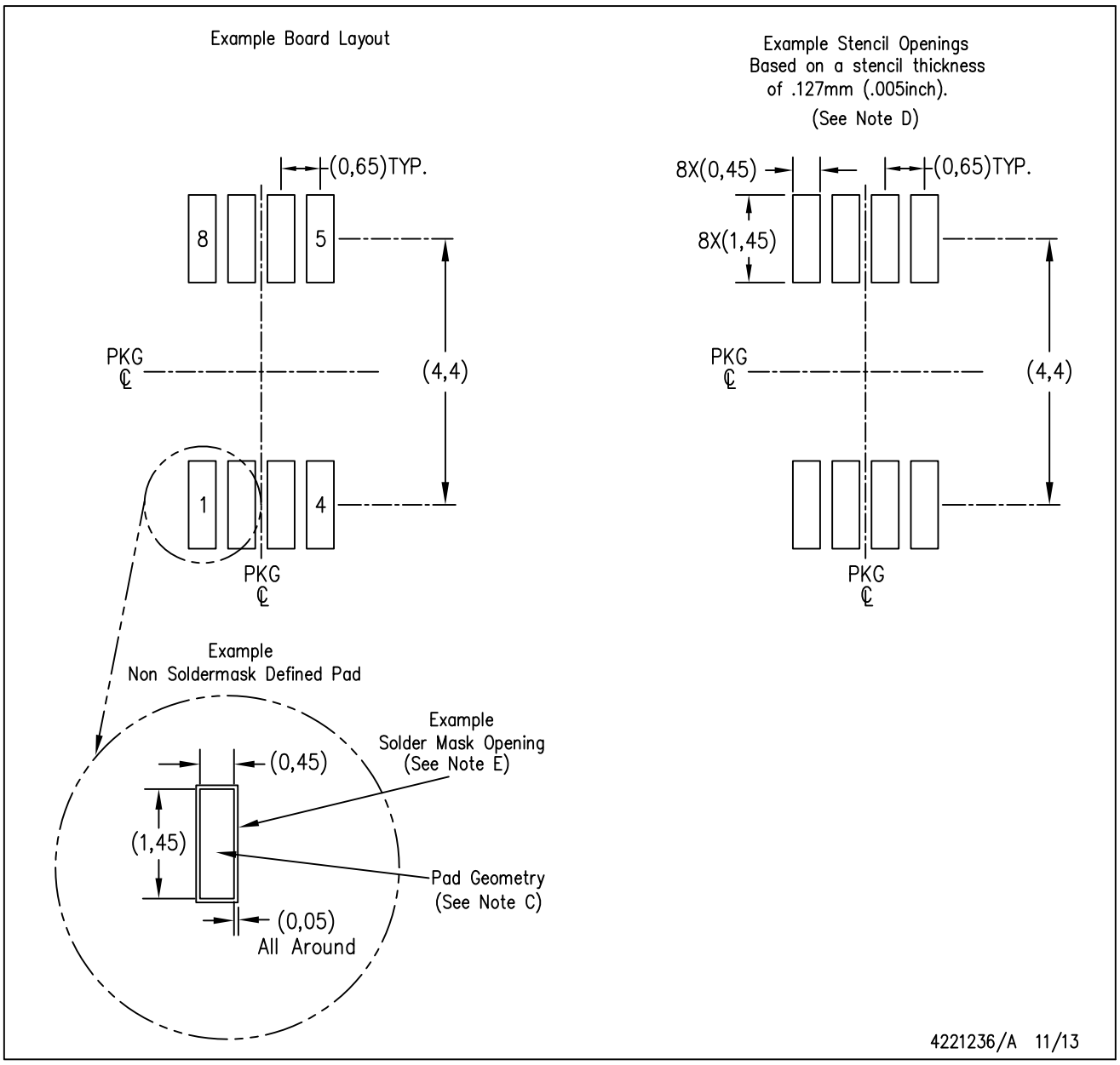
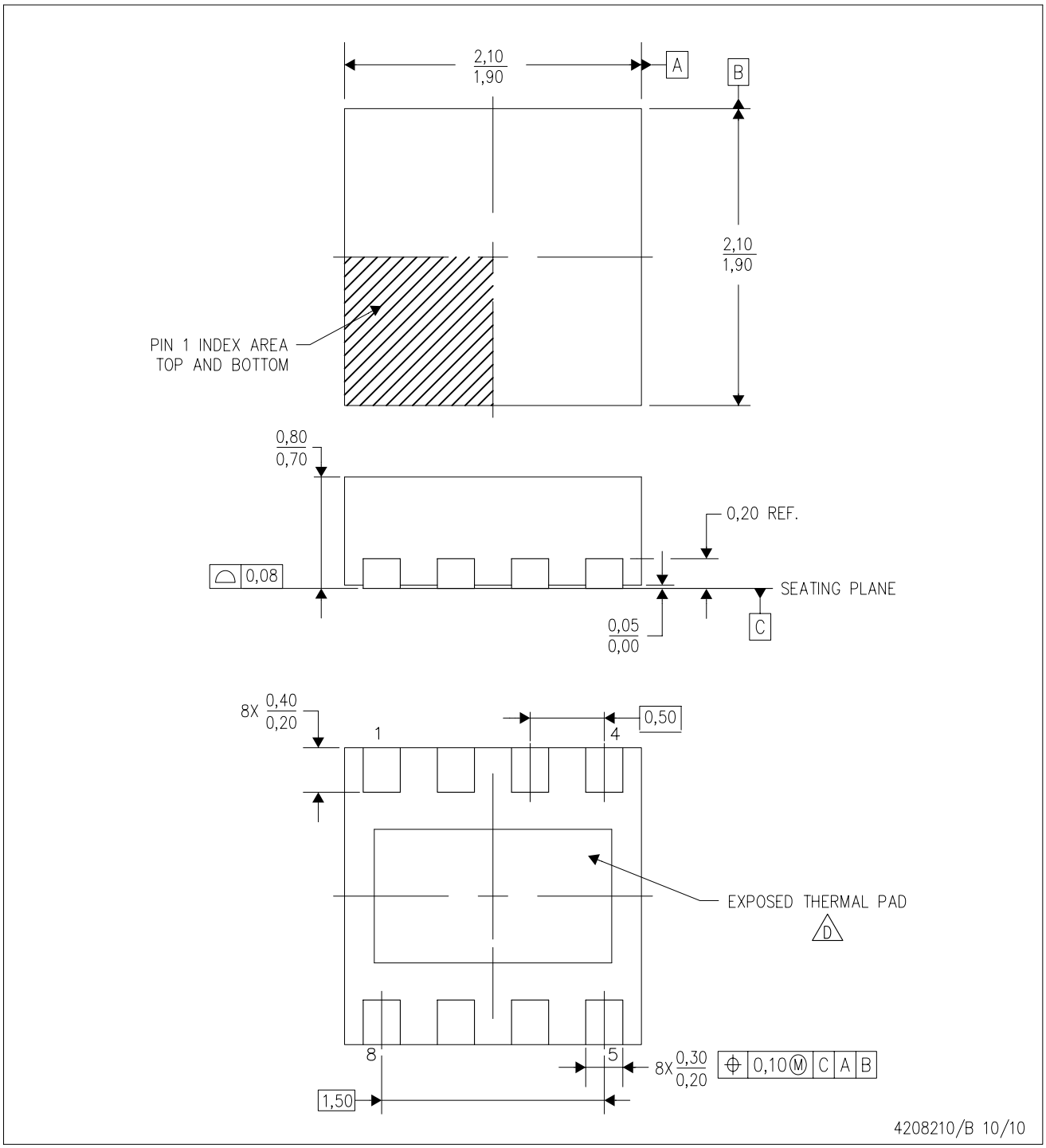
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

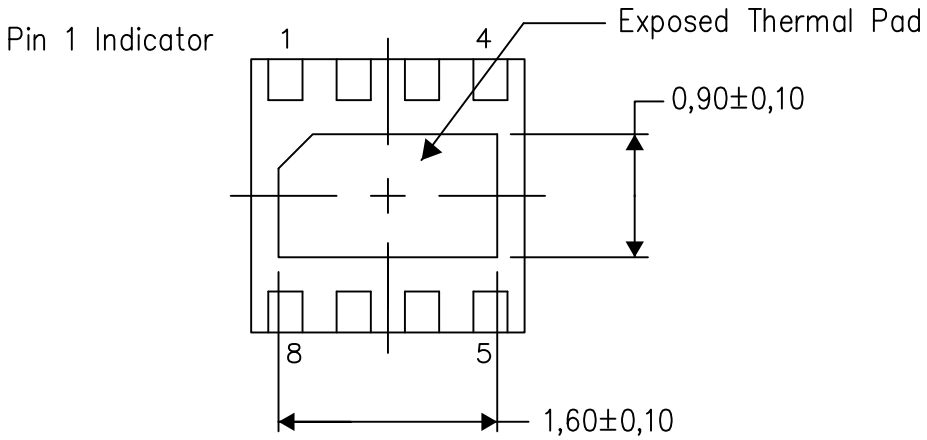
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



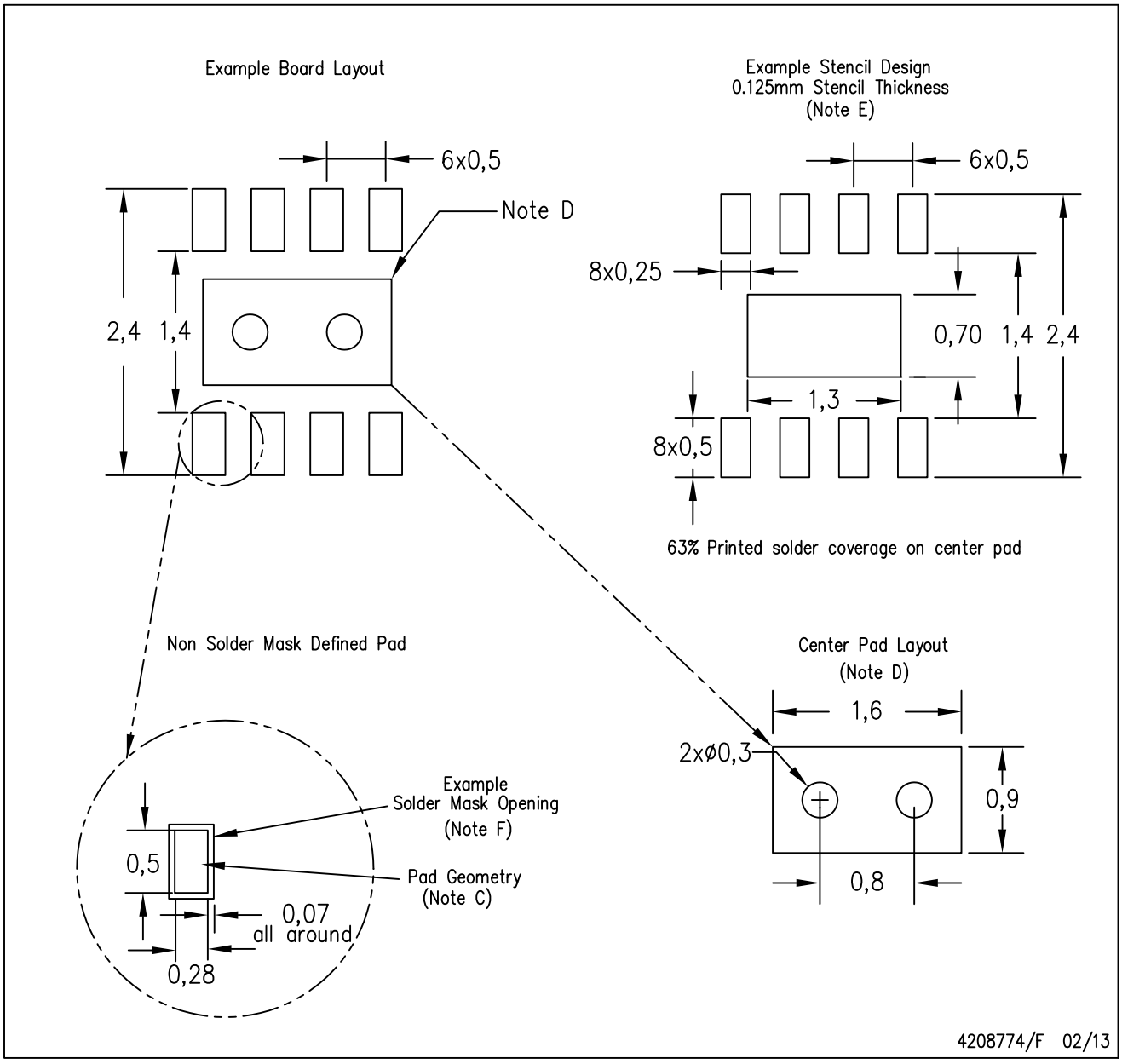
Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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