

## 54F432 Latch

Multi-Mode Buffered Latch, INV (3-State)

### Product Specification

### Military Logic Products

#### FEATURES

- Status flip-flop for interrupt commands
- Asynchronous or latched receiver mode
- Inverting
- 3-State outputs
- 300mil-wide Slim DIP package
- Functional equivalent to Intel 8212 except that 54F432 has inverting outputs

#### DESCRIPTION

The 54F432 has 8 data latches with 3-State output buffers. Also included is a status flip-flop for providing service-busy or request-interrupt commands. Separate Mode (M) and Select ( $S_0, S_1$ ) inputs allow data to be stored with the outputs enabled or disabled. The device can also be operated in a fully transparent mode.

This device is functionally equivalent to the Intel 8212 except that the 54F432 has inverting outputs.

#### ORDERING INFORMATION

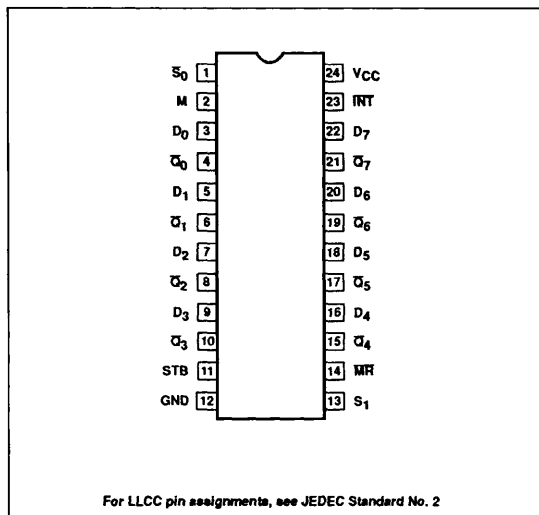
| DESCRIPTION             | ORDER CODE |
|-------------------------|------------|
| 24-Pin Ceramic DIP      | 54F432/BLA |
| 24-Pin Ceramic FlatPack | 54F432/BKA |
| 28-Pin Ceramic LLCC     | 54F432/B3A |

#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

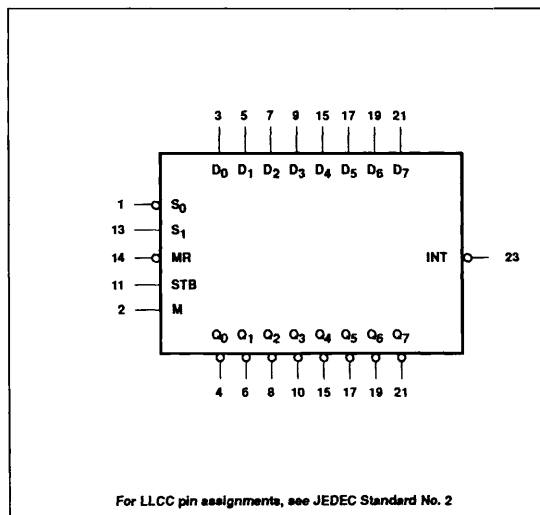
| PINS             | DESCRIPTION          | 54F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|------------------|----------------------|--------------------|---------------------|
| $D_0 - D_7$      | Data inputs          | 1.0/1.0            | 20 $\mu$ A/0.6mA    |
| $\bar{S}_0, S_1$ | Select inputs        | 1.0/1.0            | 20 $\mu$ A/0.6mA    |
| STB              | Strobe input         | 1.0/1.0            | 20 $\mu$ A/0.6mA    |
| M                | Mode Control input   | 1.0/1.0            | 20 $\mu$ A/0.6mA    |
| $\bar{MR}$       | Master Reset input   | 1.0/1.0            | 20 $\mu$ A/0.6mA    |
| INT              | Interrupt output     | 50/33              | 1.0mA/20mA          |
| $Q_0 - Q_7$      | Data latched outputs | 150/33             | 3.0mA/20mA          |

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

#### PIN CONFIGURATION



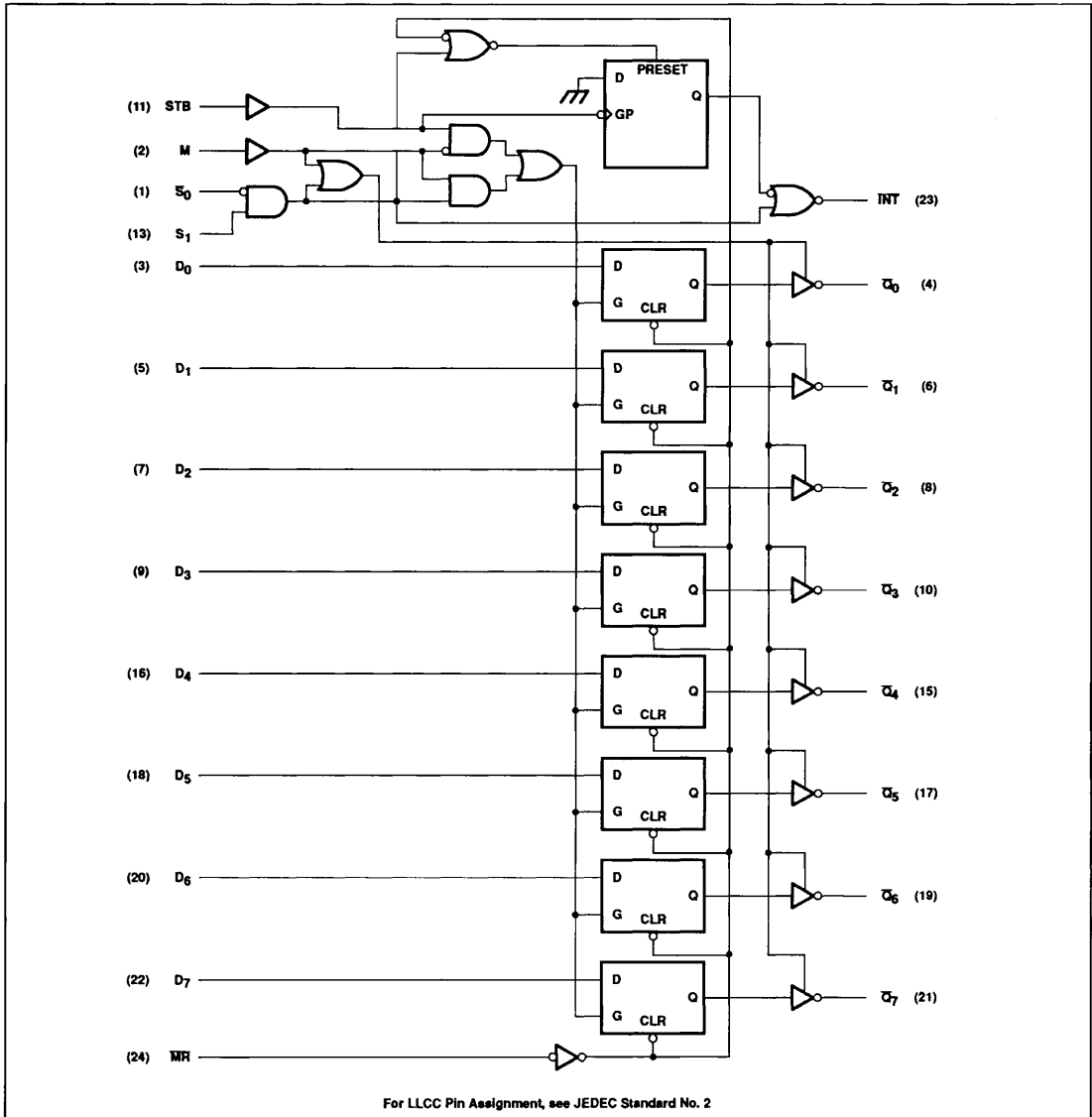
#### LOGIC SYMBOL



# Latch

# 54F432

## LOGIC DIAGRAM



# Latch

54F432

## FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates mode selection inputs and an edge-trigger status flip-flop designed specifically for implementing bus organized input/output ports. The 3-State data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands

The eight data latches are fully transparent when the internal gate enable input, G, is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select ( $S_0$  and  $S_1$ ), and the strobe (STB) inputs and during transparency each data output ( $Q_n$ )

follows its respective data input ( $D_n$ ). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M=L, the eight data latch inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most recently set up data.

In the output mode, M=H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ( $S_0$  and  $S_1$ ) inputs. See the Data Latches Function Table.

## STATUS FLIP-FLOP FUNCTION TABLE

| INPUTS |       |       |     | OUTPUT |
|--------|-------|-------|-----|--------|
| MR     | $S_0$ | $S_1$ | STB | INT    |
| L      | H     | X     | X   | H      |
| L      | X     | L     | X   | H      |
| H      | X     | X     | ↓   | L      |
| H      | L     | H     | X   | L      |

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↓ = High-to-Low clock transition

## DATA LATCHES FUNCTION TABLE

| INPUTS |   |       |       |     | DATA IN | DATA OUT    | OPERATING MODE |
|--------|---|-------|-------|-----|---------|-------------|----------------|
| MR     | M | $S_0$ | $S_1$ | STB |         |             |                |
| L      | H | H     | X     | X   | X       | H           | Clear          |
| L      | L | L     | H     | L   | X       | H           |                |
| X      | L | X     | L     | X   | X       | Z           | De-select      |
| X      | L | H     | X     | X   | X       | Z           |                |
| H      | H | H     | X     | X   | X       | $\bar{Q}_0$ | Hold           |
| H      | L | L     | H     | L   | X       | $Q_0$       |                |
| H      | H | L     | H     | X   | L       | H           | Data Bus       |
| H      | H | L     | H     | X   | H       | L           |                |
| H      | L | L     | H     | H   | L       | H           | Data Bus       |
| H      | L | L     | H     | H   | H       | L           |                |

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL    | PARAMETER  | RATING             | UNIT |
|-----------|--|--------------------|------|
| $V_{CC}$  | Supply voltage range                                 | -0.5 to +7.0       | V    |
| $V_I$     | Input voltage range                                  | -0.5 to +7.0       | V    |
| $I_I$     | Input current range                                  | -30 to +5          | mA   |
| $V_O$     | Voltage applied to output in High output state range | -0.5 to + $V_{CC}$ | V    |
| $I_O$     | Current applied to output in Low output state        | INT                | 40   |
|           |  | $Q_0 - Q_7$        | 40   |
| $T_{STG}$ | Storage temperature range                            | -65 to +150        | °C   |

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## RECOMMENDED OPERATING CONDITIONS

| SYMBOL          | PARAMETER                            | LIMITS                          |     |      | UNIT |
|-----------------|--------------------------------------|---------------------------------|-----|------|------|
|                 |                                      | Min                             | Nom | Max  |      |
| V <sub>CC</sub> | Supply voltage                       | 4.5                             | 5.0 | 5.5  | V    |
| V <sub>IH</sub> | High-level input voltage             | 2.0                             |     |      | V    |
| V <sub>IL</sub> | Low-level input voltage              |                                 |     | 0.8  | V    |
| I <sub>IK</sub> | Input clamp current                  |                                 |     | -18  | mA   |
| I <sub>OH</sub> | High-level output current            | I <sub>NT</sub>                 |     | -1.0 | mA   |
|                 |                                      | Q <sub>0</sub> , Q <sub>7</sub> |     | -3.0 | mA   |
| I <sub>OL</sub> | Low-level output current             | I <sub>NT</sub>                 |     | 20   | mA   |
|                 |                                      | Q <sub>0</sub> , Q <sub>7</sub> |     | 20   | mA   |
| T <sub>A</sub>  | Operating free-air temperature range | -55                             |     | +125 | °C   |

## DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL           | PARAMETER  | TEST CONDITIONS <sup>1</sup>  | LIMITS                 |                  |      | UNIT |
|------------------|--|---|------------------------|------------------|------|------|
|                  |  |   | Min                    | Typ <sup>2</sup> | Max  |      |
| V <sub>OH</sub>  | High-level output voltage                              | V <sub>CC</sub> = Min, V <sub>IL</sub> = Max,<br>V <sub>IH</sub> = Min                        | I <sub>OH</sub> = -1mA | 2.5              |      | V    |
|                  |  |   | I <sub>OH</sub> = -3mA | 2.4              |      | V    |
| V <sub>OL</sub>  | Low-level output voltage                               | V <sub>CC</sub> = Min, V <sub>IL</sub> = Max,<br>V <sub>IH</sub> = Min, I <sub>OL</sub> = Max |                        | .35              | .50  | V    |
| V <sub>IK</sub>  | Input clamp voltage                                    | V <sub>CC</sub> = Min, I <sub>I</sub> = I <sub>IK</sub>                                       |                        | -0.73            | -1.2 | V    |
| I <sub>I</sub>   | Input current at maximum input voltage                 | V <sub>CC</sub> = Max, V <sub>I</sub> = 7.0V  |                        |                  | 100  | μA   |
| I <sub>IH</sub>  | High-level input current                               | V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V  |                        |                  | 20   | μA   |
| I <sub>IL</sub>  | Low-level input current                                | V <sub>CC</sub> = Max, V <sub>I</sub> = 0.5V  |                        | -0.4             | -0.6 | mA   |
| I <sub>OZH</sub> | Off-state output current<br>High-level voltage applied | V <sub>CC</sub> = Max, V <sub>O</sub> = 2.7V  |                        |                  | 50   | μA   |
| I <sub>OZL</sub> | Off-state output current<br>Low-level voltage applied  | V <sub>CC</sub> = Max, V <sub>O</sub> = 0.5V  |                        |                  | -50  | μA   |
| I <sub>OS</sub>  | Short-circuit output current <sup>3</sup>              | V <sub>CC</sub> = Max, V <sub>O</sub> = 0.0V  | -60                    |                  | -150 | mA   |
| I <sub>CC</sub>  | Supply current (total)                                 | I <sub>CCH</sub>  |                        | 40               | 55   | mA   |
|                  |  | I <sub>CCL</sub>  | V <sub>CC</sub> = Max  | 50               | 70   | mA   |
|                  |  | I <sub>CCZ</sub>  |                        | 50               | 65   | mA   |

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**AC ELECTRICAL CHARACTERISTICS** (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

| SYMBOL                               | PARAMETER  | TEST CONDITIONS          | LIMITS  |             |              |   |              | UNIT     |
|--------------------------------------|--|--------------------------|---|-------------|--------------|---|--------------|----------|
|                                      |  |                          | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |             |              | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |              |          |
|                                      |  |                          | Min   | Typ         | Max          | Min   | Max          |          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>D <sub>n</sub> to Q <sub>n</sub>  | Waveform 2               | 4.5<br>2.5  | 7.5<br>4.5  | 10.5<br>7.0  | 4.0<br>2.5  | 13.0<br>6.0  | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>S <sub>0</sub> , S <sub>1</sub> or STB to Q <sub>n</sub>                    | Waveform 1, 2            | 8.5<br>6.0  | 14.0<br>9.5 | 17.0<br>13.0 | 8.0<br>5.5  | 24.0<br>14.0 | ns<br>ns |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>S <sub>0</sub> or S <sub>1</sub> to INT                                     | Waveform 1, 2            | 3.0<br>3.5  | 6.0<br>6.5  | 9.5<br>10.0  | 2.5<br>3.0  | 10.5<br>10.5 | ns<br>ns |
| t <sub>PLH</sub>                     | Propagation delay M <sup>2</sup> to Q <sub>n</sub>   | Waveform 2               | 8.0   | 12.0        | 16.0         | 7.5   | 18.5         | ns       |
| t <sub>PHL</sub>                     | Propagation delay STB to INT   | Waveform 2               | 7.0   | 10.0        | 13.5         | 6.5   | 14.5         | ns       |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable time to High or<br>Low level S <sub>0</sub> or S <sub>1</sub> to Q <sub>n</sub>    | Waveform 5<br>Waveform 6 | 6.0<br>6.0  | 9.0<br>11.0 | 12.5<br>14.0 | 5.5<br>5.5  | 15.5<br>15.0 | ns<br>ns |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable time from High<br>or Low level S <sub>0</sub> or S <sub>1</sub> to Q <sub>n</sub> | Waveform 5<br>Waveform 6 | 4.0<br>6.0  | 7.5<br>11.5 | 11.5<br>15.0 | 3.5<br>5.5  | 12.5<br>17.0 | ns<br>ns |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output Enable time to High or<br>Low level M to Q <sub>n</sub>                                   | Waveform 5<br>Waveform 6 | 5.0<br>6.0  | 7.5<br>8.0  | 11.0<br>11.5 | 4.5<br>5.5  | 12.0<br>13.0 | ns<br>ns |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output Disable time from High<br>or Low level M to Q <sub>n</sub>                                | Waveform 5<br>Waveform 6 | 3.5<br>6.0  | 6.0<br>10.0 | 9.5<br>13.0  | 3.0<br>5.5  | 10.5<br>15.0 | ns<br>ns |

**AC SETUP REQUIREMENTS**

| SYMBOL                                   | PARAMETER   | TEST CONDITIONS | LIMITS  |     |     |   |     | UNIT     |
|--|---|-----------------|---|-----|-----|---|-----|----------|
|  |   |                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |     | T <sub>A</sub> = -55°C to +125°C<br>V <sub>CC</sub> = +5.0V ± 10%<br>C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω |     |          |
|  |   |                 | Min   | Typ | Max | Min   | Max |          |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Setup time, High or Low<br>D <sub>n</sub> to S <sub>0</sub> , S <sub>1</sub> , STB or M | Waveform 3      | 0<br>0  |     |     | 1.0<br>1.0  |     | ns<br>ns |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, High or Low<br>D <sub>n</sub> to S <sub>0</sub> , S <sub>1</sub> , STB or M  | Waveform 3      | 9.0<br>8.0  |     |     | 9.5<br>9.5  |     | ns<br>ns |
| t <sub>w</sub> (H)<br>t <sub>w</sub> (L) | S <sub>0</sub> , S <sub>1</sub> or STB Pulse width<br>High or Low                       | Waveform 3      | 8.0<br>8.0  |     |     | 9.0<br>9.0  |     | ns<br>ns |
| t <sub>w</sub> (L)                       | M <sup>2</sup> Pulse width  | Waveform 4      | 8.0   |     |     | 9.0   |     | ns       |
| t <sub>rec</sub>                         | Recovery time   | Waveform 4      | 0   |     |     | 0   |     | ns       |

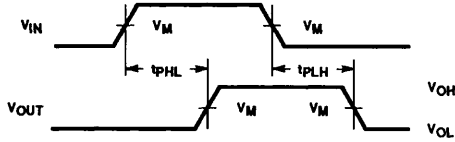
**NOTES:**

- For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

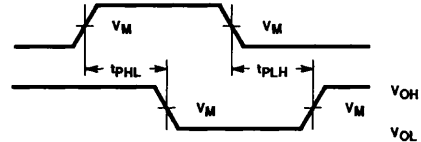
Latch

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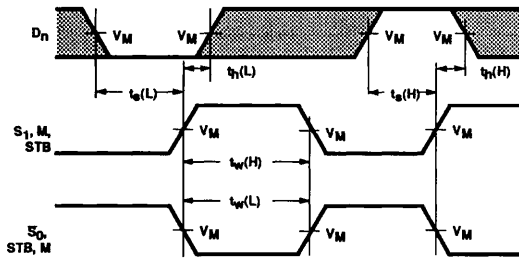
AC WAVEFORMS



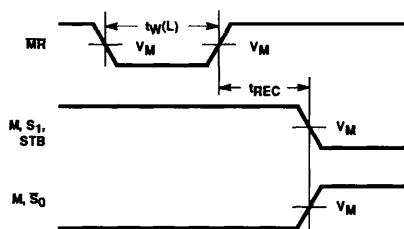
Waveform 1. Propagation Delay for Non-Inverting Outputs



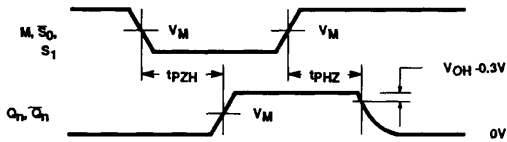
Waveform 2. Propagation Delay for Inverting Outputs



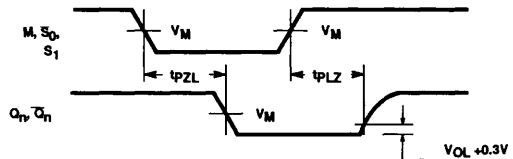
Waveform 3. Setup and Hold Times



Waveform 4. Recovery Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



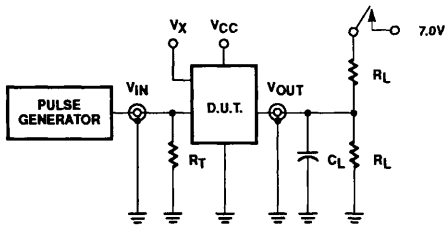
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE:  $V_M = 1.5V$   
The shaded areas indicate when the input is permitted to change for predictable output performance.

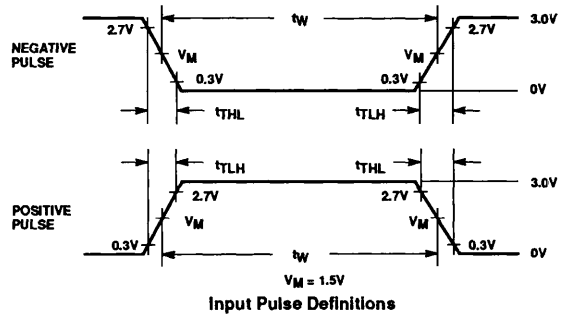
# Latch

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## TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



### SWITCH POSITION

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{pZL}$ | closed |
| All other | open   |

| INPUT PULSE CHARACTERISTICS |           |             |              |              |
|-----------------------------|-----------|-------------|--------------|--------------|
| Family                      | Rep. Rate | Pulse Width | $t_{TLH}$    | $t_{THL}$    |
| 54F                         | 1MHz      | 500ns       | $\leq 2.5ns$ | $\leq 2.5ns$ |

### DEFINITIONS:

- $R_L$  = Load Resistor; see AC Characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.
- $V_X$  = Unclocked pins must be held at:  $\leq 0.8V$ ;  $\geq 2.7V$  or open per Function Table.