

54F/74F821 10-Bit D-Type Flip-Flop

General Description

The 'F821 is a 10-bit D-type flip-flop with TRI-STATE® true outputs arranged in a broadside pinout. The 'F821 is functionally and pin compatible with the AMD's Am29821.

Features

- TRI-STATE Outputs
- Direct replacement for AMD's Am29821

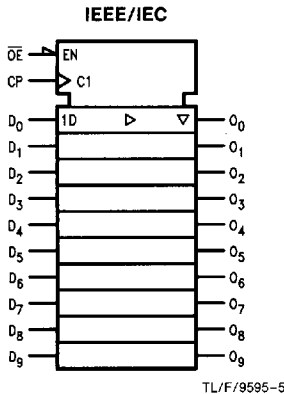
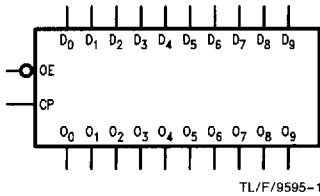
Ordering Code: See Section 11

Commercial	Military	Package Number	Package Description
74F821SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F821SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F821SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F821FM (Note 2)	W24C	24-Lead Cerpack
	54F821LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

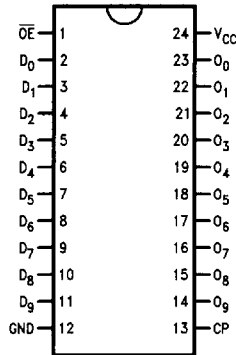
Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

Logic Symbols

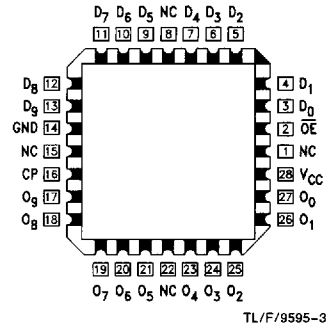


Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



Pin Assignment
for LCC



Unit Loading/Fan Out: See Section 2 for U.L. Definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D ₀ -D ₉	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}	Output Enable	1.0/1.0	20 μ A/ -0.6 mA
	TRI-STATE Input		
CP	Clock Input	1.0/1.0	20 μ A/ -0.6 mA
O ₀ -O ₉	TRI-STATE Outputs	150/40 (33.3)	-3.0 mA/24 mA (20 mA)

Functional Description

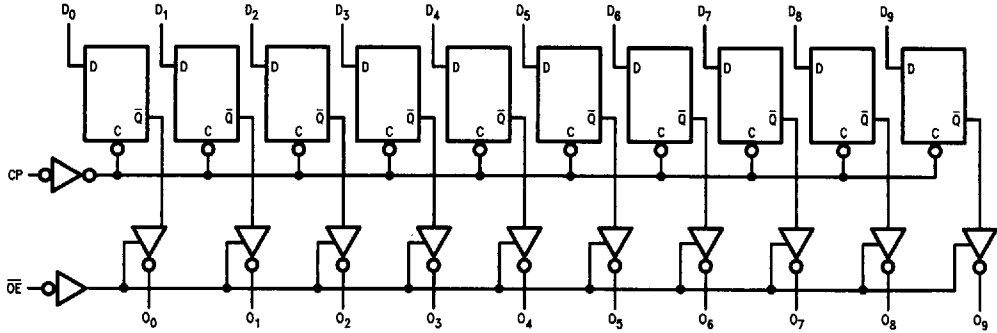
The 'F821 consists of ten D-type edge-triggered flip-flops. This device has TRI-STATE true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the \overline{OE} LOW the content of the flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs		Internal	Output	Function	
\overline{OE}	CP	\overline{Q}	O		
H	H	X	NC	Z	Hold
H	L	X	NC	Z	Hold
H	\nearrow	L	H	Z	Load
H	\nearrow	H	L	Z	Load
L	\nearrow	L	H	L	Data Available
L	\nearrow	H	L	H	Data Available
L	H	X	NC	NC	No Change in Data
L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
 H = HIGH Voltage Level
 X = Immaterial
 Z = High Impedance
 \nearrow = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



TL/F/9595-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			-50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current			-60	mA	Max	V _{OUT} = 0V
I _{CCZ}	Power Supply Current			78	100	mA	Max V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	100	150		60		70		MHz	2-1
t _{PLH}	Propagation Delay	2.0	6.4	9.5	2.0	10.5	2.0	10.5	ns	2-3
t _{PHL}	CP to O _n	2.0	6.2	9.5	2.0	10.5	2.0	10.5		
t _{PZH}	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns	2-5
t _{PZL}	\overline{OE} to O _n	2.0	6.3	10.5	2.0	13.0	2.0	11.5		
t _{PHZ}	Output Disable Time	1.5	3.4	7.0	1.0	7.5	1.5	7.5	ns	2-5
t _{PLZ}	\overline{OE} to O _n	1.5	3.5	7.0	1.0	7.5	1.5	7.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com			
		Min	Max	Min	Max	Min	Max		
t _s (H)	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns	2-6
t _s (L)	D _n to CP	2.5		4.0		3.0			
t _h (H)	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns	2-4
t _h (L)	D _n to CP	2.5		2.5		2.5			
t _w (H)	CP Pulse Width	5.0		6.0		6.0		ns	2-4
t _w (L)	HIGH or LOW	5.0		6.0		6.0			