

SN55LBC172 QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

SGLS084C – MARCH 1995 – REVISED JANUARY 2003

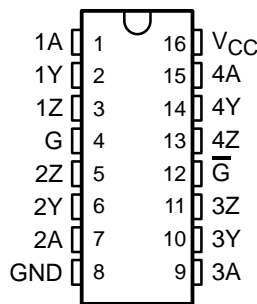
- Meets Standard EIA-485
- Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments
- Supports Data Rates up to and Exceeding Ten Million Transfers Per Second
- Common-Mode Output Voltage Range of -7 V to 12 V
- Positive- and Negative-Current Limiting
- Low Power Consumption . . . 1.5 mA Max (Output Disabled)

description

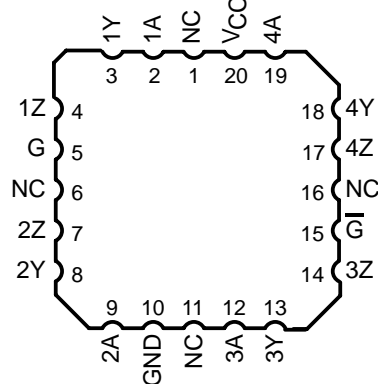
The SN55LBC172 is a monolithic quadruple differential line driver with 3-state outputs. This device is designed to meet the requirements of the Electronics Industry Association (EIA) standard RS-485. The SN55LBC172 is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry, making it suitable for party-line applications in noisy environments. The device is designed using the LinBiCMOS™ process, facilitating ultralow power consumption and inherent robustness.

The SN55LBC172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. This device offers optimum performance when used with the SN55LBC173M quadruple line receiver.

**J OR W PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC – No internal connection

ORDERING INFORMATION†

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	LCCC – FK	Tube	SNJ55LBC172FK	SNJ55LBC172FK
	CDIP – J	Tube	SNJ55LBC172J	SNJ55LBC172J
	CFP – W	Tube	SNJ55LBC172W	SNJ55LBC172W

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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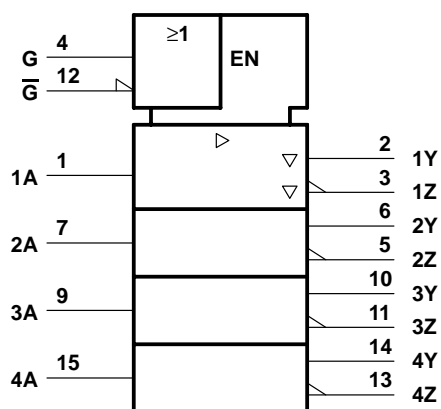
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FUNCTION TABLE
(each driver)

INPUT A	ENABLES		OUTPUTS	
	G	\bar{G}	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

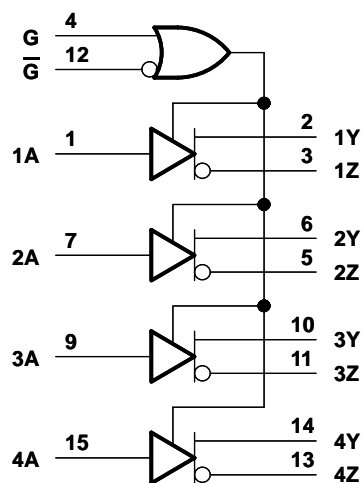
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the J or W package.

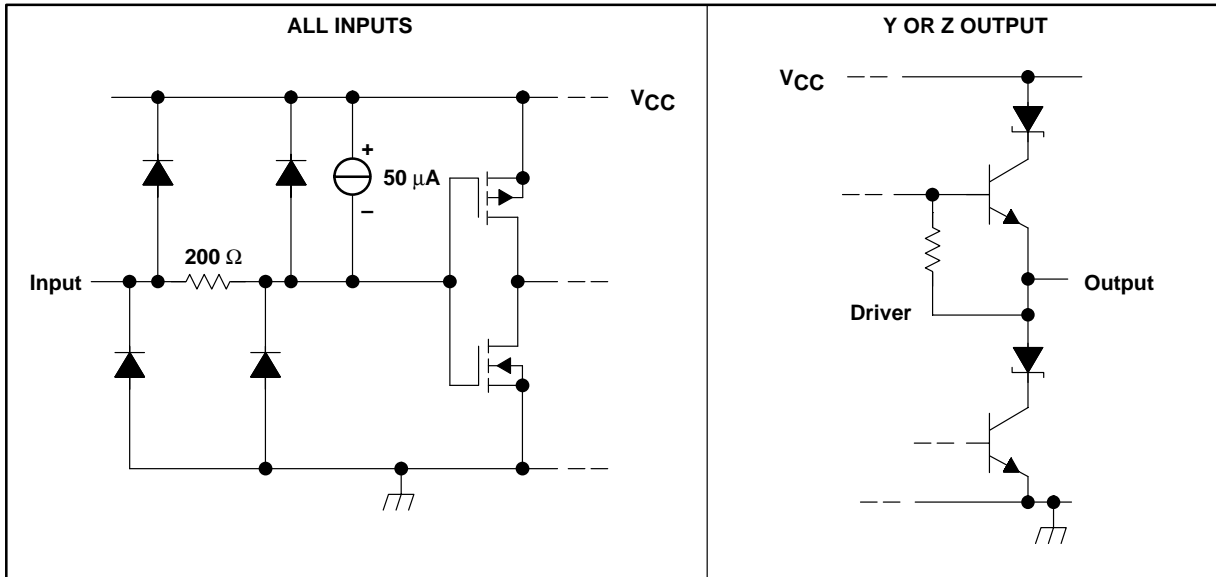
logic diagram (positive logic)



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schematic diagrams of inputs and outputs



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Output voltage range, V_O	–10 V to 15 V
Input voltage range, V_I	–0.3 V to 7 V
Continuous power dissipation	Internally limited‡
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A=125^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output voltage at any bus terminal (separately or common mode), V_O	Y or Z		12	V
			–7	
High-level output current, I_{OH}	Y or Z		–60	mA
Low-level output current, I_{OL}	Y or Z		60	mA
Continuous total power dissipation	See Dissipation Rating Table			
Operating free-air temperature, T_A	–55		125	°C



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$ V_{OD} $	Differential output voltage‡	$R_L = 54 \Omega$, See Figure 1	1.1	1.8	5	V
		$R_L = 60 \Omega$, See Figure 2	1.1	1.7	5	
$\Delta V_{OD} $	Change in magnitude of differential output voltage§				± 0.2	V
V_{OC}	Common-mode output voltage	$R_L = 54 \Omega$, See Figure 1			3 -1	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage§					± 0.2
I_O	Output current with power off	$V_{CC} = 0$, $V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7 \text{ V to } 12 \text{ V}$			± 100	μA
I_{IH}	High-level input current	$V_I = 2.4 \text{ V}$			-100	μA
I_{IL}	Low-level input current	$V_I = 0.4 \text{ V}$			-100	μA
I_{OS}	Short-circuit output current	$V_O = -7 \text{ V to } 12 \text{ V}$			± 250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		7	mA
			Outputs disabled		1.5	

† All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

‡ The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C . The lower output signal should be used to determine the maximum signal transmission distance.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

switching characteristics, $V_{CC} = 5 \text{ V}$

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54 \Omega$, See Figure 3	25°C	2	11	20	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$		2	40	
$t_{t(OD)}$	Differential output transition time	$R_L = 54 \Omega$, See Figure 3	25°C	10	15	25	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$		4	60	
t_{PZH}	Output enable time to high level	$R_L = 110 \Omega$, See Figure 4	25°C			30	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$			40	
t_{PZL}	Output enable time to low level	$R_L = 110 \Omega$, See Figure 5	25°C			30	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$			40	
t_{PHZ}	Output disable time from high level	$R_L = 110 \Omega$, See Figure 4	25°C			60	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$			115	
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$, See Figure 5	25°C			30	ns
			$-55^\circ\text{C to } 125^\circ\text{C}$			55	



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PARAMETER MEASUREMENT INFORMATION

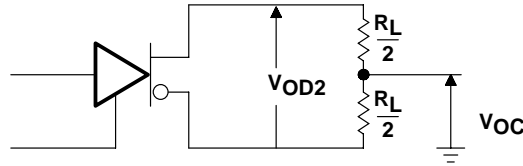


Figure 1. Differential and Common-Mode Output Voltages

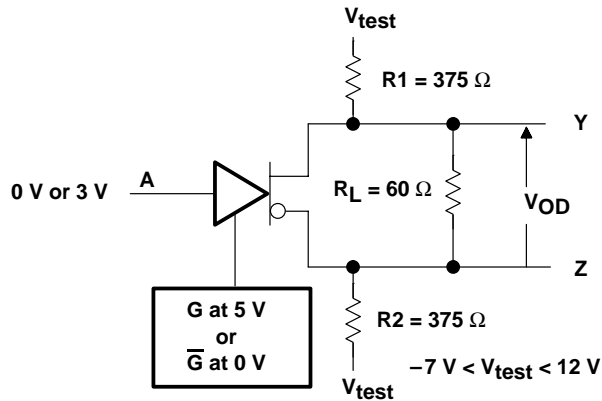
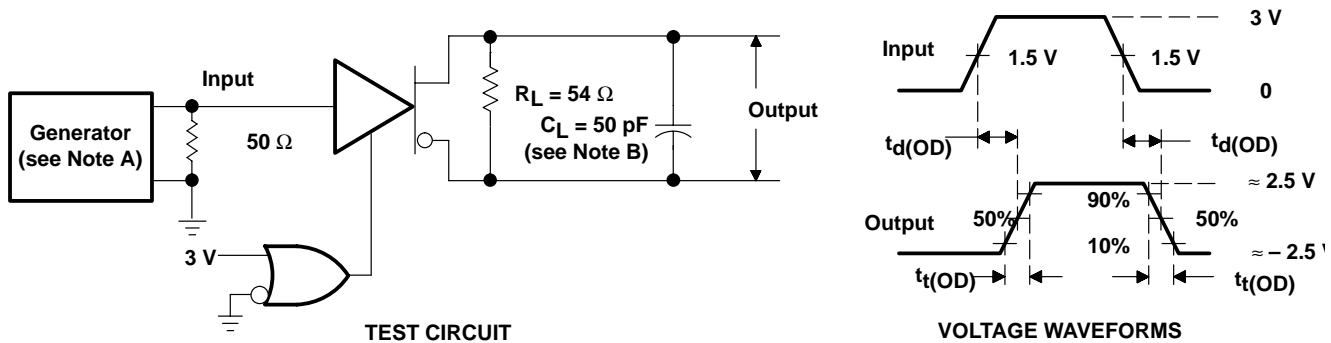


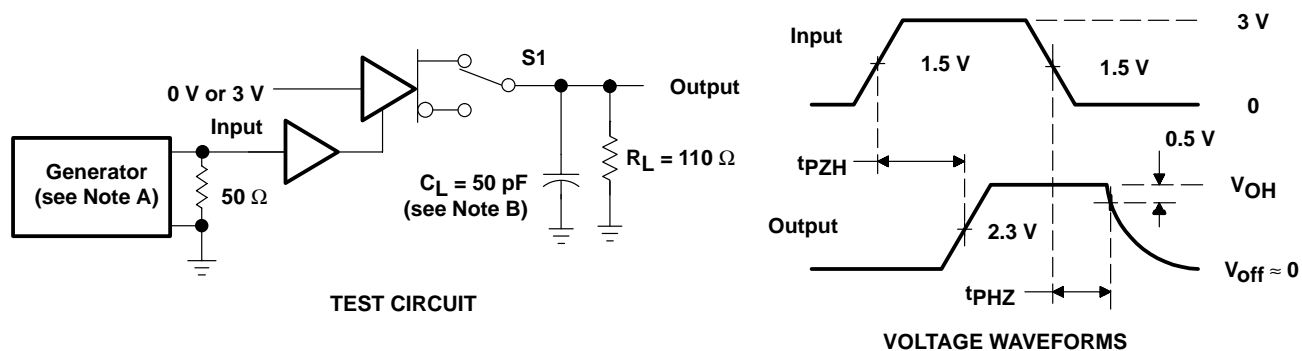
Figure 2. Driver V_{OD} Test Circuit



- NOTES: A. The input pulses are supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_O = 50 \Omega$.
- B. C_L includes probe and stray capacitance.

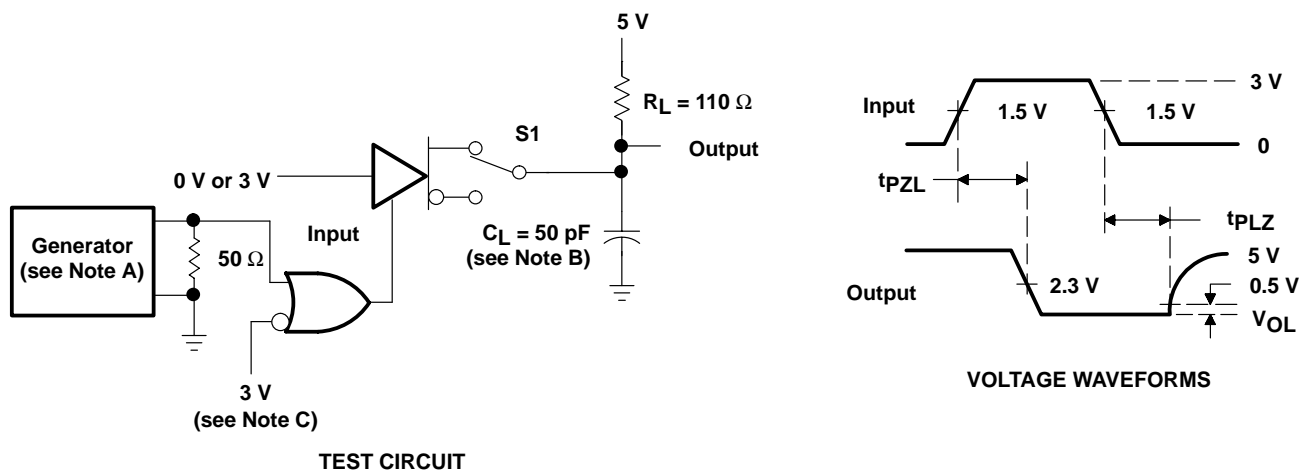
Figure 3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_0 = 50 \Omega$.
 B. C_L includes probe and stray capacitance.

Figure 4. t_{pZH} and t_{PHZ} Test Circuit and Voltage Waveforms



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, $t_r \leq$ 5 ns, $t_f \leq$ 5 ns, $Z_0 = 50 \Omega$.
 B. C_L includes probe and stray capacitance.
 C. To test the active-low enable \overline{G} , ground G and apply an inverted waveform to \overline{G} .

Figure 5. t_{pZL} and t_{PLZ} Test Circuit and Waveforms

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TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

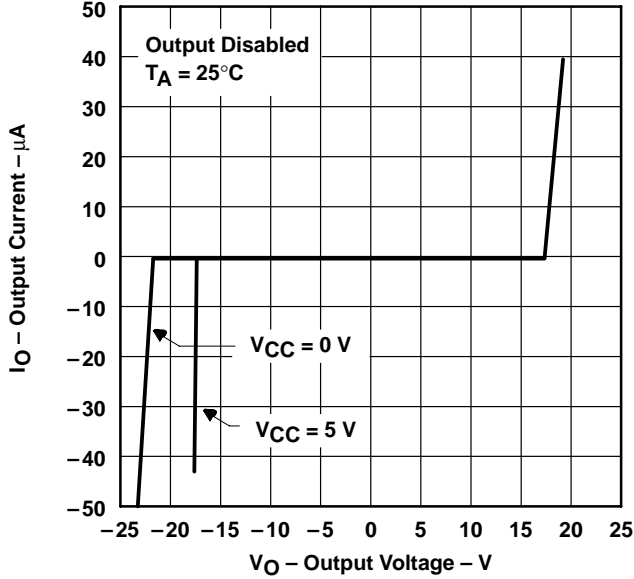


Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

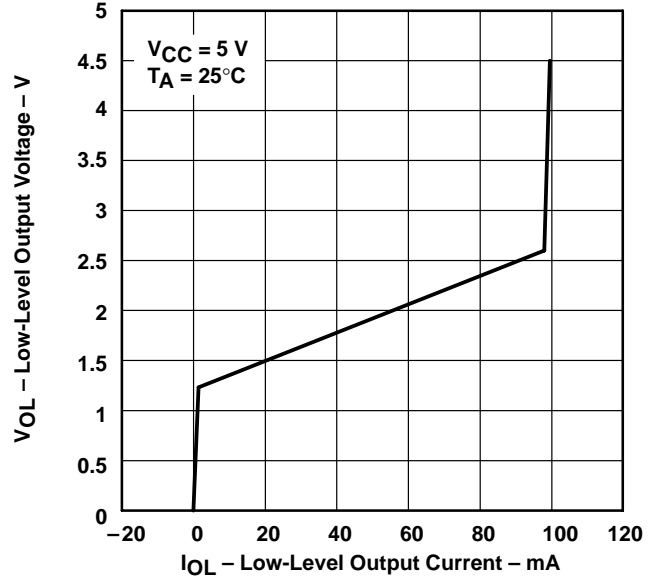


Figure 7

DRIVER
DIFFERENTIAL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

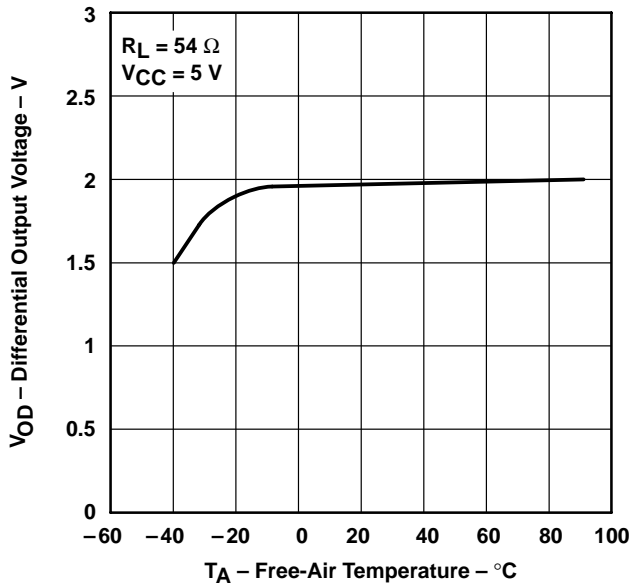


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

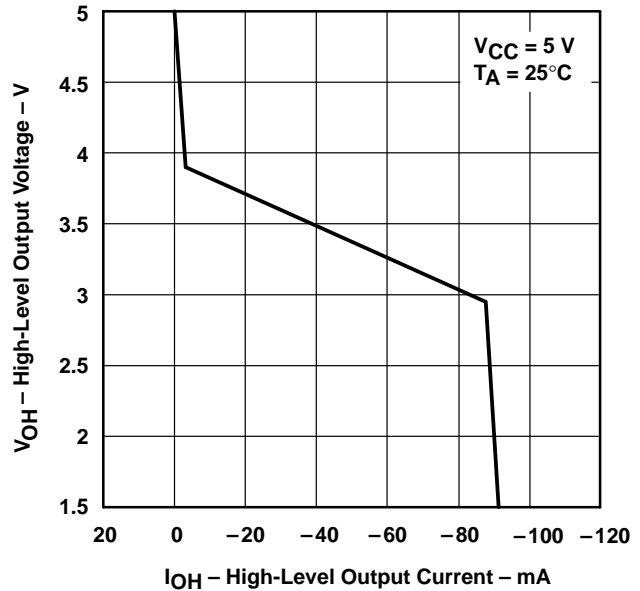


Figure 9



TYPICAL CHARACTERISTICS

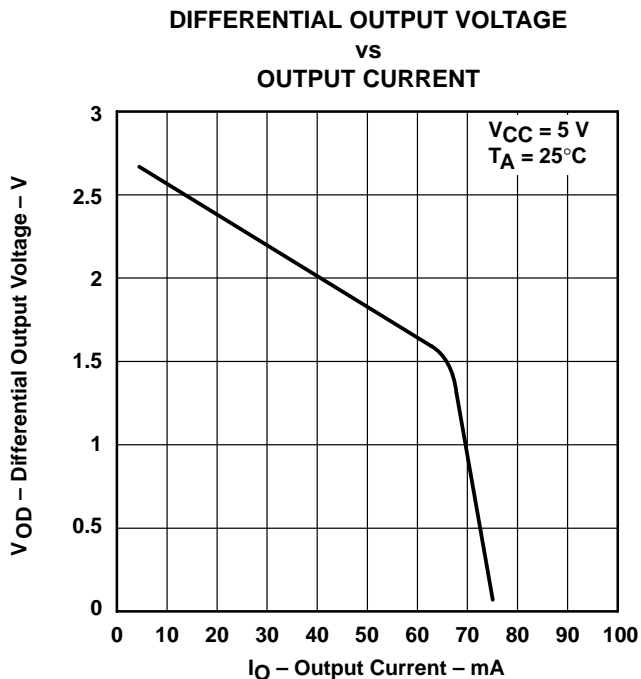


Figure 10

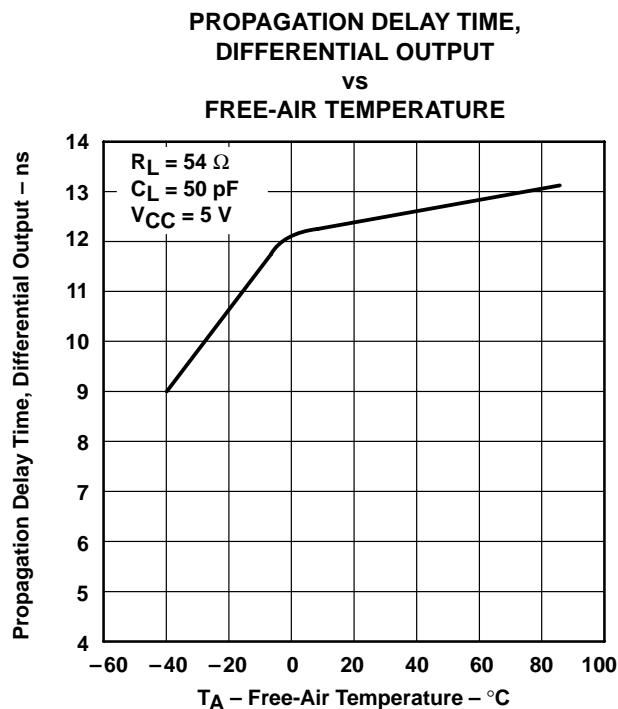


Figure 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9076503Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9076503Q2A SNJ55 LBC172FK	Samples
5962-9076503QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9076503QE A SNJ55LBC172J	Samples
5962-9076503QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9076503QF A SNJ55LBC172W	Samples
SNJ55LBC172FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9076503Q2A SNJ55 LBC172FK	Samples
SNJ55LBC172J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9076503QE A SNJ55LBC172J	Samples
SNJ55LBC172W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9076503QF A SNJ55LBC172W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN55LBC172 :

- Catalog : [SN75LBC172](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9076503Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9076503QFA	W	CFP	16	25	506.98	26.16	6220	NA
SNJ55LBC172FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC172W	W	CFP	16	25	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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