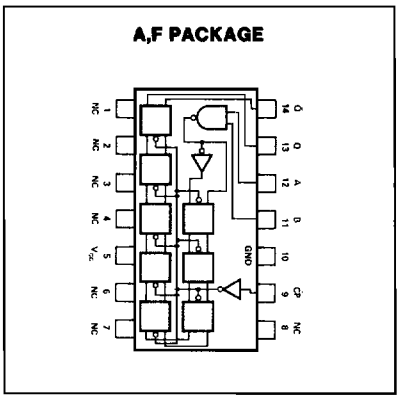
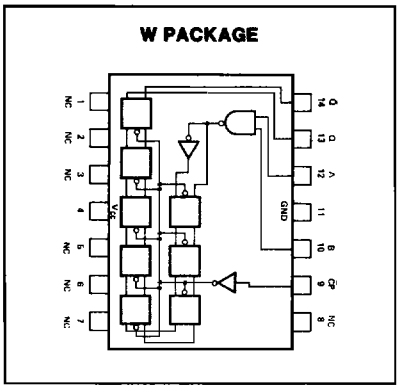
# 8-BIT SHIFT REGISTER — 54/7491

## SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

## PIN CONFIGURATION




## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| TEST CONDITIONS | 54/74 $C_L$=15pF $R_L$=400Ω | | | |
|---|---|---|---|---|
| **PARAMETER** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $f_{Max}$ | 10 | 18 | | MHz |
| Propagation delay time | | | | |
| $t_{PLH}$ Low-to-high | | 24 | 40 | ns |
| $t_{PHL}$ High-to-low | | 27 | 40 | |

Load circuit and typical waveforms are shown at the front of section.

## TRUTH TABLE

| $t_n$ | | $t_n$+8 |
|---|---|---|
| A | B | Q |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

NOTES:
1. $t_n$ = bit time before clock pulse.
2. $t_n$+8 = bit time after 8 clock pulse.

# DIVIDE-BY-TWELVE COUNTER — 54/7492

## SPEED/PACKAGE AVAILABILITY

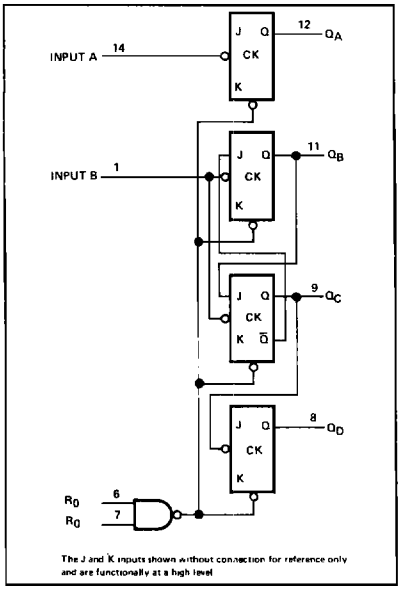
54 F,W 74 A,F

## DESCRIPTION

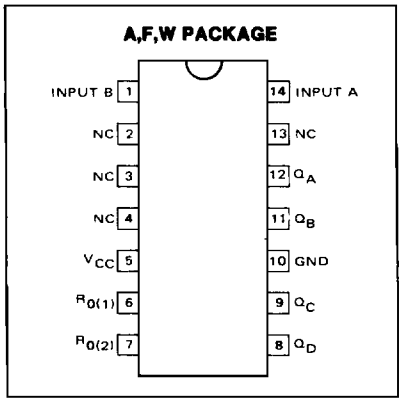
This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-six.

To use its maximum count length of this counter, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the function table.

## BLOCK DIAGRAM




## PIN CONFIGURATION



## SWITCHING CHARACTERISTICS $V_{CC}$ = 5V, $T_A$ = 25°C

| TEST CONDITIONS | | | | 54/74 $C_L$=15pF $R_L$=400 | | | 54/74LS $C_L$=15pF $R_L$=2k | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | | FROM INPUT | TO OUTPUT | MIN | TYP | MAX | MIN | TYP | MAX | UNIT |
| $f_{Count}$ | Count frequency | | | 10 | 18 | | | | | MHx |
| | | A | $Q_A$ | | | | 32 | 42 | | |
| | | B | $Q_B$ | | | | 16 | | | |
| $t_w$ | Width of pulse | A | Q | | | | 15 | | | ns |
| | | B | Q | | | | 30 | | | |
| | | Reset | Q | | | | 15 | | | |
| $t_{Setup}$ | Input setup time | | | | | | 25 | | | ns |
| Propagation delay time | | | | | | | | | | |
| $t_{PLH}$ | Low-to-high | Input Count Pulse | $Q_D$ | | 60 | 100 | | | | ns |
| $t_{PHL}$ | High-to-low | | | | 60 | 100 | | | | |
| $t_{PLH}$ | Low-to-high | A | $Q_A$ | | | | | 10 | 16 | |
| $t_{PHL}$ | High-to-low | | | | | | | 12 | 18 | |
| $t_{PLH}$ | Low-to-high | A | $Q_D$ | | | | | 32 | 48 | |
| $t_{PHL}$ | High-to-low | | | | | | | 34 | 50 | |
| $t_{PLH}$ | Low-to-high | B | $Q_B$ | | | | | 10 | 16 | |
| $t_{PHL}$ | High-to-low | | | | | | | 14 | 21 | |
| $t_{PLH}$ | Low-to-high | B | $Q_C$ | | | | | 10 | 16 | |
| $t_{PHL}$ | High-to-low | | | | | | | 14 | 21 | |
| $t_{PLH}$ | Low-to-high | B | $Q_D$ | | | | | 21 | 32 | |
| $t_{PHL}$ | High-to-low | | | | | | | 23 | 35 | |
| $t_{PHL}$ | High-to-low | Set-to-0 | Any | | | | | 26 | 40 | |

## RESET/COUNT FUNCTION TABLE

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

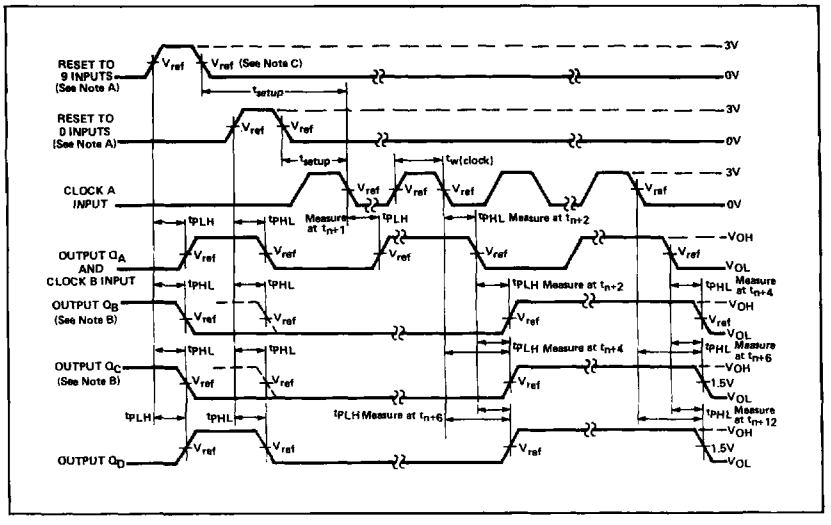
## COUNT SEQUENCE

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | H | L | L | L |
| 7 | H | L | L | H |
| 8 | H | L | H | L |
| 9 | H | L | H | H |
| 10 | H | H | L | L |
| 11 | H | H | L | H |

Output $Q_A$ is connected to Input B.

LOGIC

## PARAMETER MEASUREMENT INFORMATION




**VOLTAGE WAVEFORMS**

NOTES:
A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. $V_{ref}$ = 1.8 V.
Load circuit shown at front of book (for totem pole outputs).