

## 16-bit D-type transparent latch; (3-State)

74LVCH16373

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- Output drive capability 50Ω transmission lines @ 85°C

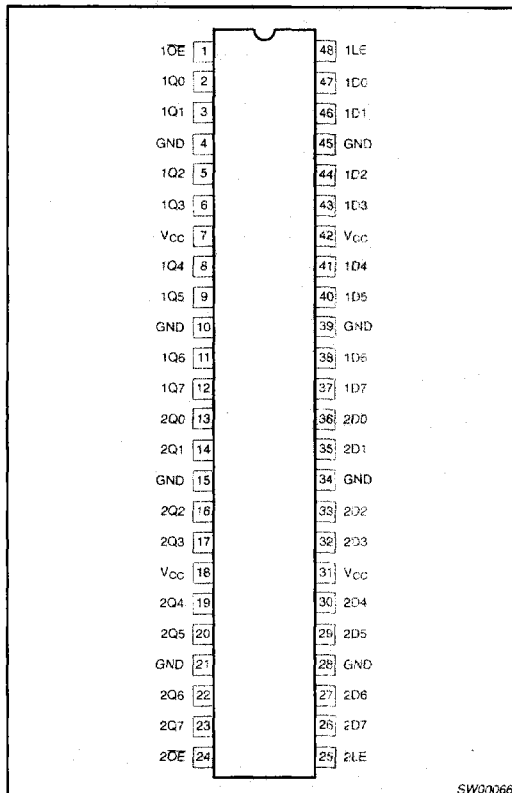
## DESCRIPTION

The 74LVCH16373 is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-State outputs for bus oriented applications. One latch enable (LE) input and one output enable (OE) are provided for each octal.

The 74LVCH16373 consists of 2 sections of eight D-type transparent latches with 3-State true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e., a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When OE is LOW, the contents of the eight latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches.

## PIN CONFIGURATION



SW00066

## ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 48-Pin Plastic SSOP Type III | -40°C to +85°C    | 74LVCH16373 DL        | VCH16373 DL   | SOT370-1   |
| 48-Pin Plastic TSSOP Type II | -40°C to +85°C    | 74LVCH16373 DGG       | VCH16373 DGG  | SOT362-1   |

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

| SYMBOL            | PARAMETER                                  | CONDITIONS                                    | TYPICAL    | UNIT |
|-------------------|--|---|------------|------|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>Dn to Qn;<br>LE to Qn | $C_L = 50\text{pF}$<br>$V_{CC} = 3.3\text{V}$ | 3.0<br>3.0 | ns   |
| $C_I$             | Input capacitance                          |   | 5.0        | pF   |
| $C_{PD}$          | Power dissipation capacitance per latch    | $V_I = \text{GND to } V_{CC}^1$               | 25         | pF   |

## NOTES:

<sup>1</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$

where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

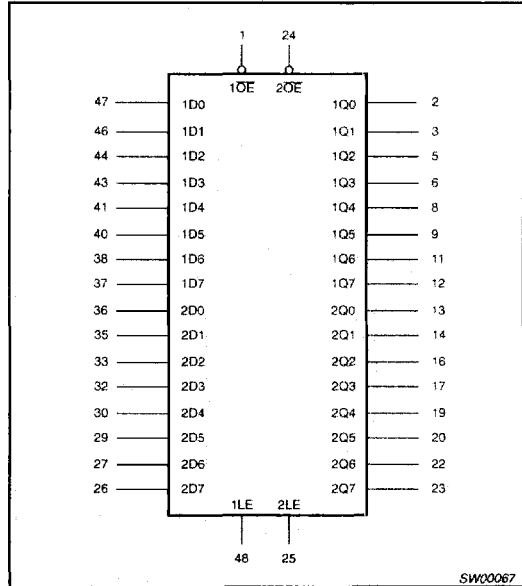
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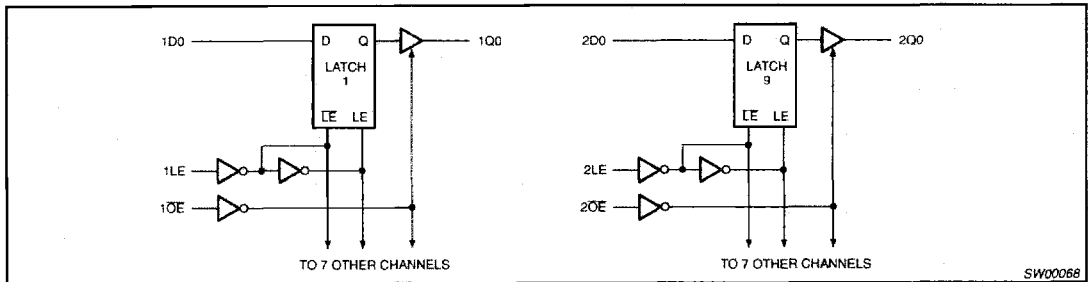
## PIN DESCRIPTION

| PIN NUMBER                     | SYMBOL          | NAME AND FUNCTION                |
|--------------------------------|-----------------|----------------------------------|
| 1                              | 1OE             | Output enable input (active LOW) |
| 2, 3, 5, 6, 8, 9, 11, 12       | 1Q0 to 1Q7      | Data inputs/outputs              |
| 4, 10, 15, 21, 28, 34, 39, 45  | GND             | Ground (0V)                      |
| 7, 18, 31, 42                  | V <sub>CC</sub> | Positive supply voltage          |
| 13, 14, 16, 17, 19, 20, 22, 23 | 2Q0 to 2Q7      | Data inputs/outputs              |
| 24                             | 2OE             | Output enable input (active LOW) |
| 25                             | 2LE             | Latch enable input (active HIGH) |
| 36, 35, 33, 32, 30, 29, 27, 26 | 2D0 to 2D7      | Data inputs                      |
| 47, 46, 44, 43, 41, 40, 38, 37 | 1D0 to 1D7      | Data inputs                      |
| 48                             | 1LE             | Latch enable input (active HIGH) |

## LOGIC SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE (per section of eight bits)

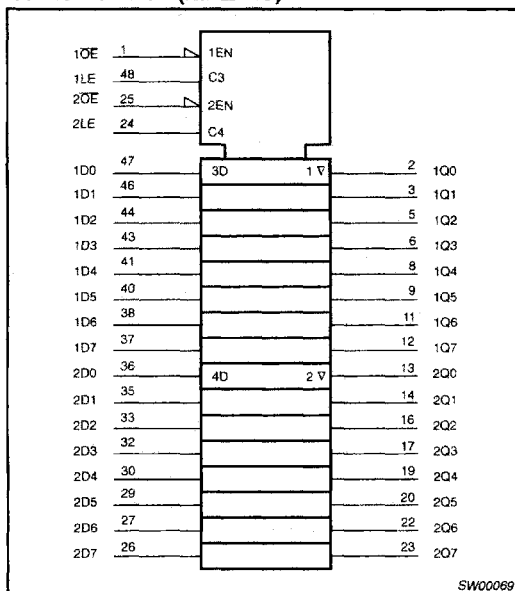
| OPERATING MODES                             | INPUTS |    |                | INTERNAL LATCHES | OUTPUTS  |
|---|--------|----|----------------|------------------|----------|
|   | OE     | LE | D <sub>n</sub> |                  | Q0 to Q7 |
| enable and read register (transparent mode) | L      | H  | L              | L                | L        |
|   | L      | H  | H              | H                | H        |
| latch and read register                     | L      | L  | l              | L                | L        |
|   | L      | L  | h              | H                | H        |
| latch register and disable outputs          | H      | L  | l              | L                | Z        |
|   | H      | L  | h              | H                | Z        |

H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
X = don't care  
Z = high impedance OFF-state

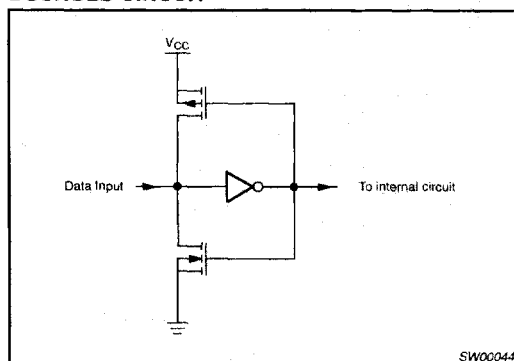
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# 74LVCH16373

## LOGIC SYMBOL (IEEE/IEC)



## BUSHOLD CIRCUIT



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0V)

| SYMBOL            | PARAMETER   | CONDITIONS   | RATING                 | UNIT |
|-------------------|---|--|------------------------|------|
| $V_{CC}$          | DC supply voltage   |  | -0.5 to +4.6           | V    |
| $I_{IK}$          | DC input diode current  | $V_I < 0$  | -50                    | mA   |
| $V_I$             | DC input voltage  | For control pins only <sup>3</sup>   | -0.5 to +5.5           | V    |
| $V_I$             | DC input voltage  | For data inputs only <sup>3</sup>  | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{OK}$          | DC output diode current   | $V_O > V_{CC}$ or $V_O < 0$  | $\pm 50$               | mA   |
| $V_{OUT}$         | DC output voltage   | Note 3   | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{OUT}$         | DC output source or sink current  | $V_O = 0$ to $V_{CC}$  | $\pm 50$               | mA   |
| $I_{GND}, I_{CC}$ | DC $V_{CC}$ or GND current  |  | $\pm 100$              | mA   |
| $T_{stg}$         | Storage temperature range   |  | -60 to +150            | °C   |
| $P_{TOT}$         | Power dissipation per package<br>-plastic medium-shrink SO (SSOP)<br>-plastic mini-pack (TSSOP) | For temperature range: -40 to +125 °C<br>above +55°C derate linearly with 11.3 mW/K<br>above +55°C derate linearly with 8 mW/K | 850<br>600             | mW   |

### NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL                          | PARAMETER  | CONDITIONS   | LIMITS |                 | UNIT |
|---------------------------------|--|--|--------|-----------------|------|
|                                 |  |  | MIN.   | MAX.            |      |
| V <sub>CC</sub>                 | DC supply voltage (for max. speed performance)   |  | 2.7    | 3.6             | V    |
| V <sub>CC</sub>                 | DC supply voltage (for low-voltage applications) |  | 1.2    | 3.6             | V    |
| V <sub>I</sub>                  | DC Input voltage range                           | Data inputs only   | 0      | V <sub>CC</sub> | V    |
| V <sub>I</sub>                  | DC Input voltage range                           | Data inputs only   | 0      | 5.5             | V    |
| V <sub>O</sub>                  | DC output voltage range                          |  | 0      | V <sub>CC</sub> | V    |
| T <sub>amb</sub>                | Operating free-air temperature range             |  | -40    | +85             | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input rise and fall times                        | V <sub>CC</sub> = 1.2 to 2.7V<br>V <sub>CC</sub> = 2.7 to 3.6V | 0<br>0 | 20<br>10        | ns/V |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL                             | PARAMETER  | TEST CONDITIONS   | LIMITS                       |                  |      | UNIT |
|------------------------------------|--|---|------------------------------|------------------|------|------|
|                                    |  |   | Temp = -40°C to +85°C        |                  |      |      |
|                                    |  |   | MIN                          | TYP <sup>1</sup> | MAX  |      |
| V <sub>IH</sub>                    | HIGH level input voltage                             | V <sub>CC</sub> = 1.2V  | V <sub>CC</sub>              |                  |      | V    |
|                                    |  | V <sub>CC</sub> = 2.7 to 3.6V   | 2.0                          |                  |      |      |
| V <sub>IL</sub>                    | LOW level input voltage                              | V <sub>CC</sub> = 1.2V  |                              |                  | GND  | V    |
|                                    |  | V <sub>CC</sub> = 2.7 to 3.6V   |                              |                  | 0.8  |      |
| V <sub>OH</sub>                    | HIGH level output voltage                            | V <sub>CC</sub> = 2.7; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA                   | V <sub>CC</sub> -0.5         |                  |      | V    |
|                                    |  | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100µA                 | V <sub>CC</sub> -0.2         | V <sub>CC</sub>  |      |      |
|                                    |  | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA                  | V <sub>CC</sub> -1.0         |                  |      |      |
| V <sub>OL</sub>                    | LOW level output voltage                             | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA                   |                              |                  | 0.4  | V    |
|                                    |  | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA                  |                              |                  | 0.2  |      |
|                                    |  | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA                   |                              |                  | 0.55 |      |
| I <sub>I</sub>                     | Input leakage current                                | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND  | Control pins                 | ±0.1             | ±5   | µA   |
|                                    |  | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND   | Data input pins <sup>2</sup> | ±0.1             | ±5   |      |
| I <sub>IHZ</sub> /I <sub>ILZ</sub> | Input current for common I/O pins                    | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND   |                              | ±0.1             | ±15  | µA   |
| I <sub>OZ</sub>                    | 3-State output OFF-state current                     | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND |                              | 0.1              | ±10  | µA   |
| I <sub>CC</sub>                    | Quiescent supply current                             | V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                                   |                              | 0.2              | 40   | µA   |
| ΔI <sub>CC</sub>                   | Additional quiescent supply current per control pin  | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0                           |                              | 5                | 500  | µA   |
| ΔI <sub>CC</sub>                   | Additional quiescent supply current per data I/O pin | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0                           |                              | 150              | 750  | µA   |
| IBHL                               | Bus hold LOW sustaining current                      | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2,3</sup>  | 75                           |                  |      | µA   |
| IBHH                               | Bus hold HIGH sustaining current                     | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2,3</sup>  | -75                          |                  |      | µA   |
| IBHLO                              | Bus hold LOW overdrive current                       | V <sub>CC</sub> = 3.6V <sup>2,4</sup>   | 450                          |                  |      | µA   |
| IBHHO                              | Bus hold HIGH overdrive current                      | V <sub>CC</sub> = 3.6V <sup>2,4</sup>   | -450                         |                  |      | µA   |

NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. For data inputs only, control inputs do not have a bus hold circuit.
3. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
4. The specified overdrive current at the data input forces the data input to the opposite logic input state.

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**AC CHARACTERISTICS**GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

| SYMBOL                 | PARAMETER                               | WAVEFORM | LIMITS                   |                  |     |                 |     |                 | UNIT |
|------------------------|---|----------|--------------------------|------------------|-----|-----------------|-----|-----------------|------|
|                        |   |          | $V_{CC} = 3.3V \pm 0.3V$ |                  |     | $V_{CC} = 2.7V$ |     | $V_{CC} = 1.2V$ |      |
|                        |   |          | MIN                      | TYP <sup>1</sup> | MAX | MIN             | MAX | MAX             |      |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation delay<br>Dn to Qn           | 1, 5     |                          | 3.1              | 5.5 |                 | 6.5 | 17.6            | ns   |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation delay<br>LE to Qn           | 2, 5     |                          | 3.1              | 5.5 |                 | 6.5 |                 | ns   |
| $t_{pZH}$<br>$t_{pZL}$ | 3-State output enable time<br>OE to Qn  | 3, 5     |                          | 3.6              | 6.5 |                 | 7.5 |                 | ns   |
| $t_{pHZ}$<br>$t_{pLZ}$ | 3-State output disable time<br>OE to Qn | 3, 5     |                          | 3.4              | 6.0 |                 | 6.5 |                 | ns   |
| $t_W$                  | LE pulse width HIGH                     | 2        | 4.0                      |                  |     | 5.0             |     |                 | ns   |
| $t_{su}$               | Set-up time Dn to LE                    | 4        | 2.0                      |                  |     | 2.5             |     |                 | ns   |
| $t_h$                  | hold time Dn to LE                      | 4        | 1.5                      |                  |     | 2.0             |     |                 | ns   |

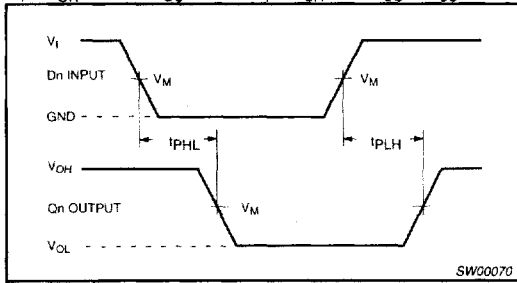
**NOTE:**1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

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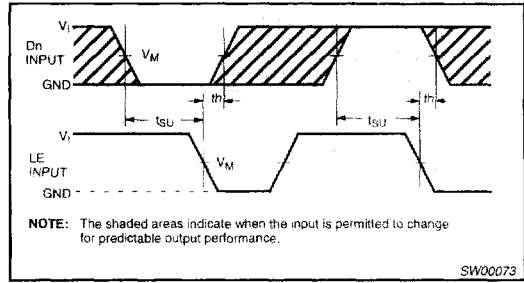
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## AC WAVEFORMS

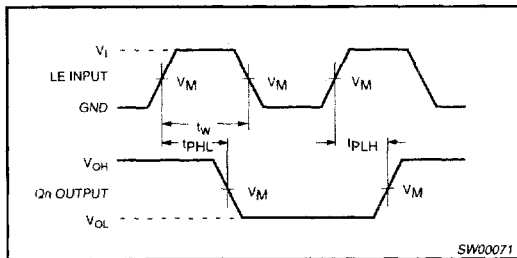
$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$ ;  $V_M = 0.5 V_{CC}$  at  $V_{CC} < 2.7V$ .  
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_X = V_{OL} + 0.1 V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$ ;  $V_Y = V_{OH} - 0.1 V_{CC}$  at  $V_{CC} < 2.7V$



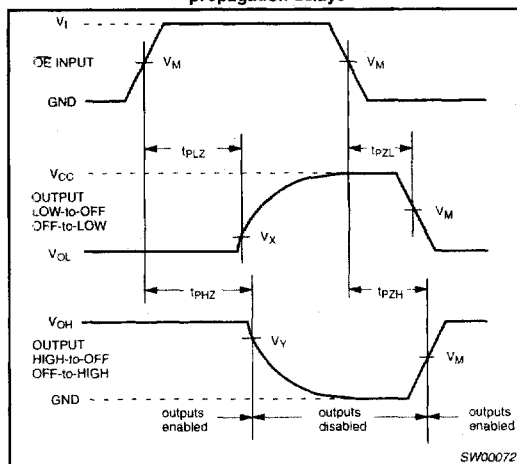
Waveform 1. Waveforms showing the input (Dn) to output (Qn) propagation delays



Waveform 4. Waveforms showing the data set-up and hold times for the Dn input to the LE input

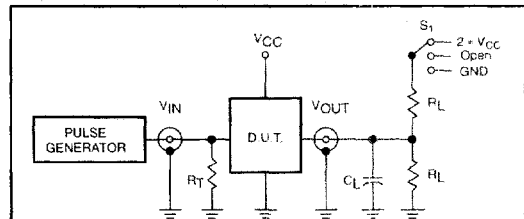


Waveform 2. Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Qn) propagation delays



Waveform 3. Waveforms showing the 3-State enable and disable times

## TEST CIRCUIT



Test Circuit for 3-State Outputs

### SWITCH POSITION

| TEST              | SWITCH       |
|-------------------|--------------|
| $t_{PLH}/t_{PHL}$ | Open         |
| $t_{PLZ}/t_{PZL}$ | $2 * V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND          |

| $V_{CC}$     | $V_I$    |
|--------------|----------|
| $< 2.7V$     | $V_{CC}$ |
| $2.7 - 3.6V$ | $2.7V$   |

### DEFINITIONS

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times