

74VHC573 • 74VHCT573 Octal D-Type Latch with TRI-STATE® Outputs

General Description

The VHC/VHCT573 is an advanced high speed CMOS octal latch with TRI-STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type latch is controlled by a latch enable input (LE) and an Output Enable input (\overline{OE}). When the \overline{OE} input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0V–7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Noise Immunity:
 - VHC: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
 - VHCT: $V_{IH} = 2.0V$, $V_{IL} = 0.8V$
- Power Down Protection:
 - VHC = inputs only
 - VHCT = inputs and outputs
- Low Noise:
 - VHC $V_{OLP} = 0.6V$ (typ)
 - VHCT $V_{OLP} = 0.8V$ (typ)
- Low Power Dissipation:
 - $I_{CC} = 4 \mu A$ (Max) @ $T_A = 25^\circ C$
- Balanced propagation delays: $t_{PLH} \cong t_{PHL}$
- Pin and function compatible with 74HC/HCT573

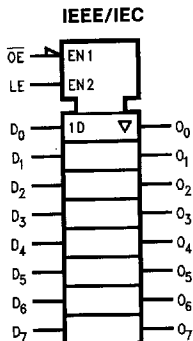
Note: *VHCT specifications are preliminary

Ordering Code: See Section 6

Commercial	Package Number	Package Description
74VHC573M	M20B	20-Lead Molded JEDEC SOIC
74VHC573SJ	M20D	20-Lead Molded EIAJ SOIC
74VHC573MSC	MSC20	20-Lead Molded EIAJ Type I SSOP
74VHC573MTC	MTC20	20-Lead Molded JEDEC Type I TSSOP
74VHC573N	N20A	20-Lead Molded DIP
74VHCT573M	M20B	20-Lead Molded JEDEC SOIC
74VHCT573SJ	M20D	20-Lead Molded EIAJ SOIC
74VHCT573MTC	MTC20	20-Lead Molded JEDEC Type I TSSOP
74VHCT573N	N20A	20-Lead Molded DIP

Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

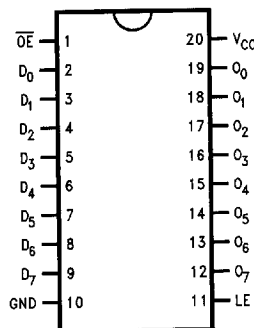
Logic Symbol



TL/F/11563-1

Connection Diagram

Pin Assignment for
DIP, SSOP, TSSOP and SOIC



TL/F/11563-2

Pin Names	Description
D_0 – D_7	Data Inputs
LE	Latch Enable Input
\overline{OE}	TRI-STATE Output Enable Input
O_0 – O_7	TRI-STATE Outputs

Functional Description

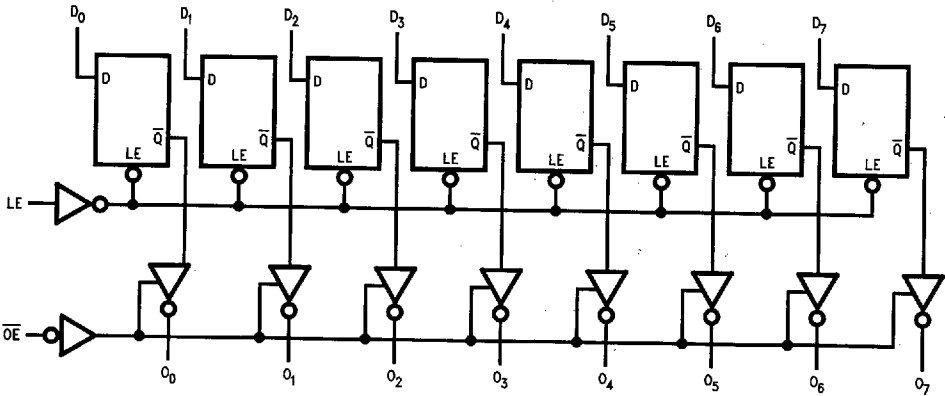
The VHC/VHCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs, a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
\overline{OE}	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Logic Diagram



TL/F/11563-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to +7.0V
DC Output Voltage (V_{OUT})	-0.5V to $V_{CC} + 0.5V$
VHC	-0.5V to +7.0V
VHCT*	-0.5V to +7.0V
Input Diode Current (I_{IK})	-20 mA
Output Diode Current	
VHC	± 20 mA
VHCT	-20 mA
DC Output Current (I_{OUT})	± 25 mA
DC V_{CC} /GND Current (I_{CC})	± 75 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Lead Temperature (T_L)	260°C
(Soldering, 10 seconds)	

* $V_{OUT} > V_{CC}$ only if output is in H or Z state

Note 1: *Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.*

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
VHC	4.5V to +5.5V
VHCT	0V to +5.5V
Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	-40°C to +85°C
74VHC/VHCT	
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$ (VHC only)	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices

Symbol	Parameter	V_{CC} (V)	74VHC			74VHC		Units	Conditions	
			$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to +85°C				
			Min	Typ	Max	Min	Max			
V_{IH}	High Level Input Voltage	2.0 3.0-5.5	1.50 0.7 V_{CC}			1.50 0.7 V_{CC}		V		
V_{IL}	Low Level Input Voltage	2.0 3.0-5.5			0.50 0.3 V_{CC}	0.50 0.3 V_{CC}		V		
V_{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V		$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
		3.0	2.58			2.48				
V_{OL}	Low Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
		3.0			0.36		0.44			
		4.5			0.36		0.44	V		
		3.0					0.44			
I_{OZ}	TRI-STATE Output Off-State Current	5.5			± 0.25		± 2.5	μA	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	
I_{IN}	Input Leakage Current	0-5.5			± 0.1		± 1.0	μA	$V_{IN} = 5.5V$ or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	μA	$V_{IN} = V_{CC}$ or GND	

DC Characteristics for 'VHC Family Devices: See Section 2 for Waveforms (Continued)

Symbol	Parameter	V _{CC} (V)	74VHC		Units	Conditions	Fig. No.
			T _A = 25°C				
			Typ	Limits			
**V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	0.9	1.2	V	C _L = 50 pF	2-11, 12
**V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-0.8	-1.0	V	C _L = 50 pF	2-11, 12
**V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0		3.5	V	C _L = 50 pF	2-11, 12
**V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		1.5	V	C _L = 50 pF	2-11, 12

**Parameter guaranteed by design.

DC Characteristics for 'VHCT Family Devices (Preliminary)

Symbol	Parameter	V _{CC} (V)	74VHCT			74VHCT		Units	Conditions
			T _A = 25°C			T _A = -40°C to +85°C			
			Min	Typ	Max	Min	Max		
V _{IH}	High Level Input Voltage	4.5 5.5	2.0 2.0			2.0 2.0	V		
V _{IL}	Low Level Input Voltage	4.5 5.5			0.8 0.8	0.8 0.8	V		
V _{OH}	High Level Output Voltage	4.5	3.15	3.65		3.15	V	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA I _{OH} = -8 mA	
		4.5	2.5			2.4	V		
V _{OL}	Low Level Output Voltage	4.5		0.0	0.1	0.1	V	V _{IN} = V _{IH} or V _{IL} I _{OL} = -50 μA I _{OL} = 8 mA	
		4.5			0.36	0.44	V		
I _{OZ}	TRI-STATE Output Off-State Current	5.5			±0.25	±2.5	μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	0-5.5			±0.1	±1.0	μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5			4.0	40.0	μA	V _{IN} = V _{CC} or GND	
I _{CC(T)}	Maximum I _{CC} /Input	5.5			1.35	1.50	mA	V _{IN} = 3.4V Other Inputs = V _{CC} or GND	
I _{OPD}	Output Leakage Current (Power Down State)	0.0			±0.5	±0.5	μA	V _{OUT} = 5.5V	

DC Characteristics for 'VHCT (Preliminary): See Section 2 for Waveforms (Continued)

Symbol	Parameter	V _{CC} (V)	74VHCT		Units	Conditions	Fig. No.
			T _A = 25°C				
			Typ	Limits			
**V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5	V	C _L = 50 pF	2-11, 12
**V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-1.0	-1.3	V	C _L = 50 pF	2-11, 12
**V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0		2.0	V	C _L = 50 pF	2-11, 12
**V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0		0.8	V	C _L = 50 pF	2-11, 12

**Parameter guaranteed by design.

AC Electrical Characteristics for 'VHC Family Devices : See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHC		74VHC		Units	Conditions	Fig. No.	
			T _A = 25°C			T _A = -40°C to +85°C				
			Min	Typ	Max	Min				Max
t _{PLH} t _{PHL}	Propagation Delay Time (LE to O _n)	3.3 ± 0.3	7.6	11.9	1.0	14.0	ns	C _L = 15 pF	2-6	
			10.1	15.4	1.0	17.5				
		5.0 ± 0.5	5.0	7.7	1.0	9.0	ns	C _L = 15 pF	2-6	
			6.5	9.7	1.0	11.0				
t _{PLH} t _{PHL}	Propagation Delay Time (D-O _n)	3.3 ± 0.3	7.0	11.0	1.0	13.0	ns	C _L = 15 pF	2-5	
			9.5	14.5	1.0	16.5				
		5.0 ± 0.5	4.5	6.8	1.0	8.0	ns	C _L = 15 pF	2-5	
			6.0	8.8	1.0	10.0				
t _{PZL} t _{PZH}	TRI-STATE Output Enable Time	3.3 ± 0.3	7.3	11.5	1.0	13.5	ns	R _L = 1 kΩ	C _L = 15 pF	2-7, 8
			9.8	15.0	1.0	17.0				
		5.0 ± 0.5	5.2	7.7	1.0	9.0	ns	C _L = 15 pF	2-7, 8	
			6.7	9.7	1.0	11.0				
t _{PLZ} t _{PHZ}	TRI-STATE Output Disable Time	3.3 ± 0.3	10.7	14.5	1.0	16.5	ns	R _L = 1 kΩ	C _L = 50 pF	2-7, 8
		5.0 ± 0.5	6.7	9.7	1.0	11.0			C _L = 50 pF	2-7, 8
t _{OSLH} t _{OSHL}	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 1)	C _L = 50 pF	
		5.0 ± 0.5		1.0		1.0			C _L = 50 pF	
C _{IN}	Input Capacitance		4	10		10	pF	V _{CC} = Open		
C _{OUT}	Output Capacitance		6				pF	V _{CC} = 5.0V		
C _{PD}	Power Dissipation Capacitance		29				pF	(Note 2)		

Note 1: Parameter guaranteed by design. t_{OSLH} = |t_{PLH} max - t_{PLH} min|; t_{OSHL} = |t_{PHL} max - t_{PHL} min|

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}/8 (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD}(total) = 21 + 8n.

AC Operating Requirements for 'VHC Devices : See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHC			74VHC		Units	Conditions	Fig. No.
			T _A = 25°C			T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max			
t _{w(H)} t _{w(L)}	Minimum Pulse Width (LE)	3.3 ± 0.3	5.0			5.0		ns		2-6
		5.0 ± 0.5	5.0			5.0				
t _s	Minimum Setup Time	3.3 ± 0.3	3.5			3.5		ns		2-9
		5.0 ± 0.5	3.5			3.5				
t _h	Minimum Hold Time	3.3 ± 0.3	1.5			1.5		ns		2-9
		5.0 ± 0.5	1.5			1.5				

AC Electrical Characteristics for 'VHCT (Preliminary) : See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHCT			74VHCT		Units	Conditions	Fig. No.
			T _A = 25°C			T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation Delay Time (LE to O _n)	5.0 ± 0.5	7.7	12.3	1.0	13.5	ns	C _L = 15 pF C _L = 50 pF	2-6	
			8.5	13.3	1.0	14.5				
t _{PLH} t _{PHL}	Propagation Delay Time (D to O _n)	5.0 ± 0.5	5.1	8.5	1.0	9.5	ns	C _L = 15 pF C _L = 50 pF	2-5	
			5.9	9.5	1.0	10.5				
t _{PZL} t _{PZH}	TRI-STATE Output Enable Time	5.0 ± 0.5	6.3	10.9	1.0	12.5	ns	R _L = 1 kΩ C _L = 15 pF C _L = 50 pF	2-7, 8	
			7.1	11.9	1.0	13.5				
t _{PLZ} t _{PHZ}	TRI-STATE Output Disable Time	5.0 ± 0.5	6.8	11.2	1.0	12.0	ns	R _L = 1 kΩ C _L = 50 pF	2-7, 8	
t _{OSLH} t _{OSHL}	Output to Output Skew	5.0 ± 0.5	1.0		1.0		ns	(Note 1)		
C _{IN}	Input Capacitance		4	10	10		pF	V _{CC} = Open		
C _{OUT}	Output Capacitance		9					pF	V _{CC} = 5.0V	
C _{PD}	Power Dissipation Capacitance		27					pF	(Note 2)	

Note 1: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH \max} - t_{PLH \min}|$; $t_{OSHL} = |t_{PHL \max} - t_{PHL \min}|$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC \text{ (opr.)}} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC/8}$ (per F/F). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: $C_{PD \text{ (total)}} = 14 + 13n$.

AC Operating Requirements for 'VHCT (Preliminary) : See Section 2 for Waveforms

Symbol	Parameter	V _{CC} (V)	74VHCT			74VHCT		Units	Conditions	Fig. No.
			T _A = 25°C			T _A = -40°C to +85°C				
			Min	Typ	Max	Min	Max			
t _{w(H)}	Minimum Pulse Width (LE)	5.0 ± 0.5	6.5			6.5		ns		2-6
t _s	Minimum Setup Time	5.0 ± 0.5	1.5			1.5		ns		2-9
t _h	Minimum Hold Time	5.0 ± 0.5	3.5			3.5		ns		2-9