XECOM

XE1216/XE1216C SMARTWATCH

FEATURES

- SmartWatch keeps track of hundredth of seconds, seconds, minutes, hours, days, date of the month, months, and years.
- Converts standard 2K x 8, 8K x 8 and 32K x 8 CMOS static RAMS into nonvolatile memory.
- Embedded lithium energy cell maintains watch information and retains RAM data.
- Watch function is transparent to RAM operation.
- Month and year determine the number of days in each month.
- Proven gas-tight socket contacts.
- Full 10% operating range.
- Operating temperature range 0°C to 70°C.
- Accuracy is better than ± 1 min./month @ 25°C.

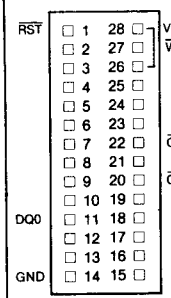
DESCRIPTION

The XE1216 and XE1216C are 28-pin 0.6 inch-wide DIP sockets with a built-in CMOS watch function, a non-volatile RAM controller circuit, and an embedded lithium energy source. The XE1216 accepts either 24-pin 2K x 8 or 28-pin 8K x 8 JEDEC Bytewide CMOS static RAMS. The XE1216C accepts either 28-pin 8K x 8 or 32K x 8 JEDEC Bytewide CMOS static RAMs.

When the socket is mated with an appropriate CMOS static RAM, it provides a complete solution to problems associated with memory volatility and uses a common energy source to maintain time and date. A key feature of the SmartWatch is that the watch function remains transparent to the static RAM. The SmartWatch monitors VCC for an out of tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent loss of watch and RAM data. The SmartWatch uses pins 28, 27, 26, 22, 20, 11 and 1 for RAM and watch control. All other pins are passed straight through to the socket receptacle.

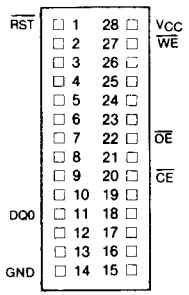
PIN CONNECTIONS

XE1216



All Pins Pass Through Except 20, 26, 28
Pin 20 Conditioned Chip Enable
Pin 26 Switched VCC for 24 Pin RAM
Pin 28 Switched VCC for 28 Pin RAM
Pin 1 $\overline{\text{RESET}}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

XE 1216C



All Pins Pass Through Except 20, 28
Pin 20 Conditioned Chip Enable
Pin 28 Switched VCC
Pin 1 $\overline{\text{RESET}}$
Pin 22 Output Enable
Pin 27 Write Enable
Pin 11 Data Input/Output 0
Pin 14 Ground

The SmartWatch provides time keeping information including hundredths of seconds, seconds, minutes, hours, day, date, month and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

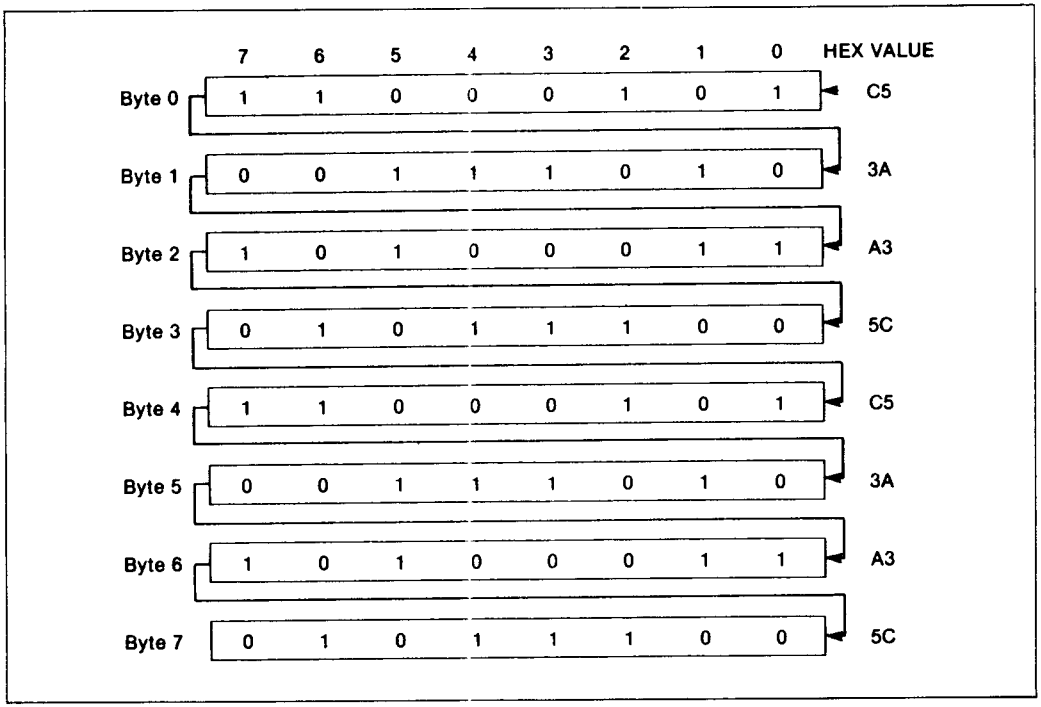
Communication with the SmartWatch is established by pattern recognition on a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses which occur prior to recognition of the 64 bit pattern are directed to memory. After recognition is established, the next 64 read or write cycles either extract or update data in the Smart Watch, memory access is inhibited.

Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of chip enable ($\overline{CE}$), output enable ($\overline{OE}$) and write enable ($\overline{WE}$). Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the SmartWatch starts the pattern recognition sequence by moving a pointer to the first bit of the 64 bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the SmartWatch. These 64 cycles are used only to gain access to the SmartWatch, therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to the SmartWatch are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a SmartWatch scratch pad. When the first write cycle is executed, it is compared to bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

NONVOLATILE CONTROLLER OPERATION

The XE1216 SmartWatch performs circuit functions required to make a CMOS RAM nonvolatile. First, a switch is provided to direct power from the battery or VCC supply, depending on which voltage is greater. This switch has a voltage drop of less than 0.2 volts. The second function which is involved is power fail detection. Power fail detection occurs at typically 4.25 volts. The XE1216 constantly monitors the VCC supply. When VCC goes out of tolerance, a comparator outputs a power fail signal to the chip enable logic. The third function accomplishes write protection by holding the chip enable signal to the memory within 0.2 volts of VCC or battery. During nominal power supply conditions the memory chip enable signal will track the chip enable signal sent to the socket with a maximum propagation delay of 20 ns.

SMARTWATCH COMPARISON REGISTER DEFINITION — Figure 1



NOTE:
The pattern recognition in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the SmartWatch is less than 1 to 10^{19}.

SMARTWATCH REGISTER INFORMATION

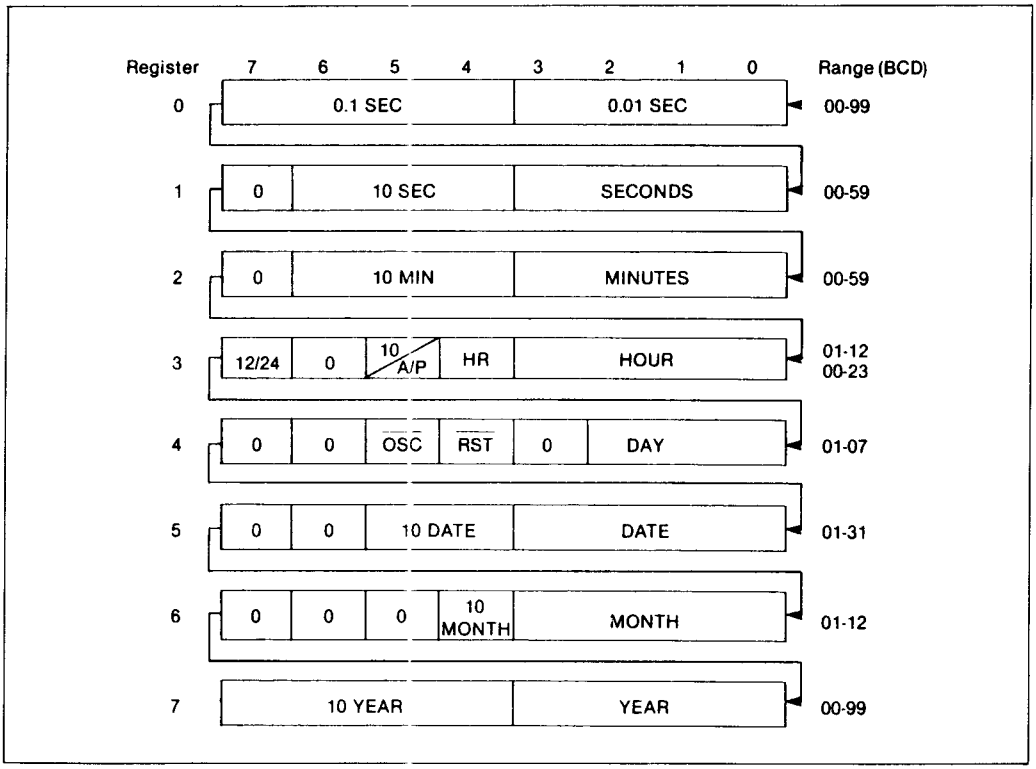
The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64 bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch register is in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12 hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24 hour mode, bit 5 is the second 10-hour bit (20-23 hours).

SMARTWATCH REGISTER DEFINITION — Figure 2



OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from XECOM set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5 and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to + 7V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 70°C
Soldering Temperature	260°C for 10 Sec

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PIN 26L, Pin 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1, 3
Logic 1	V_{IH}	2.2		V_{CC} + 0.3	V	1, 10
Logic 0	V_{IL}	-0.3		+ 0.8	V	1, 10

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, VCC = 4.5 to 5.5V)

PIN 26L, PIN 28L Supply	I_{CCI}			5	mA	3, 4, 5
PIN 26U, PIN 28U Supply Voltage	V_{CCO}	V_{CC} - 0.2			V	3, 8
PIN 26U, PIN 28U Supply Current	I_{CCO}			80	mA	3, 8
Input Leakage	I_{IL}	-1.0		+ 1.0	μA	4,10,13
Output @ 2.4V	I_{OH}	- 1.0			mA	2
Output @ 0.4V	I_{OL}			4.0	mA	2

(0°C to 70°, VCC < 4.5V)

PIN 20U Output	V_{OHL}	V_{CC} - .02 V_{BAT} - 0.2			V	3
PIN 26U, PIN 28U Battery Current	I_{BAT}			1	μA	3, 6
PIN 26U, PIN 28U Battery Current	V_{BAT}	2	3	3.6	V	3

CAPACITANCE

(tA = 25°C)

PARAMETER	SYMBOL	MIN	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

A.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, VCC = 4.5 to 5.5V)

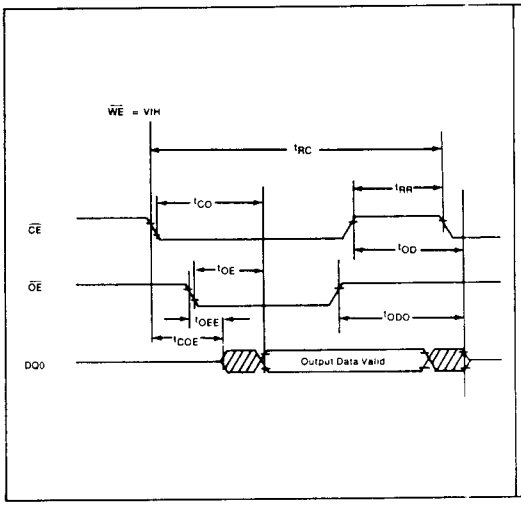
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			100	ns	
$\overline{CE}$ To Output Low Z	t_{COE}	10			ns	
$\overline{OE}$ To Output Low Z	t_{OEE}	10			ns	
$\overline{CE}$ To Output High Z	t_{OD}			100	ns	
$\overline{OE}$ To Output High Z	t_{ODO}			100	ns	
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
Write Pulse Width	t_{WP}	170			ns	
Write Recovery	t_{WR}	50			ns	11
Data Set Up Time	t_{DS}	100			ns	11
Data Hold Time	t_{DH}	0			ns	12
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
Preset Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2, 9
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

(0°C to 70°C, VCC < 4.5V)

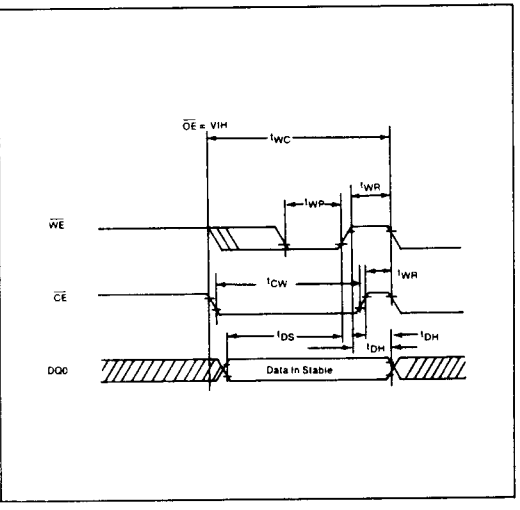
Recovery at Power Up	t_{REC}			2	ms	
VCC Slew Rate 4.5 - 3V	t_F	300			μs	
$\overline{CE}$ Pulse Width	t_{CE}			1.5	μs	7

TIMING DIAGRAMS

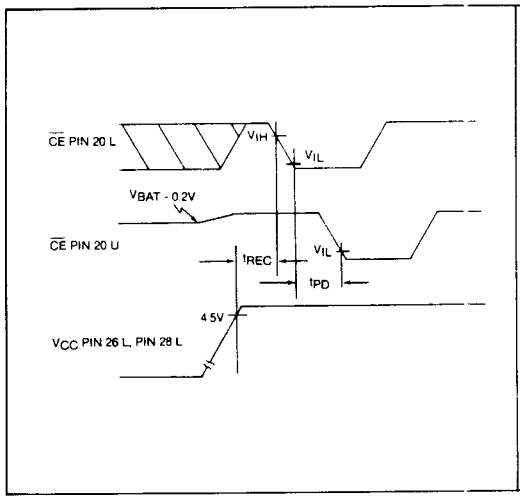
READ CYCLE TO SMARTWATCH



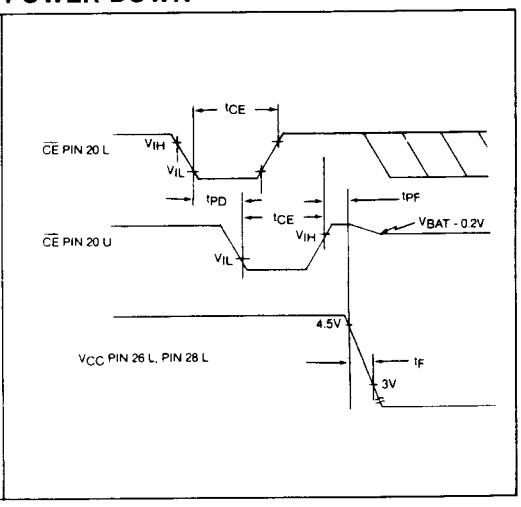
WRITE CYCLE TO SMARTWATCH



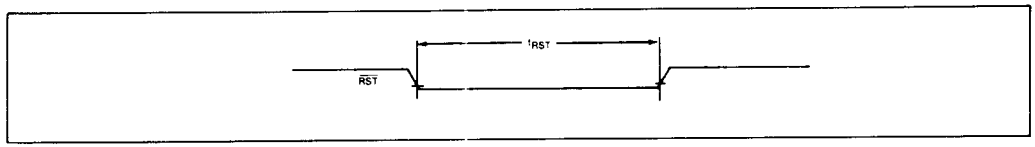
POWER UP



POWER DOWN



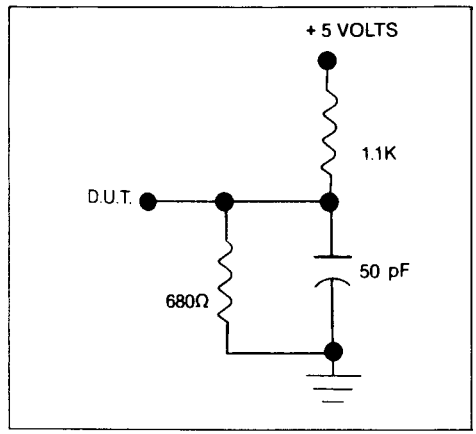
RESET FOR SMARTWATCH



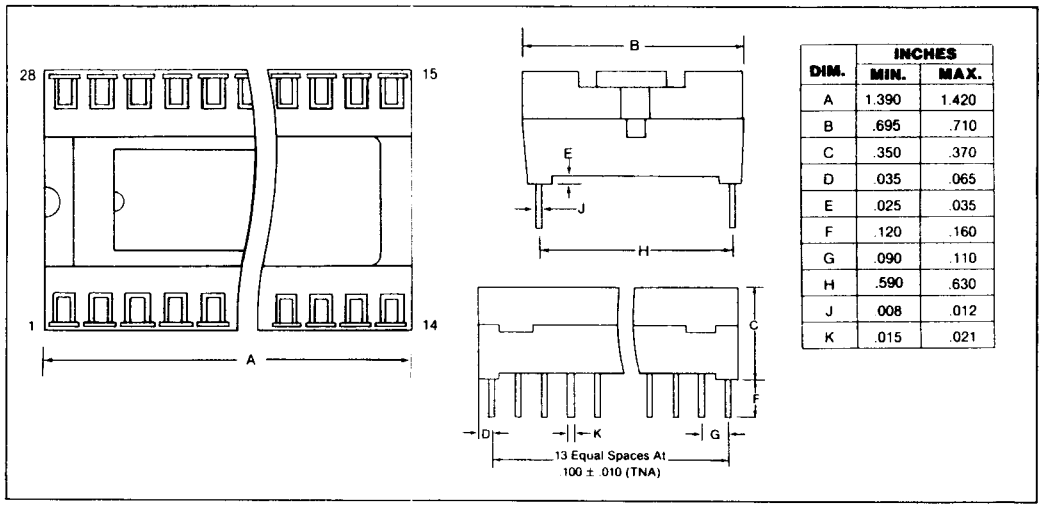
NOTES

1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 3.
3. PIN locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. PIN 26 L may be connected to VCC or left disconnected at the P.C. board.
6. IBAT is the maximum current which a correctly installed memory can use in the data retention mode and meet data retention expectations of more than 10 years at 25 °C.
7. ^{t}CE max. must be met to insure data integrity on power loss.
8. VCC is within nominal limits and a memory is installed in the socket.
9. Input pulse rise and fall times equal 10 ns.
10. Applies to Pins 1 L, 11 L, 20 L, 22 L and 27 L.
11. ^{t}WR is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
12. ^{t}DH and ^{t}DS are a function of the first occurring edge of $\overline{WE}$ or $\overline{CE}$.
13. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

OUTPUT LOAD — Figure 3



MECHANICAL SPECIFICATIONS



DIM.	INCHES MIN.	INCHES MAX.
A	1.390	1.420
B	.695	.710
C	.350	.370
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021

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