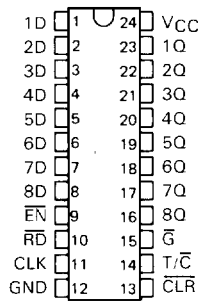
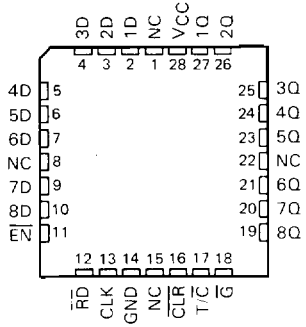
D2854, OCTOBER 1984 – REVISED JUNE 1986

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- T/$\overline{C}$ Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DW OR NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection.

description

These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable ($\overline{EN}$) is low. Data can be read-back onto the data inputs by taking the read input ($\overline{RD}$) low, in addition to having $\overline{EN}$ low. Whenever $\overline{EN}$ is high, both the read-back and write modes are disabled. Transitions on $\overline{EN}$ should only be made with CLK high in order to prevent false clocking.

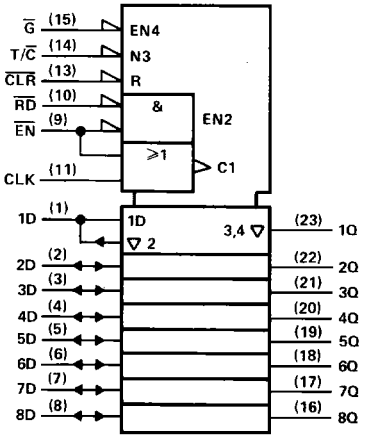
The polarity of the Q outputs can be controlled by the polarity input T/$\overline{C}$. When T/$\overline{C}$ is high, Q will be the same as is stored in the flip-flops. When T/$\overline{C}$ is low, the output data will be inverted. The Q outputs can be placed in a high-impedance state by taking the output control ($\overline{G}$) high. The output control $\overline{G}$ does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input ($\overline{CLR}$) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

The -1 version of the SN74ALS996 is identical to the standard version except that the recommended maximum I_{OL} is increased to 48 milliamperes.

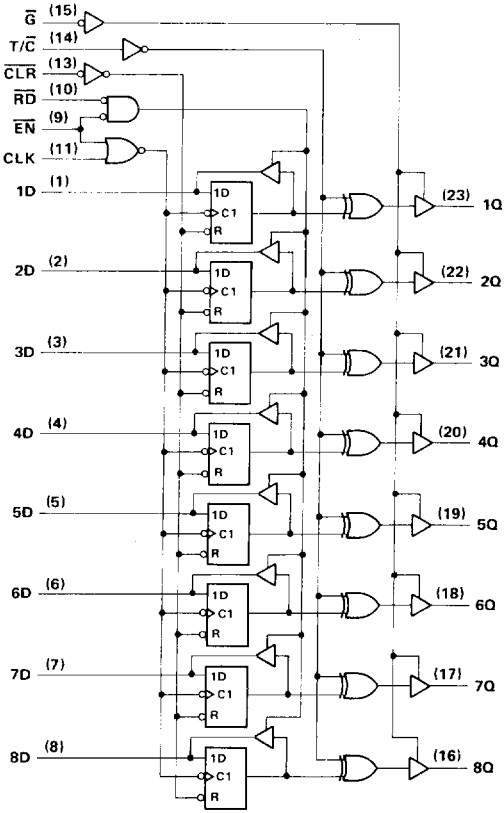
The SN74ALS996 is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

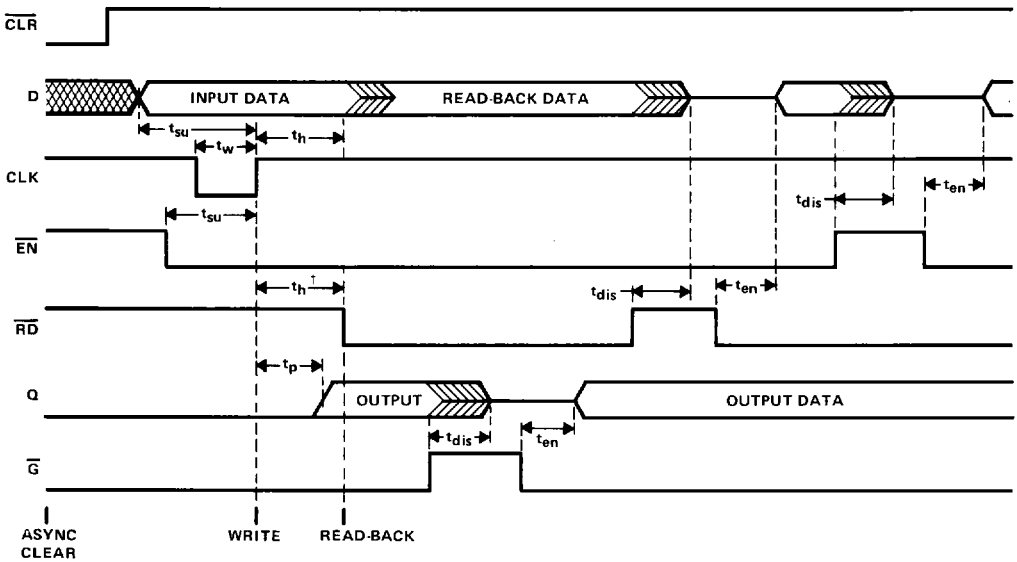
logic diagram (positive logic)



Pin numbers shown are for DW and NT packages.

timing diagram

($T/\overline{C}$ = H)



†This hold time ensures the readback circuit will not create a conflict on the input data bus.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage ($\overline{G}$, $\overline{RD}$, $\overline{EN}$, CLK, $\overline{CLR}$, and T/$\overline{C}$) . . . . . 7 V
Voltage applied to D inputs and to disabled 3-state outputs . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Q			−2.6	mA
		D			−0.4	
I_{OL}	Low-level output current	Q			24	mA
					48†	
		D			8	
f_{clock}	Clock frequency		0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			ns
		CLK low	14.5			
		CLK high	14.5			
t_{su}	Setup time	Data before CLK↑	15			ns
		$\overline{EN}$ low before CLK↑	10			
		CLK high before $\overline{EN}$↑‡	15			
		$\overline{CLR}$ high (inactive) before CLK↑	10			
t_h	Hold time	Data after CLK↑	0			ns
		$\overline{EN}$ low after CLK↑	5			
		$\overline{RD}$ high after CLK↑§	5			
T_A	Operating free-air temperature		0		70	°C

†The 48-mA limit applies only to the -1 versions and only if V_{CC} is maintained between 4.75 V and 5.25 V.
‡This setup time guarantees that $\overline{EN}$ will not false clock the data register.
§This hold time ensures there will be no conflict on the input data bus.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
	Q	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	D	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.35	0.5	
	Q	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4	
		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	
		V_{CC} = 4.75 V,	I_{OL} = 48 mA (-1 versions)		0.35	0.5	
I_{OZH}	Q	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−20	
I_I	D inputs	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	mA
	All others	V_{CC} = 5.5 V,	V_I = 7 V			0.1	
I_{IH}	D inputs‡	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	All others					20	
I_{IL}	D inputs‡	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1	mA
	All others					−0.1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V, EN, RD low	Q outputs high		35	55	mA
			Q outputs low		55	85	
			Q outputs disabled		42	65	

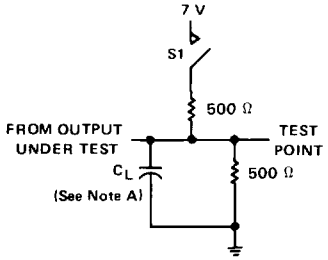
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ The output conditions have been chosen to produce current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

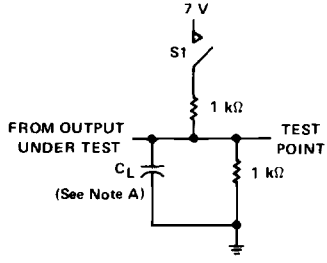
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, T_A = 0°C to 70°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}				40		35		MHz
t_{PLH}	CLK (T/$\overline{C}$ = H or L)	Q		16	24	5	28	ns
t_{PHL}				16	24	5	28	
t_{PLH}	$\overline{CLR}$ (T/$\overline{C}$ = L)	Q		15	23	7	27	ns
t_{PHL}	$\overline{CLR}$ (T/$\overline{C}$ = H)			13	19	7	23	
t_{PLH}	T/$\overline{C}$	Q		13	20	5	23	ns
t_{PHL}				13	20	5	23	
t_{PHL}	$\overline{CLR}$	D		19	25	8	30	ns
t_{en}	$\overline{RD}$	D		9	15	3	16	ns
t_{dis}				10	16	3	19	
t_{en}	$\overline{EN}$	D		9	14	3	16	ns
t_{dis}				10	16	3	19	
t_{en}	$\overline{G}$	Q		8	13	4	15	ns
t_{dis}				4	8	1	10	

t_{en} = t_{PZH} or t_{PZL}
t_{dis} = t_{PHZ} or t_{PLZ}

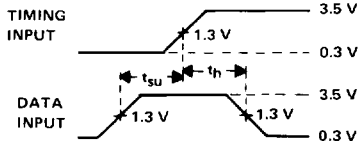
PARAMETER MEASUREMENT INFORMATION



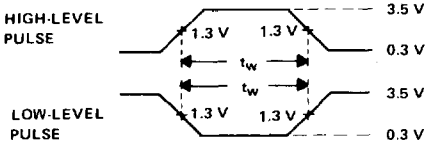
LOAD CIRCUIT FOR Q OUTPUTS



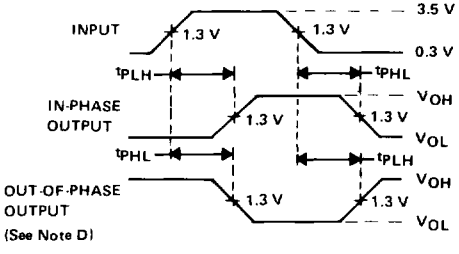
LOAD CIRCUIT FOR D OUTPUTS



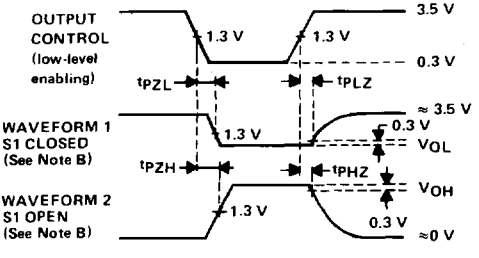
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is open.

FIGURE 1