BiCMOS 16KX4 Bit Static RAM (With $\overline{OE}$)

FEATURES

- **Fast Access Time: 10, 12, 15, 20ns (max.)**
- **Low Power Dissipation**
  - **Standby ..... 20mA (max.)**
  - **Operating ..... 160mA (max.)**
- **Single 5V±10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Fully Static Operation**
  - **—No clock or refresh required**
- **Standard Pin Configuration**
  - **KM64B66P: 24-pin DIP (300 mil.)**
  - **KM64B66J: 24-pin SOJ (300 mil.)**

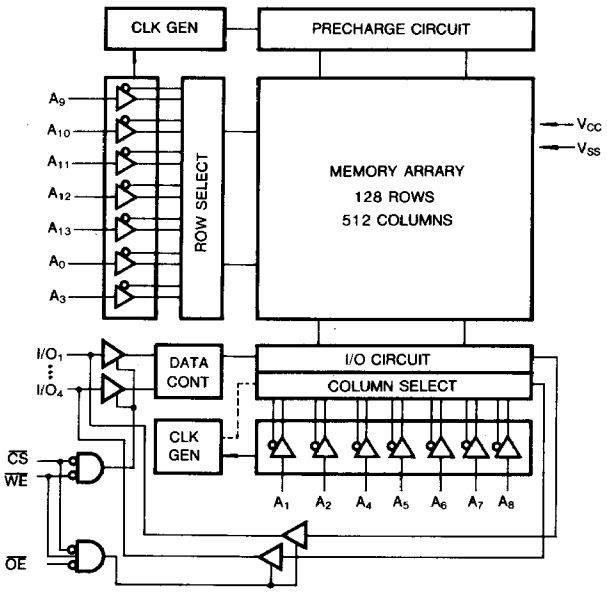
GENERAL DESCRIPTION

The KM64B66 is a 65,536-bit high-speed Static Random Access Memory organized as 16,384 words by 4 bits.

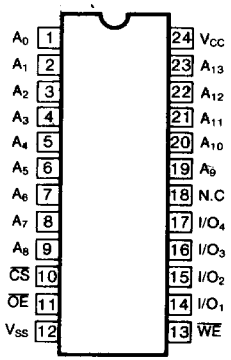
The device is fabricated using Samsung's advanced BiCMOS process.

The KM64B66 has been designed for high speed applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



(DIP and SOJ)

Pin Name	Pin Function
A_0-A_{13}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O_1-I/O_4	Data Inputs/Outputs
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on V_{CC} Supply Relative to V_{SS}	V_{IN}, V_{OUT}	−0.5 to 6.5	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−0.5 to 6.5	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	−55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

* Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $T_A=0°C$ to $+70°C$)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Input Leakage Current	$\|I_U\|$	$V_{IN}=V_{SS}$ to V_{CC}, V_{CC}=Max.				2	μA
Output Leakge Current	$\|I_{LO}\|$	$\overline{CS}=V_{IH}$, $\overline{WE}=V_{IL}$ $V_{I/O}=V_{SS}$ to V_{CC}, V_{CC}=Max.				10	μA
Operating Current	I_{CC1}	$f_{MAX}=0$, $I_{I/O}=0mA$, $\overline{CS}=V_{IL}$				80	mA
	I_{CC2}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$, Min Cycle=100% Duty	−10			160	mA
			−12			140	
			−15			120	
			−20			100	
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$				20	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$ $V_{IN}\leq 0.2V$ or $V_{IN}\geq V_{CC}-0.2V$				8	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$				0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$		2.4			V
Input High Voltage	V_{IH}			2.2		$V_{CC}+0.5$	V
Input Low Voltage	V_{IL}	Min=−3.0V for <20ns pulse*		−0.5		0.8	V

* Note: This V_{IL} description is not a test condition. It is an Absolute Maximum Rating. V_{IL} condition greater than those described use Improger functional operation of the device.

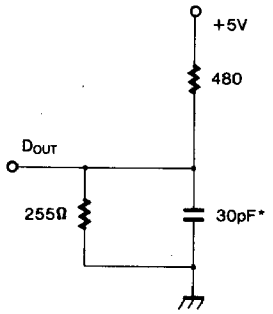
CAPACITANCE* ($f=1MHz$, $T_A=25°C$)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Capacitance	C_{IN}	$V_{IN}=0V$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT}=0V$	—	7	pF

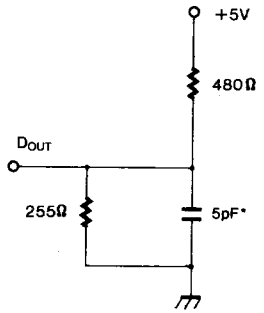
TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See below

Output Load (A)



Output Load (B)
(for t_{CHZ}, t_{OHZ}, t_{CLZ}, t_{OLZ}, t_{WZ} & t_{OW})

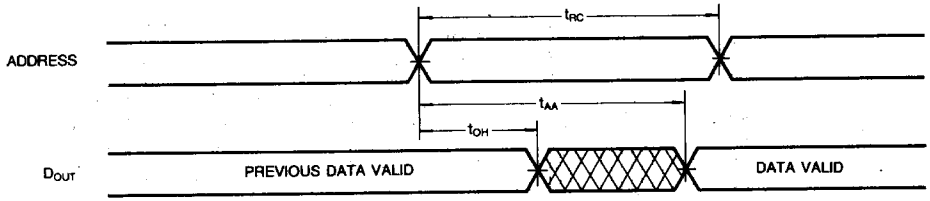


* Including Scope and Jig Capacitance

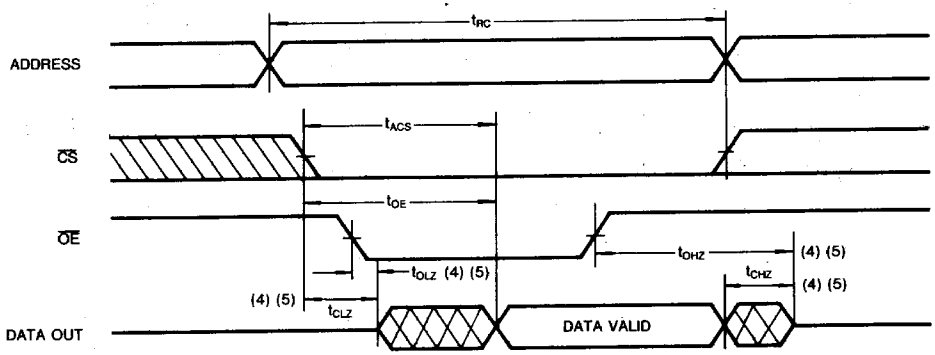
READ CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	Symbol	KM64B66-10		KM64B66-12		KM64B66-15		KM64B66-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10		12		15		20		ns
Address Access Time	t_{AA}		10		12		15		20	ns
Chip Select to Output	t_{ACS}		10		12		15		20	ns
Chip Select to Output Low-Z (Note 4,5)	t_{CLZ}	3		3		3		3		ns
Output Enable to Output Valid	t_{OE}		6		7		8		8	ns
Output Enable to Low-Z (Note 4,5)	t_{OLZ}	1		1		1		2		ns
Chip Disable to High-Z Output (Note 4,5)	t_{CHZ}		4		5		6		8	ns
Output Disable to High-Z (Note 4,5)	t_{OHZ}		4		5		6		8	ns
Output Hold from Address Change	t_{OH}	3		3		3		3		ns

TIMING WAVEFORM OF READ CYCLE NO. 1 (Note 1, 2, 6)



TIMING WAVEFORM OF READ CYCLE NO. 2 (Note 1, 3, 5)

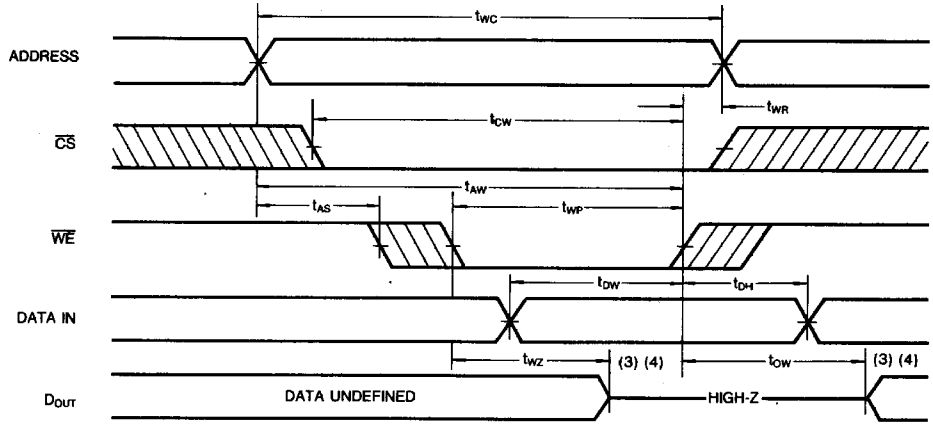


Notes:
1. $\overline{WE}$ is high for ready cicle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max) is less than t_{LZ} (min) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (b).
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.

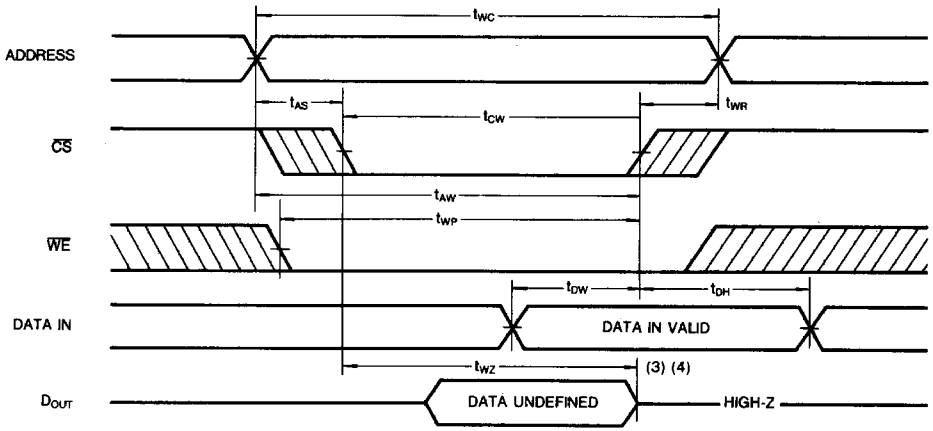
WRITE CYCLE (V_{CC}=5V±10%, T_A=0°C to +70°C)

Parameter	Symbol	KM64B66-10		KM64B66-12		KM64B66-15		KM64B66-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle	t_{WC}	10		12		15		20		ns
Chip Select to End of Write	t_{CW}	6		8		10		13		ns
Address Setup	t_{AS}	0		0		0		0		ns
Address Valid to End of Write	t_{AW}	6		8		10		13		ns
Write Pulse Width	t_{WP}	6		8		10		13		ns
Write Recovery	t_{WR}	0		0		0		0		ns
Write to Output High-Z	t_{WZ}		4		6		6		8	ns
Data to Write Time Overlap	t_{DW}	6		6		8		10		ns
Data Hold from Write	t_{DH}	0		0		0		0		ns
End Write to Output Low-Z	t_{OW}	3		3		3		3		ns

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$, and a low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load (B).
4. This parameter is sampled and not 100% tested.
5. At any given temperature and voltage condition, t_{WZ}(max) is less that t_{OW}(min) both for a given device and from device to device.
6. $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

FUNCTIONAL DESCRIPTION

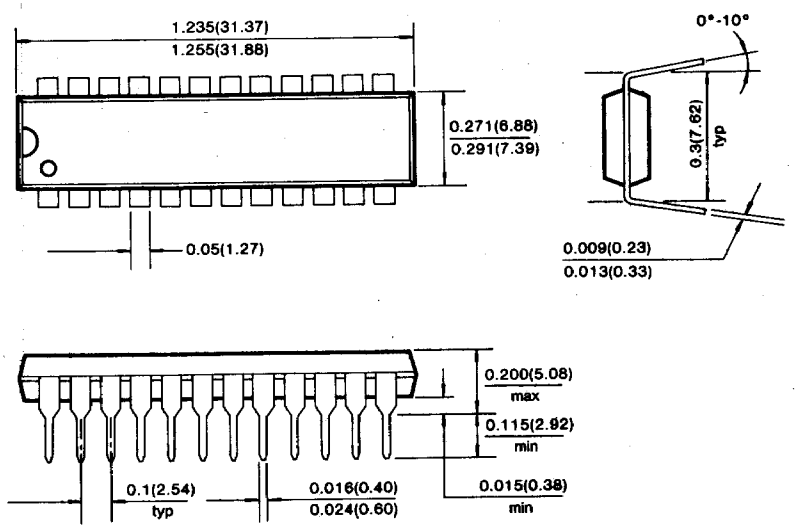
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current	Mode
H	X	X	High-Z	I_{SB}, I_{SB1}	Standby Mode
L	H	H	D_{OUT}	I_{CC1}, I_{CC2}	Output Disable
L	H	L	D_{OUT}	I_{CC1}, I_{CC2}	Read
L	L	X	D_{IN}	I_{CC1}, I_{CC2}	Write

* Note: X means Don't Care

PACKAGE DIMENSIONS

24 PIN PLASTIC DUAL-IN-LINE PACKAGE

Unit: Inches (Milimeters)



24 PIN PLASTIC SMALL OUTLINE J FORM PACKAGE