54/7473 01101D
54H/74H73 01101H
54LS/74LS73 01101J

DUAL JK FLIP-FLOP
(With Separate Clears and Clocks)

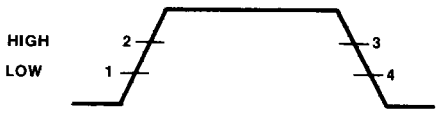
DESCRIPTION — The '73 and 'H73 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM



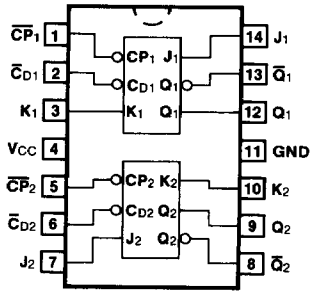
Asynchronous Input:
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear is independent of clock

The 'LS73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

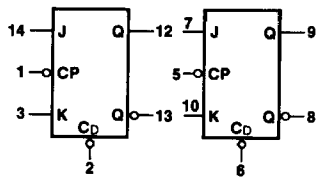
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7473PC, 74H73PC 74LS73PC		9A
Ceramic DIP (D)	A	7473DC, 74H73DC 74LS73DC	5473DM, 54H73DM 54LS73DM	6A
Flatpak (F)	A	7473FC, 74H73FC 74LS73FC	5473FM, 54H73FM 54LS73FM	3I

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



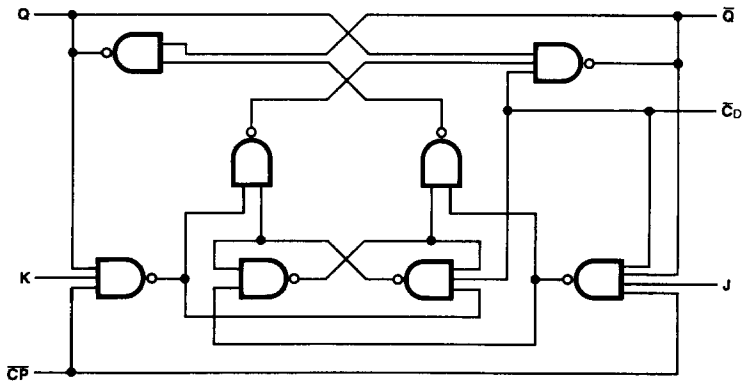
V_{CC} = Pin 4
GND = Pin 11

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

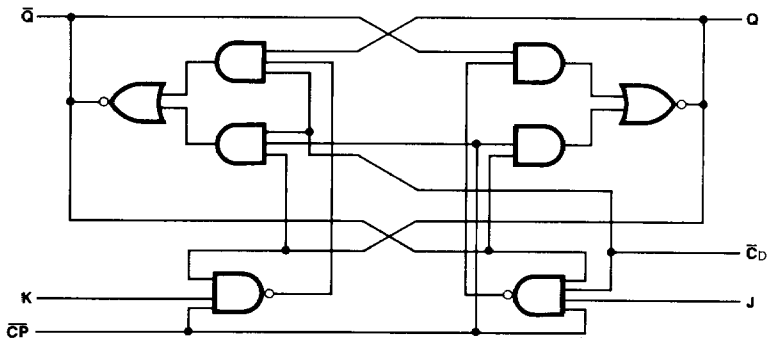
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	1.25/1.25	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	2.5/2.5	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	20/10	12.5/12.5	10/5.0 (2.5)

LOGIC DIAGRAMS (one half shown)

'73, 'H73



'LS73



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		40		50		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74H C_L = 25 pF, R_L = 280 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	15		25		30		MHz	Fig. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q or $\overline{Q}$		25 40		21 27		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q or $\overline{Q}$		25 40		13 24		20 30	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74H		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		20		ns	Fig. 3-18 ('73, 'H73) Fig. 3-7 ('LS73)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		12 16		13.5 20		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ Pulse Width LOW	25		16		25		ns	Figs. 3-1, 3-10