

# NM93CS06LZ/CS46LZ/CS56LZ/CS66LZ 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.7V to 5.5V) and Data Protect (MICROWIRE™ Bus Interface)

## General Description

The NM93CS06LZ/CS46LZ/CS56LZ/CS66LZ devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CSxxLZ Family functions in an extended voltage operating range and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. N registers ( $N \leq 16$ ,  $N \leq 64$ ,  $N \leq 128$ ,  $N \leq 256$ ) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. (All registers greater than, or equal to, the selected address are then protected from further change.) Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

These devices are available in both SO and TSSOP packages for small space considerations.

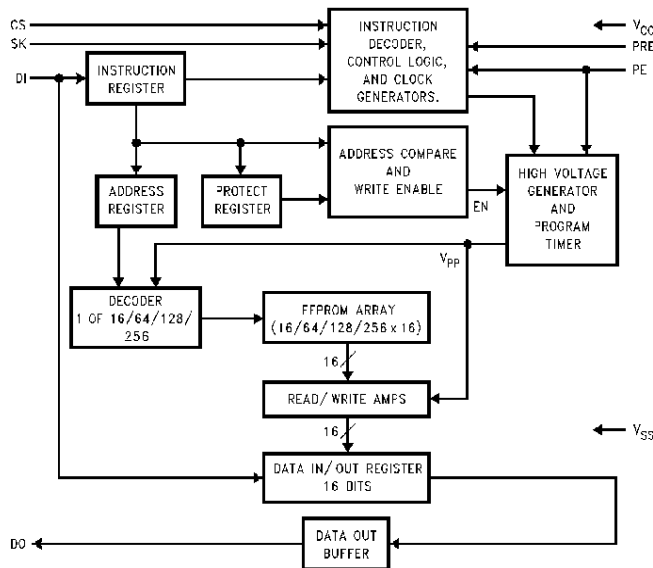
The serial interface that control these EEPROMs is MICROWIRE compatible, providing simple interfacing to standard microcontrollers and microprocessors. There are a

total of 10 instructions, 5 which operate on the EEPROM memory and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PREAD, PRWRITE, PRCLEAR, PRDISABLE and PRENABLE.

## Features

- 2.7V to 5.5V operation in all modes
- Less than 1.0  $\mu\text{A}$  standby current
- Sequential register read
- Write protection in a user-defined section of memory
- Typical active current of 200  $\mu\text{A}$
- Direct write: no erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance:  $10^6$  changes
- Packages available: 8-pin SO, 8-pin DIP, 8-Pin TSSOP

## Block Diagram

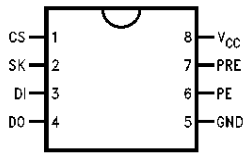


TL/D/11807-1

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MICROWIRE™ is a trademark of National Semiconductor Corporation.

## Connection Diagrams

Dual-In-Line Package (N),  
8-Pin SO Package (M8) and  
8-Pin TSSOP Package (MT8)



Top View

TL/D/11807-2

NS Package Number N08E (N)  
NS Package Number M08A (M8)  
NS Package Number MTC08 (MT8)

### Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V <sub>CC</sub>	Power Supply

## Ordering Information

### Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06LZN/NM93CS46LZN/NM93CS56LZN/NM93CS66LZN NM93CS06LZM8/NM93CS46LZM8/NM93CS56LZM8/NM93CS66LZM8 NM93CS46LZMT8/NM93CS56LZMT8/NM93CS66LZMT8

### Extended Temp. Range (-40°C to +85°C)

Order Number
NM93CS06LZEN/NM93CS46LZEN/NM93CS56LZEN/NM93CS66LZEN NM93CS06LZEM8/NM93CS46LZEM8/NM93CS56LZEM8/NM93CS66LZEM8 NM93CS46LZEMT8/NM93CS56LZEMT8/NM93CS66LZEMT8

### Automotive Temp. Range (-40°C to +125°C)

Order Number
NM93CS06LZVN/NM93CS46LZVN/NM93CS56LZVN/NM93CS66LZVN NM93CS06LZVM8/NM93CS46LZVM8/NM93CS56LZVM8/NM93CS66LZVM8 NM93CS06LZVMT8/NM93CS46LZVMT8/NM93CS56LZVMT8/NM93CS66LZVMT8

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	$V_{CC} + 1V$ to $-0.3V$
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

**Operating Conditions**

Ambient Operating Temperature	0°C to +70°C
NM93CSxxLZ	-40°C to +85°C
NM93CSxxLZE	-40°C to +125°C
NM93CSxxLZV	
Power Supply ( $V_{CC}$ ) Range	2.7V to 5.5V

**DC and AC Electrical Characteristics: 2.7V <  $V_{CC}$  < 4.5V**

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
$I_{CCA}$	Operating Current		CS = $V_{IH}$ , SK = 250 kHz		1	mA
$I_{CCS}$	Standby Current		CS = 0V		1	$\mu A$
$I_{IL}$ $I_{OL}$	Input Leakage Output Leakage		$V_{IN} = 0V$ to $V_{CC}$ (Note 3)		$\pm 200$	nA
$V_{IL}$ $V_{IH}$	Input Low Voltage Input High Voltage			-0.1 $0.8 V_{CC}$	$0.15 V_{CC}$ $V_{CC} + 1$	V
$V_{OL}$ $V_{OH}$	Output Low Voltage Output High Voltage		$I_{OL} = 10 \mu A$ $I_{OH} = -10 \mu A$	$0.9 V_{CC}$	$0.1 V_{CC}$	V
fSK	SK Clock Frequency		(Note 4)	0	250	kHz
tSKH	SK High Time			1		$\mu s$
tSKL	SK Low Time			1		$\mu s$
tSKS	SK Setup Time			0.4		$\mu s$
tCS	Minimum CS		(Note 2)	1		$\mu s$
tCSS	CS Setup Time			0.2		$\mu s$
tPRES	PRE Setup Time			0.2		$\mu s$
tPES	PE Setup Time			0.2		$\mu s$
tDIS	DI Setup Time			0.4		$\mu s$
tDH	DO Hold Time			70		ns
tCSH	CS Hold Time			0		$\mu s$
tPEH	PE Hold Time			0.4		$\mu s$
tPREH	PRE Hold Time			0.4		$\mu s$
tDIH	DI Hold Time			0.4		$\mu s$
tPD1	Output Delay to "1"				2	$\mu s$
tPD0	Output Delay to "0"				2	$\mu s$
tSV	CS to Status Valid				1	$\mu s$
tDF	CS to DO in TRI-STATE®		CS = $V_{IL}$		0.4	$\mu s$
tWP	Write Cycle Time		$V_{CC} = 2.7V$		15	ms
			$V_{CC} = 2.7V$		15	ms

### DC and AC Electrical Characteristics: 4.5V < V<sub>CC</sub> < 5.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I <sub>CCA</sub>	Operating Current		CS = V <sub>IH</sub> , SK = 1.0 MHz		1	mA
I <sub>CCS</sub>	Standby Current		CS = 0V		1	μA
I <sub>IL</sub> I <sub>OL</sub>	Input Leakage Output Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub>		± 200	nA
V <sub>IL</sub> V <sub>IH</sub>	Input Low Voltage Input High Voltage			-0.1 2	0.8 V <sub>CC</sub> + 1	V V
V <sub>OL1</sub> V <sub>OH1</sub>	Output Low Voltage Output High Voltage		I <sub>OL</sub> = 2.1 mA I <sub>OH</sub> = -400 μA	2.4	0.4	V V
V <sub>OL2</sub> V <sub>OH2</sub>	Output Low Voltage Output High Voltage		I <sub>OL</sub> = 10 μA I <sub>OL</sub> = -10 μA	V <sub>CC</sub> - 0.2	0.2	V V
f <sub>SK</sub>	SK Clock Frequency		(Note 5)	0	1	MHz
t <sub>SKH</sub>	SK High Time	NM93CS06LZ-NM93CS66LZ NM93CS06LZE/V-NM93CS66LZE/V		250 300		ns
t <sub>SKL</sub>	SK Low Time			250		ns
t <sub>SKS</sub>	SK Setup Time		SK Must Be at V <sub>IL</sub> for t <sub>SKS</sub> before CS goes high	50		ns
t <sub>CS</sub>	Minimum CS Low Time		(Note 2)	250		ns
t <sub>CSS</sub>	CS Setup Time			50		ns
t <sub>PRES</sub>	PRE Setup Time			50		ns
t <sub>PH</sub>	DO Hold Time			70		ns
t <sub>PES</sub>	PE Setup Time			50		ns
t <sub>DIS</sub>	DI Setup Time			100		ns
t <sub>CSH</sub>	CS Hold Time			0		ns
t <sub>PEH</sub>	PE Hold Time			250		ns
t <sub>PREH</sub>	PRE Hold Time			50		ns
t <sub>DIH</sub>	DI Hold Time			20		ns
t <sub>PD1</sub>	Output Delay to "1"				500	ns
t <sub>PD0</sub>	Output Delay to "0"				500	ns
t <sub>SV</sub>	CS to Status Valid				500	ns
t <sub>DF</sub>	CS to DO in TRI-STATE®		CS = V <sub>IL</sub>		100	ns
t <sub>WP</sub>	Write Cycle Time				10	ms

## Capacitance

$T_A = 25^\circ\text{C}$   $f = 1\text{ MHz}$

Symbol	Test	Max	Units
$C_{OUT}$	Output Capacitance	5	pF
$C_{IN}$	Input Capacitance	5	pF

**Note 1:** Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** CS (Chip Select) must be brought low (to  $V_{IL}$ ) for an interval of  $t_{CS}$  in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

**Note 3:** Typical leakage values are in the 20 nA range.

**Note 4:** The shortest allowable SK clock period =  $1/f_{SK}$  (as shown under the  $f_{SK}$  parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both  $t_{SKH}$  and  $t_{SKL}$  limits must be observed. Therefore, it is not allowable to set  $1/f_{SK} = t_{SKH}(\text{minimum}) + t_{SKL}(\text{minimum})$  for shorter SK cycle time operation.

## AC Test Conditions

$V_{CC}$ Range	$V_{IL}/V_{IH}$ Input Levels	$V_{IL}/V_{IH}$ Timing Level	$V_{OL}/V_{OH}$ Timing Level	$I_{OL}/I_{OH}$
$2.7\text{V} \leq V_{CC} < 4.5\text{V}$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	$\pm 10\ \mu\text{A}$
$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	- 2.1 mA/0.4 mA

Output Load: 1 TTL Gate ( $C_L = 100\text{ pF}$ )

## Functional Description

The extended voltage EEPROMs of the NM93CSxxLZ Family have 10 instructions as described below. Note that MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the CS06 and CS46 the next 8 bits carry the op code and the 6-bit address for register selection. For the CS56 and CS66, the next 10 bits carry the op code and the 8-bit address for register selection. All Data In signals are clocked into the device on the low-to-high SK transition.

### Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **Sequential Read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

### Write Enable (WEN):

When  $V_{CC}$  is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or  $V_{CC}$  is removed from the part.

### Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is allocated to the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the  $t_{CS}$  interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and that the part is ready for another instruction.

### Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". As in the WRITE mode, the D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the  $t_{CS}$  interval. This function is **DISABLED** if the protect register is in use to lock out a section memory.

### Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: For all protect register operations: If the PRE pin is not held at  $V_{IH}$ , all instructions will be applied to the EEPROM array, rather than the Protect Register.

### Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the D0 pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

### Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

### Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and therefore enables all registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence; however, after loading the PRCLEAR instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will **PREVENT** the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming op-code.

### Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction, the Protect Register **must** first be cleared by executing a PRCLEAR operation and the PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

### Protect Register Disable (PRDS):

The PRDS instruction is a **ONE TIME ONLY** instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

### Instruction Set for the NM93CS06LZ and NM93CS46LZ

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5-A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5-A0	D15-D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15-D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5-A0		1	1	Programs address into Protect Register. Thereafter, memory addresses $\geq$ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	<b>ONE TIME ONLY</b> instruction after which the address in the Protect Register cannot be altered.

**Note:** Address bits A5 and A4 become "Don't Care" for the NM93CS06LZ.

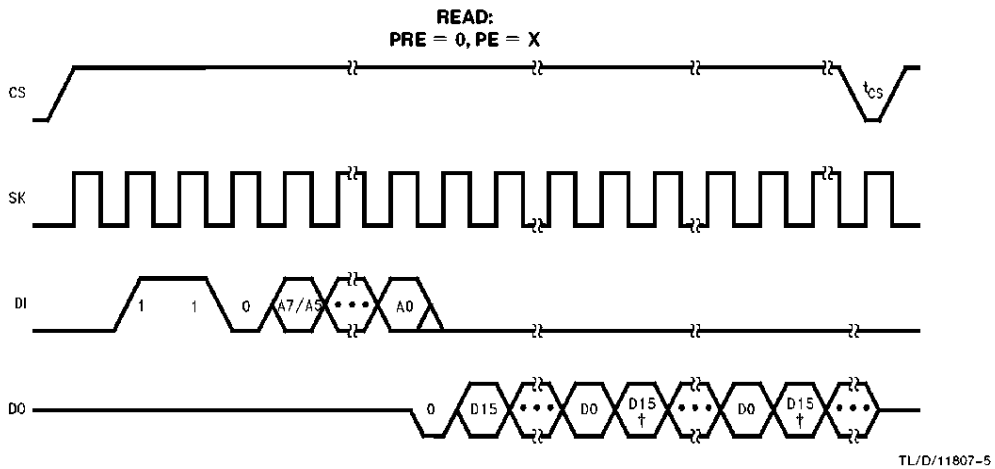
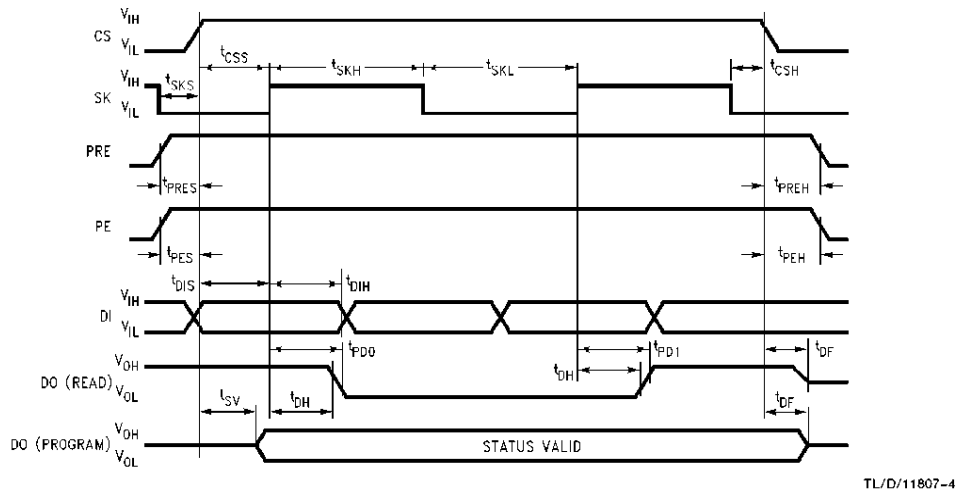
### Instruction Set for the NM93CS56LZ and NM93CS66LZ

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7-A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7-A0	D15-D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15-D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7-A0		1	1	Programs address into Protect Register. Thereafter, memory addresses $\geq$ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	<b>ONE TIME ONLY</b> instruction after which the address in the Protect Register cannot be altered.

**Note:** Address bit A7 becomes "Don't Care" for the NM93CS56LZ.

## Timing Diagrams

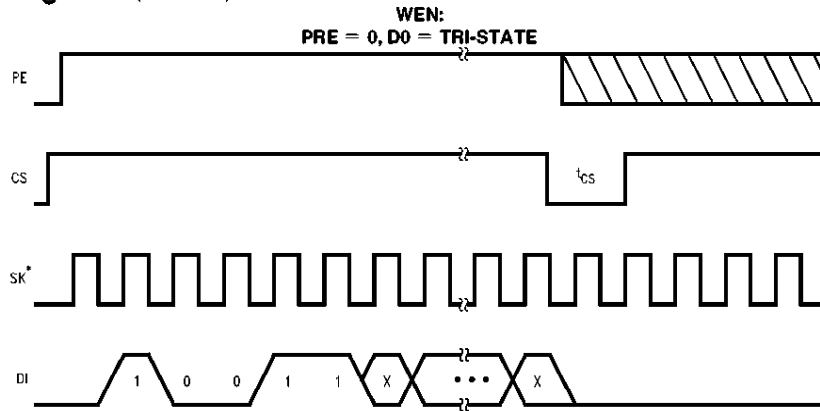
### Synchronous Data Timing



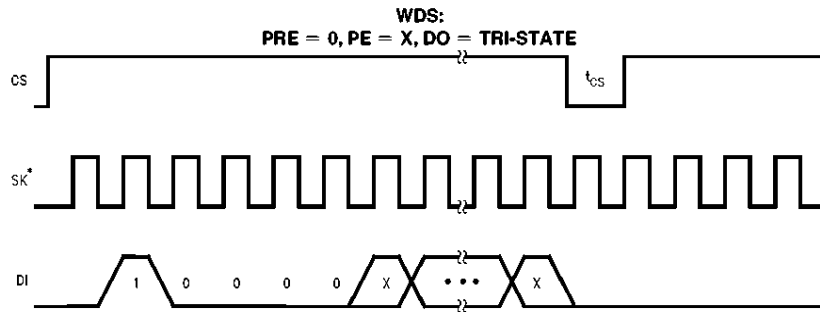
<sup>†</sup>Sequential read is possible when CS is held high. The device will automatically cycle to the next register and output sequentially.



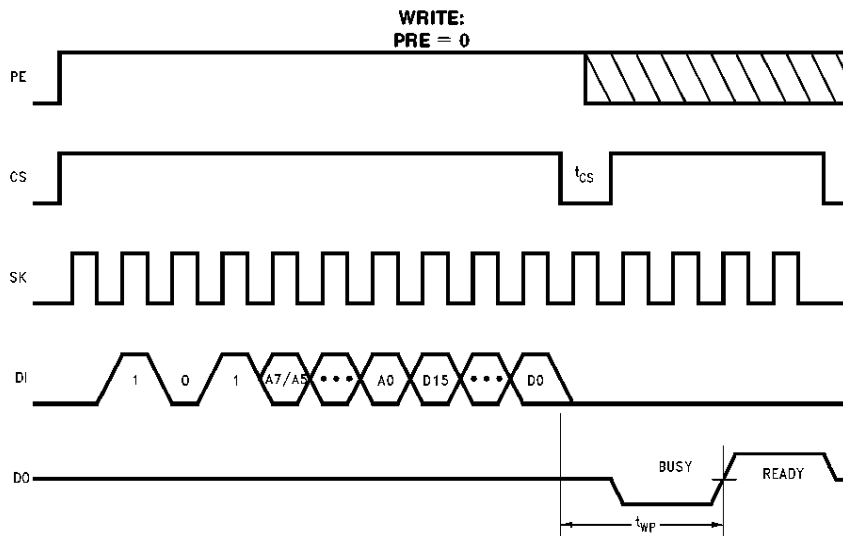
**Timing Diagrams** (Continued)



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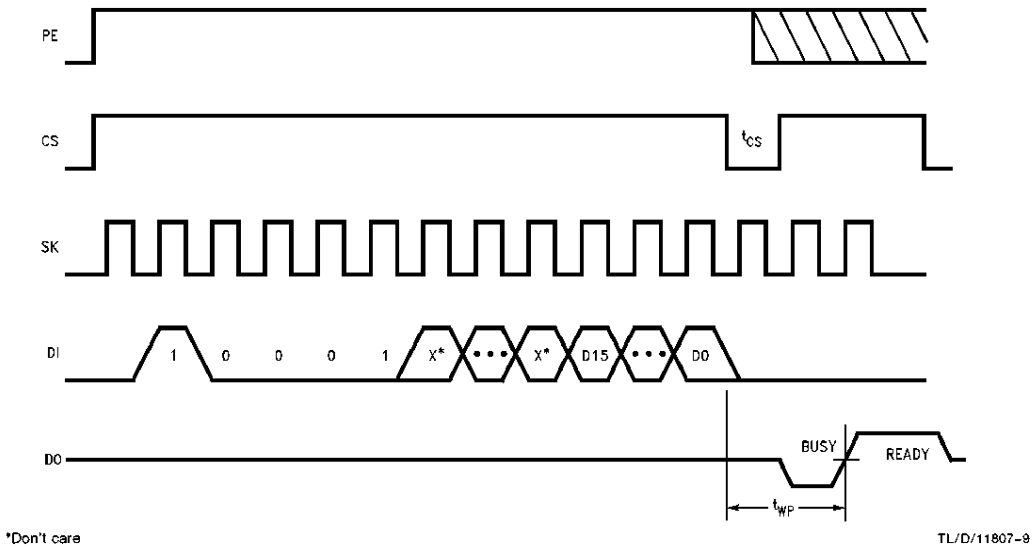
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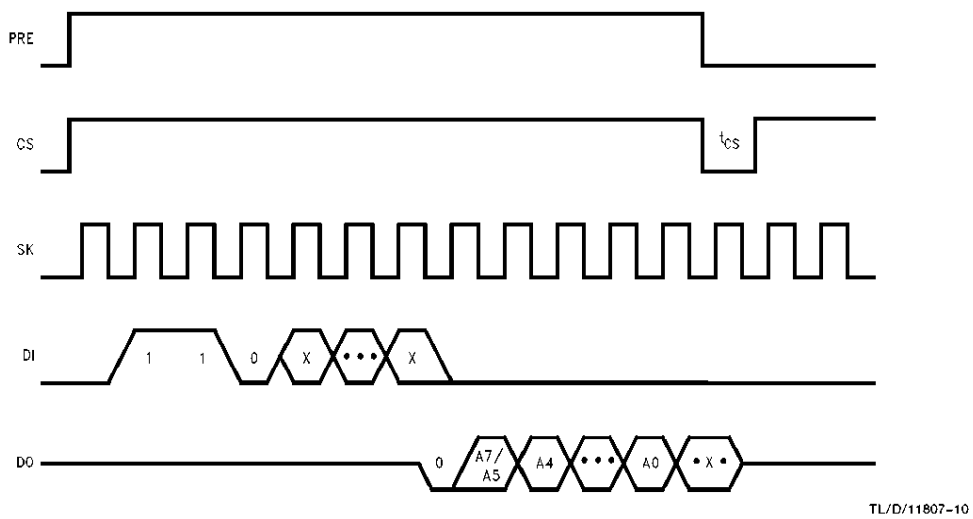
TL/D/11807-8

## Timing Diagrams (Continued)

**WRALL:**  
**PRE = 0**  
**(PROTECT REGISTER MUST BE CLEARED)**

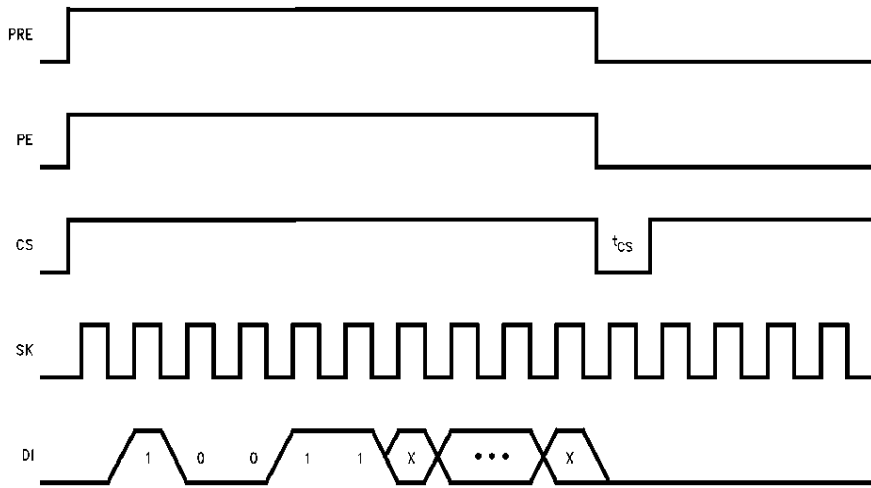


**PRREAD:**  
**PE = X**



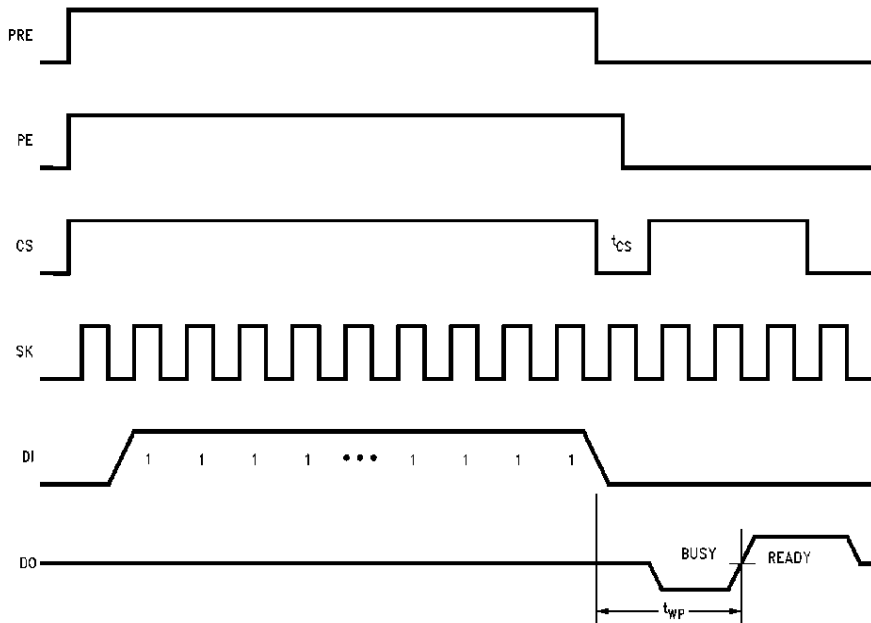
**Timing Diagrams** (Continued)

**PREN:**  
**D0 = TRI-STATE**  
**(A WEN CYCLE MUST PRECEDE A PREN CYCLE)**



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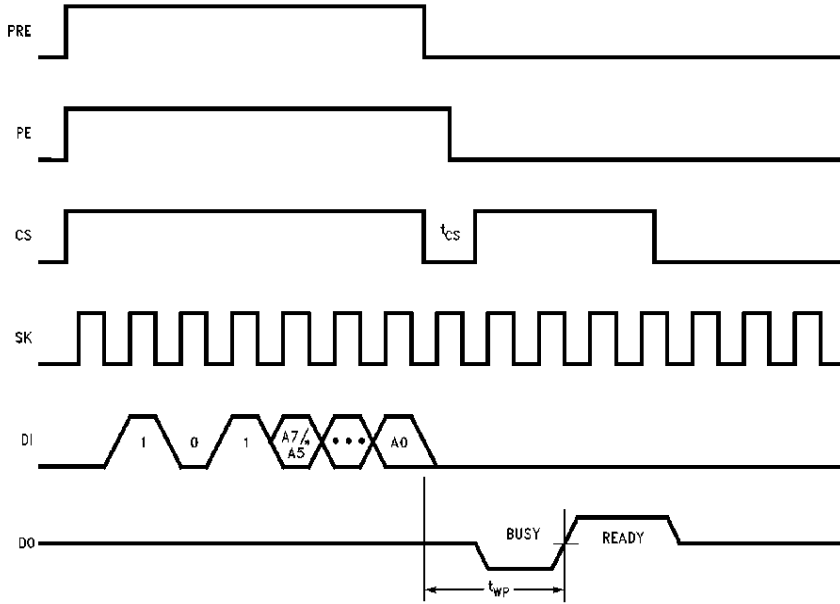
**PRCLEAR:**  
**(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)**



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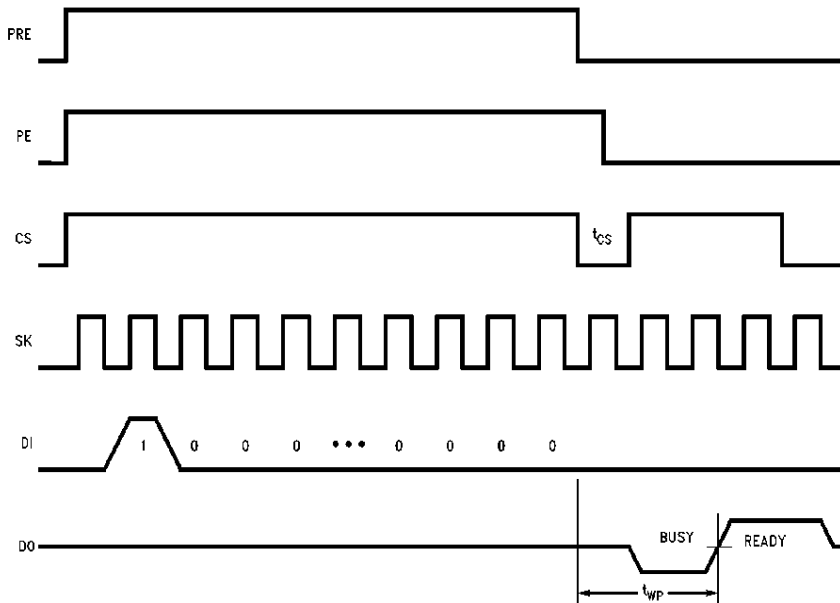
**Timing Diagrams** (Continued)

**PRWRITE<sup>†</sup>:**  
**(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)**



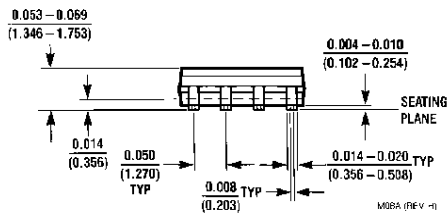
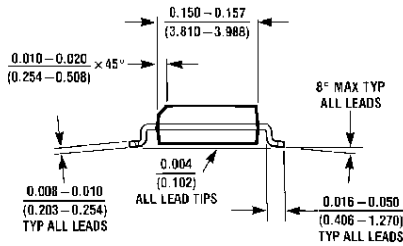
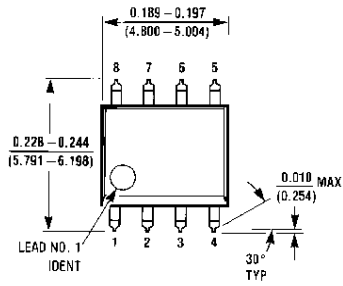
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**PRDS:**  
**(ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)**

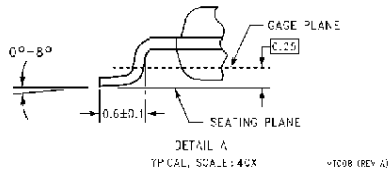
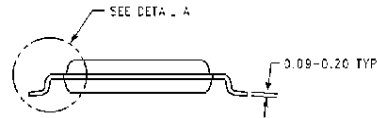
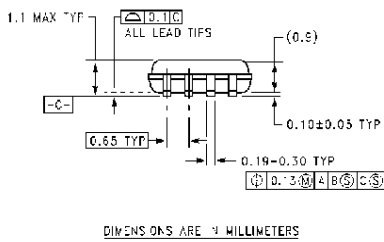
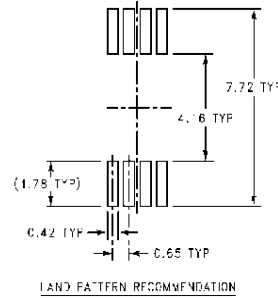
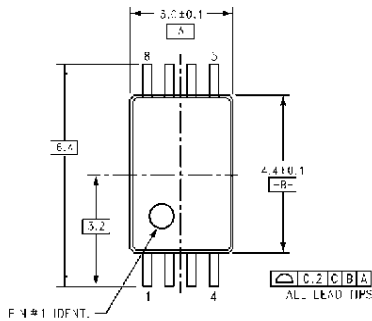


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**Physical Dimensions** inches (millimeters) unless otherwise noted



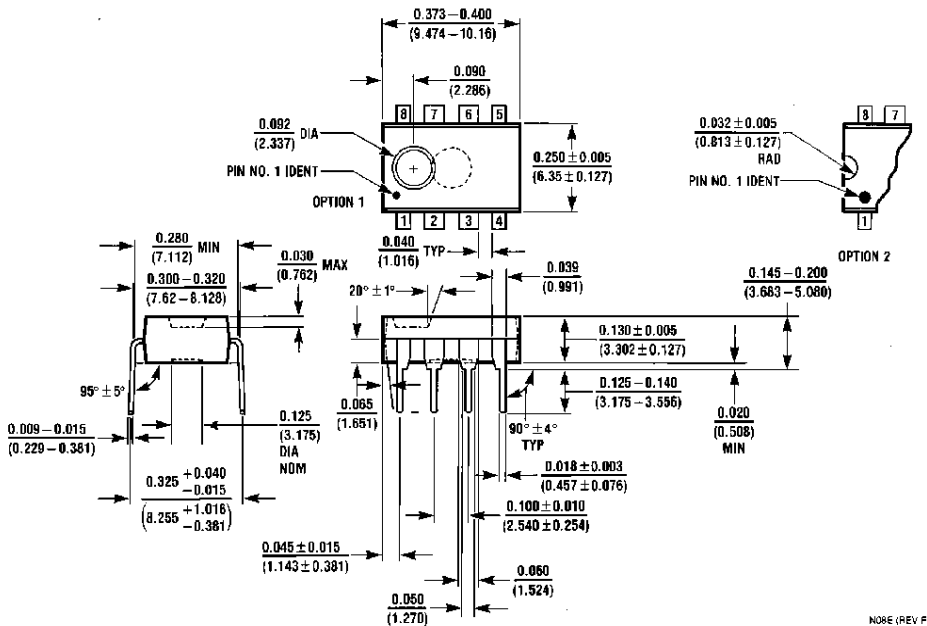
**Molded Small Out-Line Package (M8)**  
NS Package Number M08A



**8-Pin Molded TSSOP, JEDEC (MT8)**  
NS Package Number MTC08

**NM93CS06LZ/CS46LZ/CS56LZ/CS66LZ 256-/1024-/4096-Bit Serial EEPROM  
with Extended Voltage (2.7V to 5.5V) and Data Protect (MICROWIRE Bus Interface)**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Molded Dual-In-Line Package (N)  
NS Package Number N08E**

NOTE (REV F)

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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