SRAM

32K x 8 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V* power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards
- Commercial temperature range (0°C to +70°C)

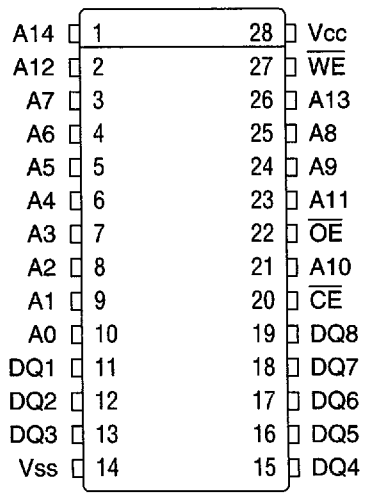
OPTIONS — MARKING

- Timing
  - 12ns access — -12*
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic SOJ (300 mil) — DJ
- Part Number Example: MT5LC2568DJ-15 L

*Vcc = +3.3V ±0.165V

PIN ASSIGNMENT (Top View)

28-Pin SOJ
(SC-1)



GENERAL DESCRIPTION

The MT5LC2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to technical note TN-05-16, "A Designer's Guide to 3.3V SRAMs," for further information.

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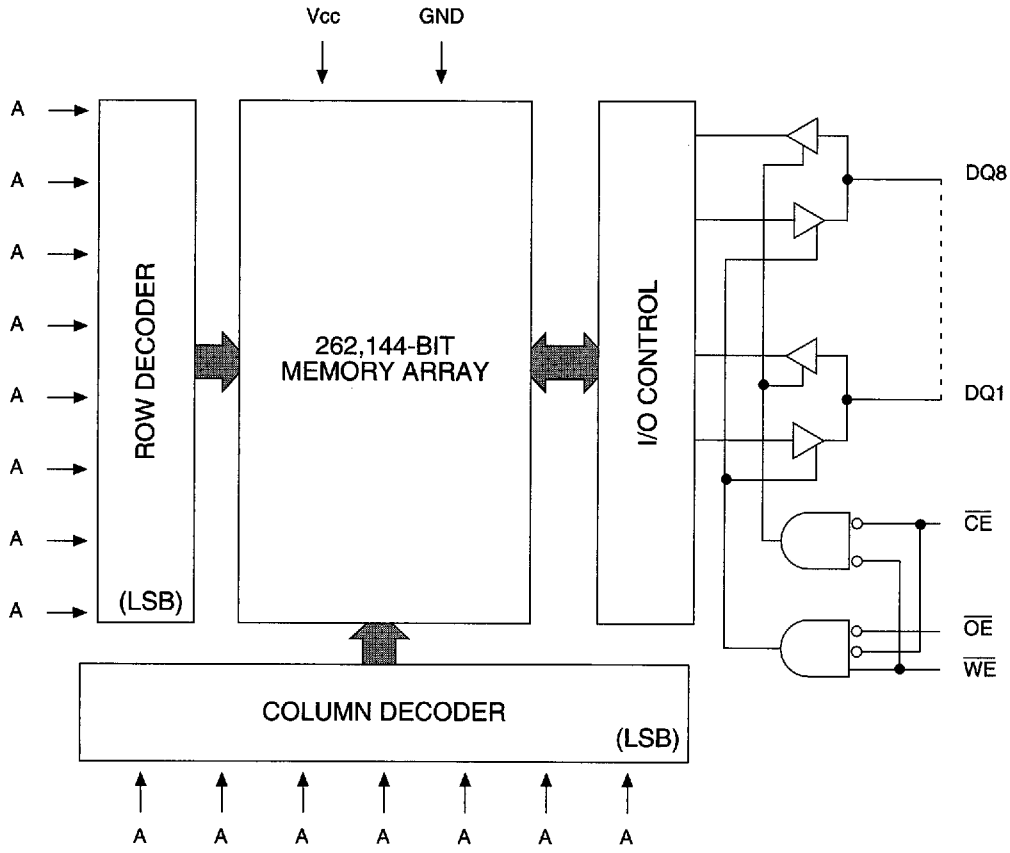
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Note 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage	15, 20 and 25ns	V_{CC}	3.0	3.6	V	1
Supply Voltage	12ns	V_{CC}	3.135	3.465	V	1, 15

				MAX					
DESCRIPTION	CONDITIONS	SYM	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = $1/^tRC$	I_{CC}	75	125	110	95	90	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = $1/^tRC$	I_{SB1}	17	35	30	25	25	mA	13
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	1.0	3	3	3	3	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	SYM	-12*		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	tRC	12		15		20		25		ns	
Address access time	tAA		12		15		20		25	ns	
Chip Enable access time	tACE		12		15		20		25	ns	
Output hold from address change	tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		3		3		ns	7
Chip Disable to output in High-Z	tHZCE		6		8		9		9	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		ns	4
Chip Disable to power-down time	tPD		12		15		20		25	ns	4
Output Enable access time	tAOE		6		7		8		8	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		ns	
Output Disable to output in High-Z	tHZOE		6		6		7		7	ns	6
WRITE Cycle											
WRITE cycle time	tWC	12		15		20		25		ns	
Chip Enable to end of write	tCW	8		10		12		15		ns	
Address valid to end of write	tAW	8		10		12		15		ns	
Address setup time	tAS	0		0		0		0		ns	
Address hold from end of write	tAH	1		1		1		1		ns	
WRITE pulse width	tWP1	8		10		12		15		ns	
WRITE pulse width	tWP2	12		12		15		15		ns	
Data setup time	tDS	7		8		10		10		ns	
Data hold time	tDH	0		0		0		0		ns	
Write Disable to output in Low-Z	tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	tHZWE		6		7		8		10	ns	6, 7

*Vcc = 3.3V ±0.165V

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AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

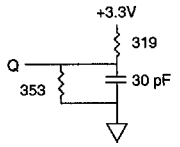


Fig. 1 OUTPUT LOAD EQUIVALENT

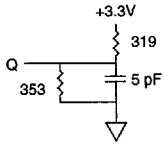


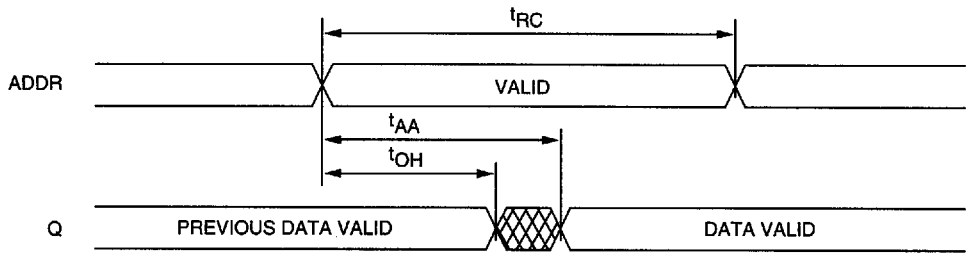
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

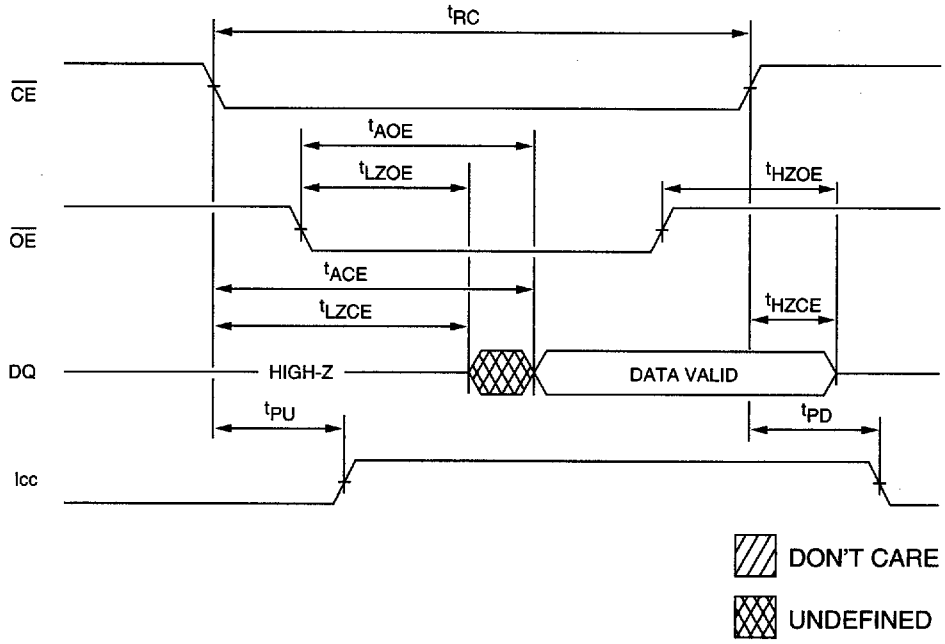
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200ms$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. V_{CC} is 3.3V ±0.3V for the 15, 20 and 25ns speed grades and 3.3V ±0.165V for the 12ns speed grade.

SRAM

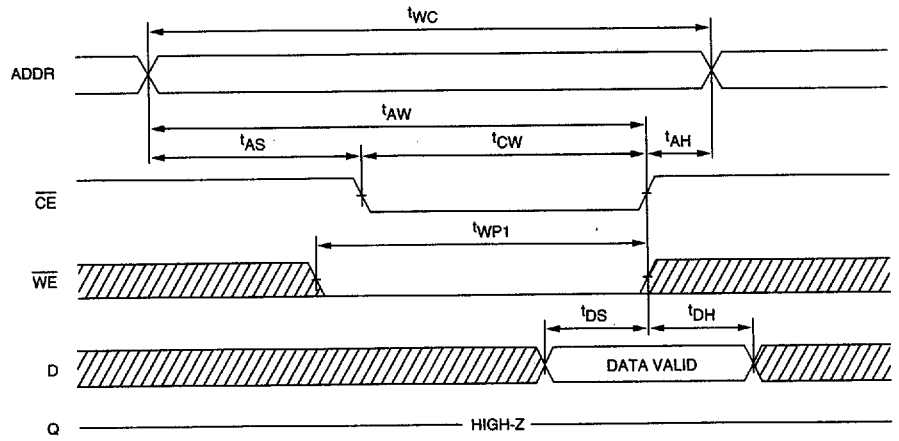
READ CYCLE NO. 1 [8, 9]



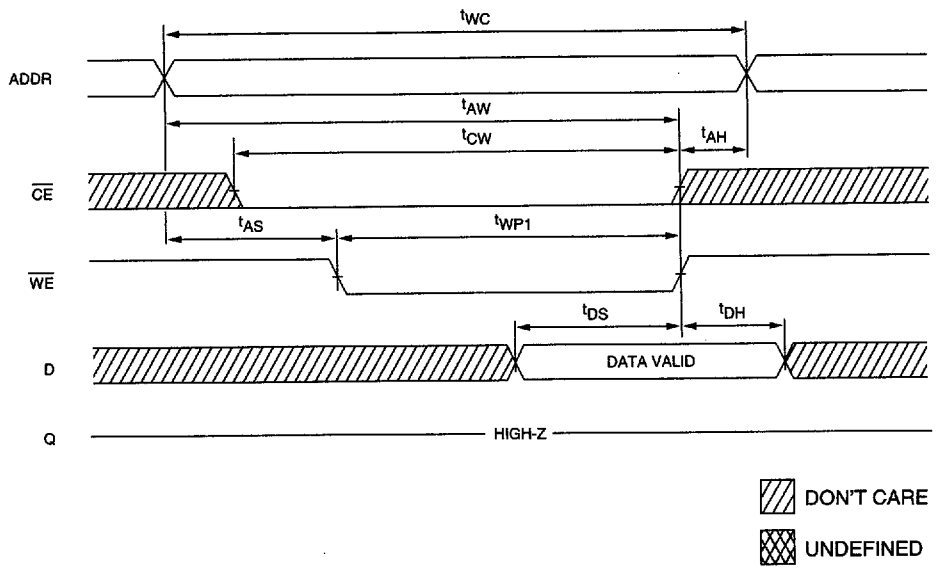
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

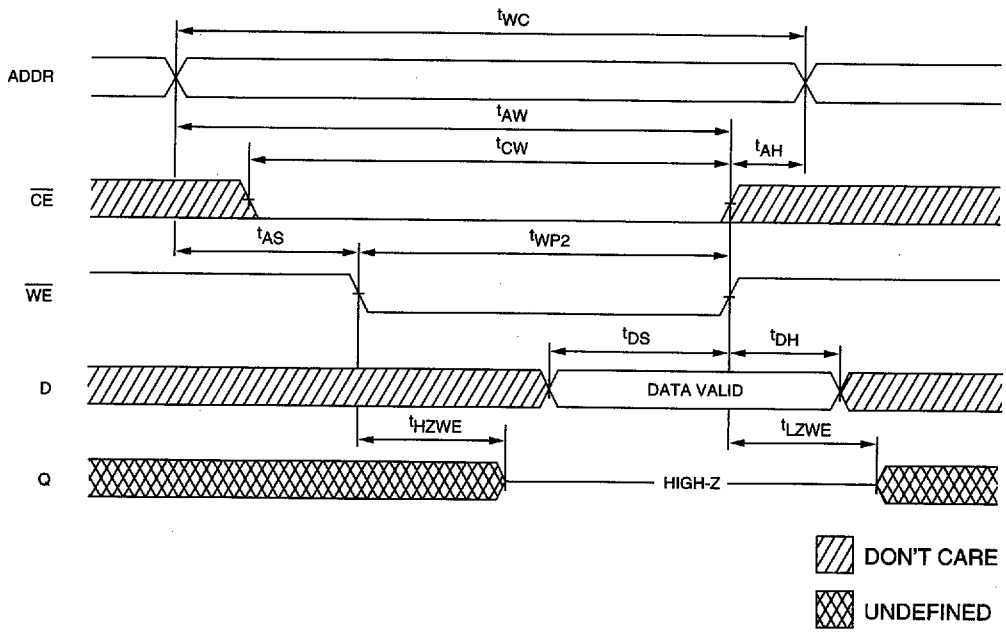


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

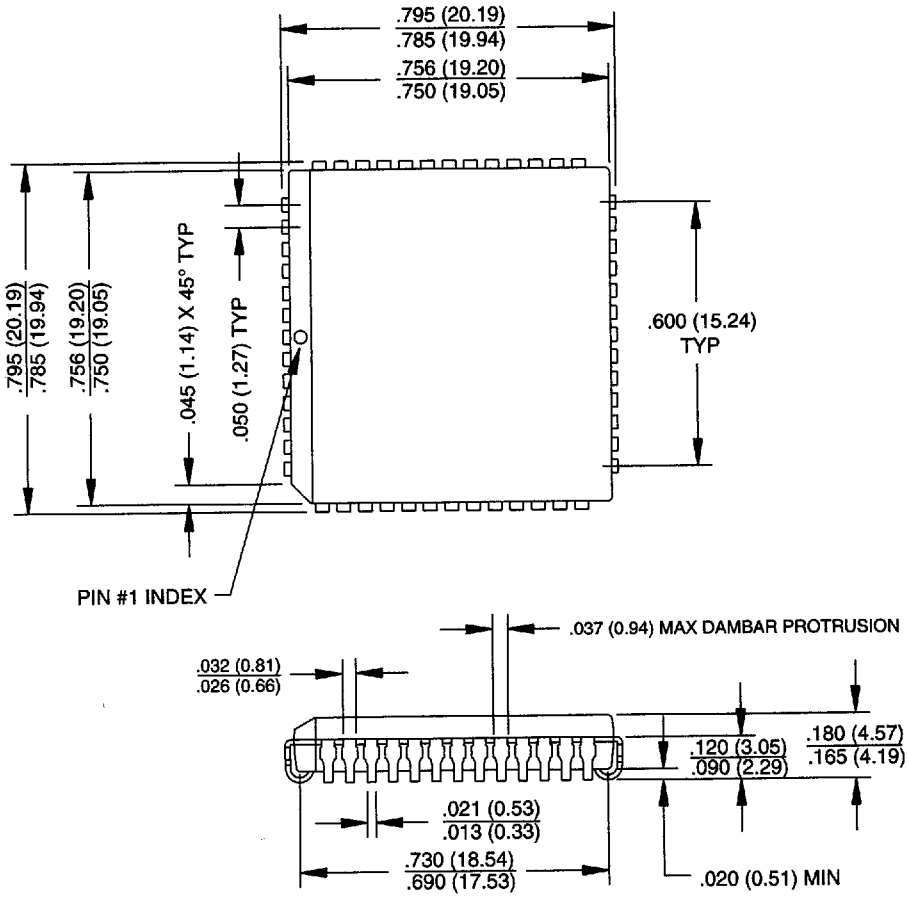
WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

52-PIN PLCC

SA-1



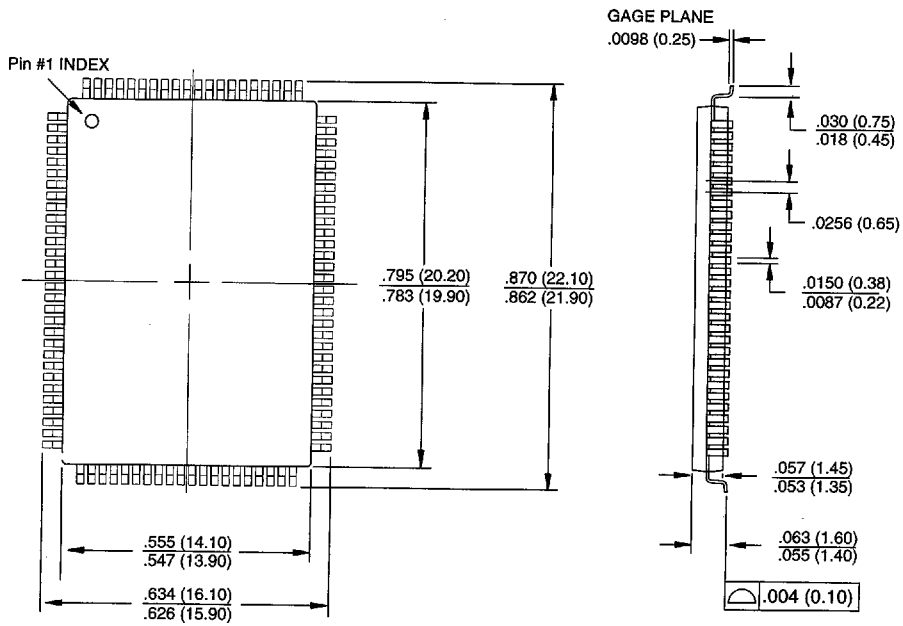
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

PACKAGE INFORMATION

100-PIN TQFP

SB-1



PACKAGE INFORMATION

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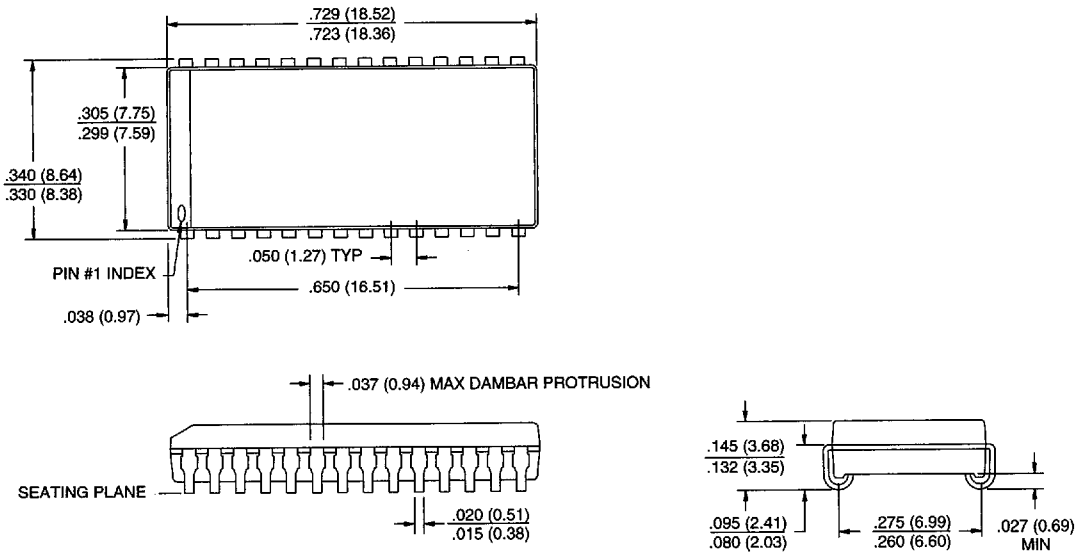
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SC-1

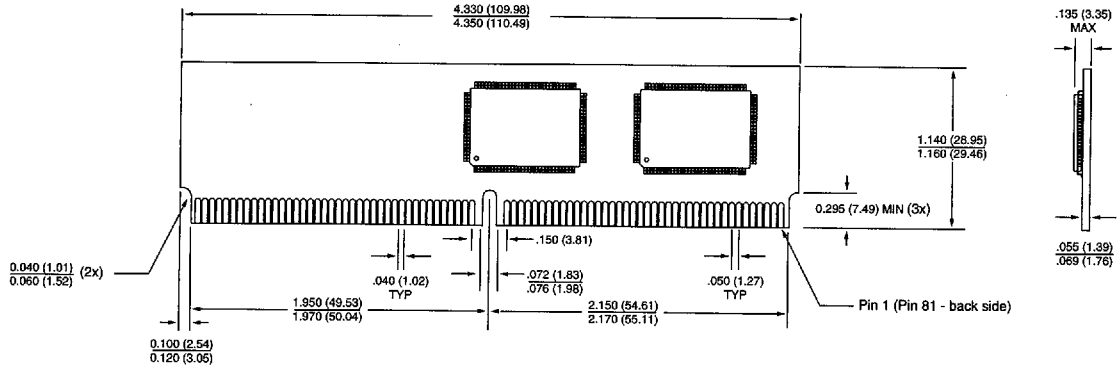


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

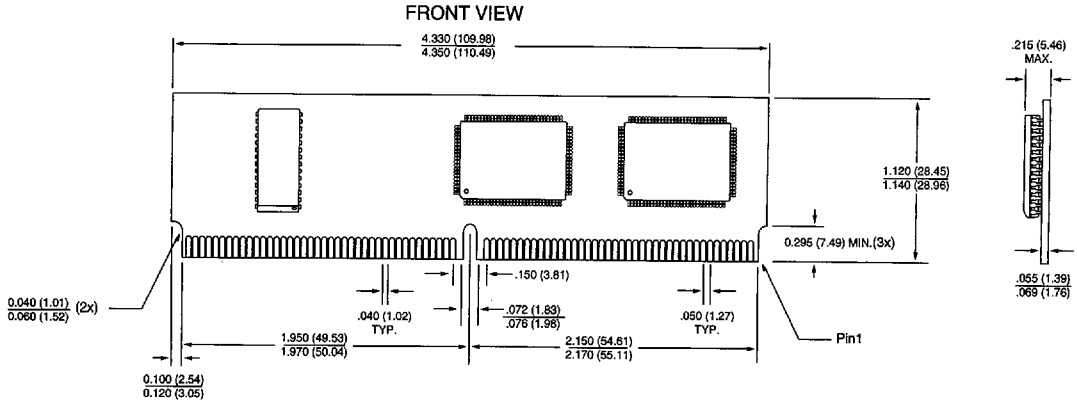
160-PIN MODULE DIMM

SD-1



160-PIN MODULE DIMM

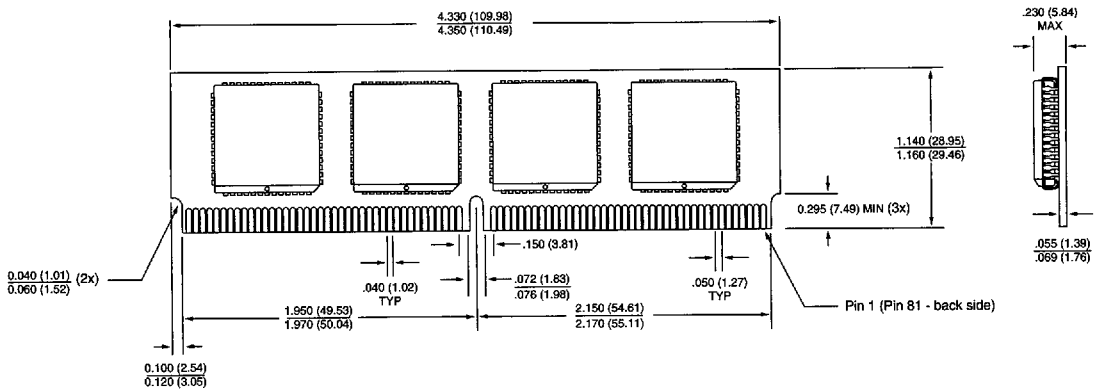
SD-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

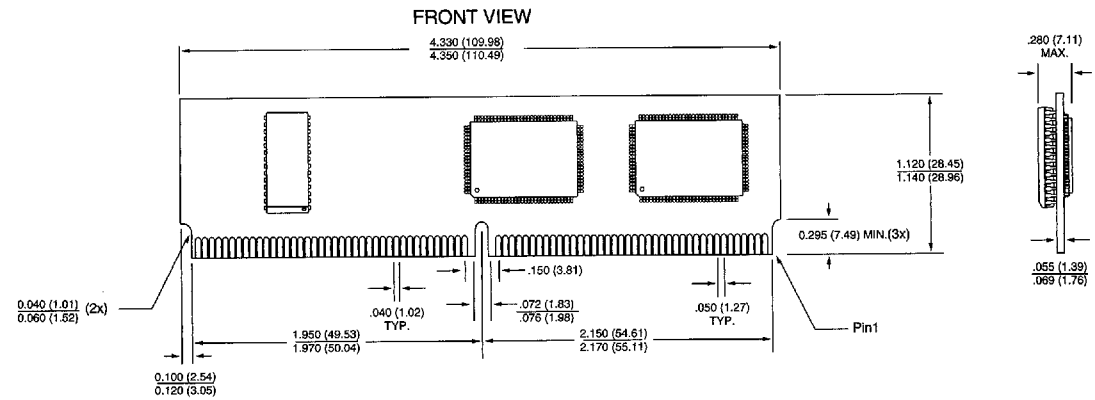
160-PIN MODULE DIMM

SD-3



160-PIN MODULE DIMM

SD-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION