GENERAL SEMICONDUCTOR®

GF2301

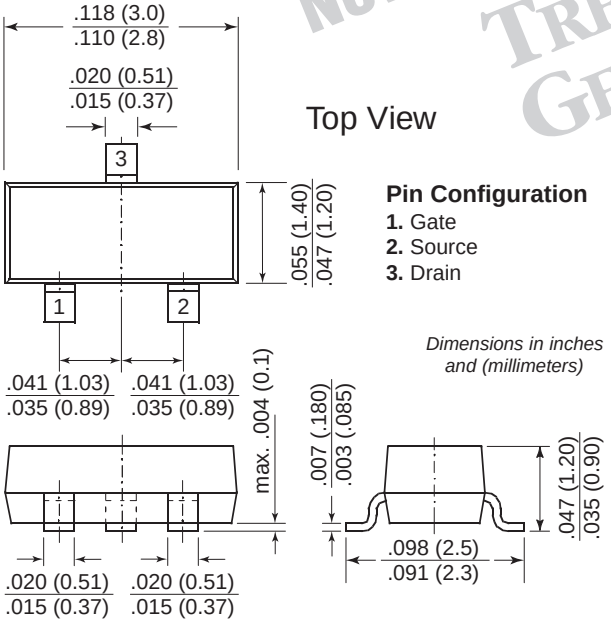
P-Channel Enhancement-Mode MOSFET

Low $V_{GS(th)}$ **V_{DS}** -20V **$R_{DS(ON)}$** 0.13Ω **I_D** -2.3A

TO-236AB (SOT-23)

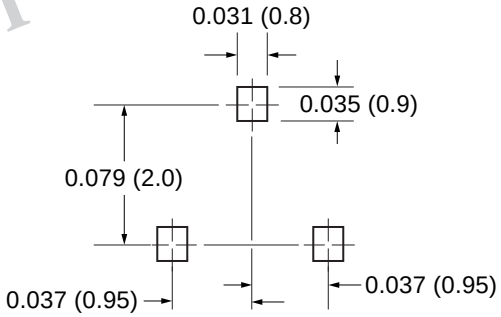
New Product

TRENCH GENFET®



Pin Configuration
1. Gate
2. Source
3. Drain

Dimensions in inches and (millimeters)



Mounting Pad Layout

Mechanical Data

Case: SOT-23 Plastic Package
Weight: approx. 0.008g
Marking Code: 01

Features

- Advanced Trench Process Technology
- High density cell design for ultra-low on-resistance
- Popular SOT-23 package with copper lead frame for superior thermal and electrical capabilities
- Compact and low profile
- –2.5V rated

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–20	V
Gate-Source-Voltage		V_{GS}	±8	V
Continuous Drain Current T_J = 150°C	T_A = 25°C T_A = 70°C	I_D	–2.3 –1.5	A
Pulsed Drain Current (1)		I_{DM}	–10	A
Maximum Power Dissipation (2)	T_A = 25°C T_A = 70°C	P_D	1.25 0.8	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to +150	°C
Maximum Junction-to-Ambient Thermal Resistance(2)		$R_{\theta JA}$	100	°C/W

Note:
(1) Pulse width limited by maximum junction temperature.
(2) Surface mounted on FR4 board, t ≤ 5 sec.

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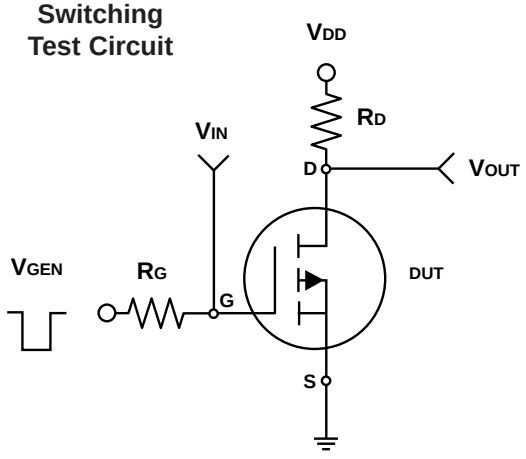
Electrical Characteristics (T_J = 25°C unless otherwise noted)

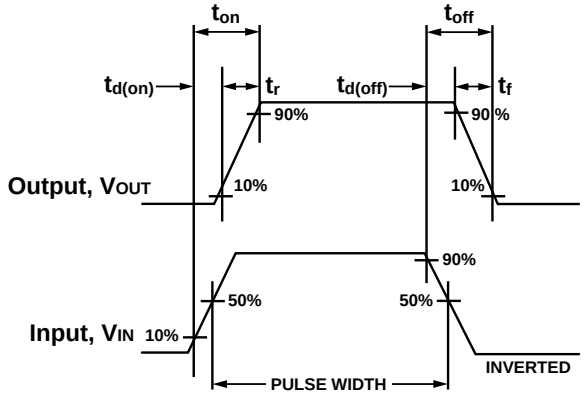
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = –250μA	–20	—	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250μA	–0.45	—	—	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±8V	—	—	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –16V, V_{GS} = 0V	—	—	–1.0	μA
		V_{DS} = –16V, V_{GS} = 0V, T_J = 55°C	—	—	–10	
On-State Drain Current[1]	$I_{D(on)}$	V_{DS} ≤ –5V, V_{GS} = –4.5V	–6	—	—	A
		V_{DS} ≤ –5V, V_{GS} = –2.5V	–3	—	—	
Drain-Source On-State Resistance[1]	$R_{DS(on)}$	V_{GS} = –4.5V, I_D = –2.8A	—	95	130	mΩ
		V_{GS} = –2.5V, I_D = –2.0A	—	122	190	
Forward Transconductance[1]	g_{fs}	V_{DS} = –5V, I_D = –2.8A	—	6.5	—	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = –6V, V_{GS} = –4.5V I_D = –2.8A	—	5.4	10	nC
Gate-Source Charge	Q_{gs}		—	0.8	—	
Gate-Drain Charge	Q_{gd}		—	1.1	—	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –6V, R_L = 6Ω I_D ≈ –1A, V_{GEN} = –4.5V R_G = 6Ω	—	5	25	ns
Rise Time	t_r		—	19	60	
Turn-Off Delay Time	$t_{d(off)}$		—	95	110	
Fall Time	t_f		—	65	80	
Input Capacitance	C_{iss}	V_{DS} = –6V, V_{GS} = 0V f = 1.0MHz	—	447	—	pF
Output Capacitance	C_{oss}		—	124	—	
Reverse Transfer Capacitance	C_{rss}		—	80	—	
Source-Drain Diode						
Maximum Diode Forward Current	I_S	—	—	—	–1.6	A
Diode Forward Voltage	V_{SD}	I_S = –1.6A, V_{GS} = 0V	—	–0.8	–1.2	V

Note:
(1) Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%

Switching Test Circuit



Switching Waveforms



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Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

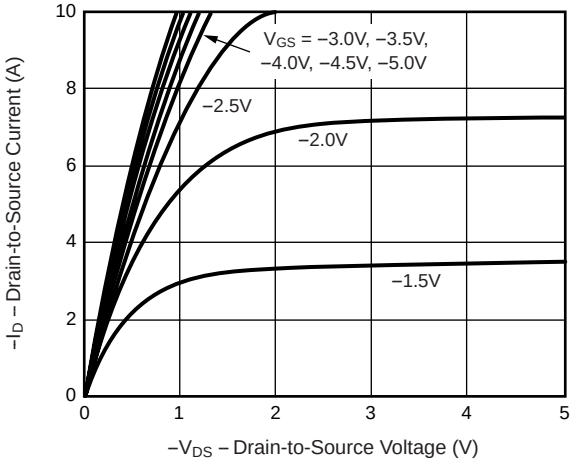

Fig. 2 – Transfer Characteristics

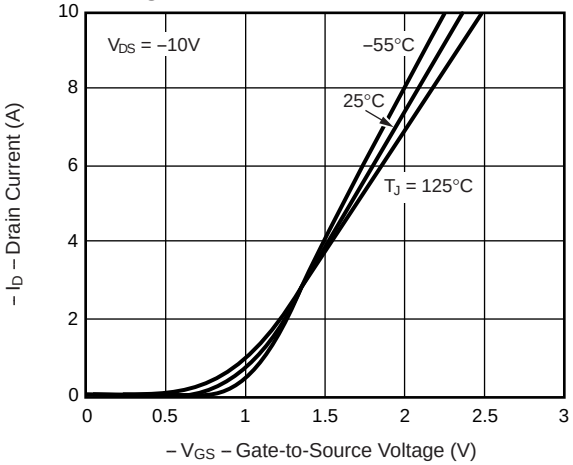

Fig. 3 – Threshold Voltage vs. Temperature

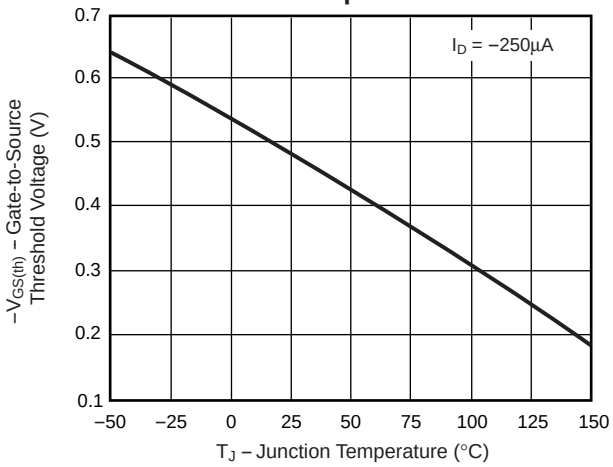

Fig. 4 – On-Resistance vs. Drain Current

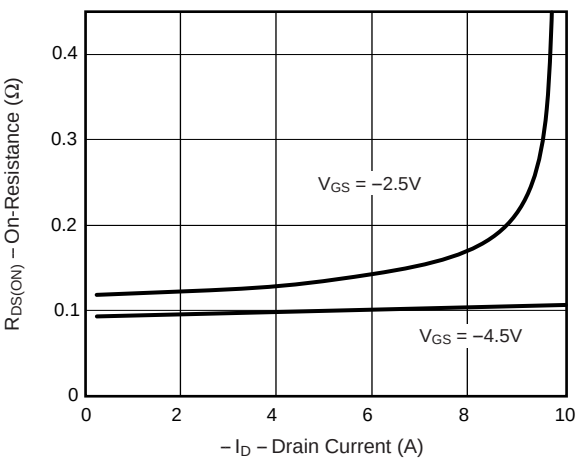

Fig. 5 – On-Resistance vs. Junction Temperature

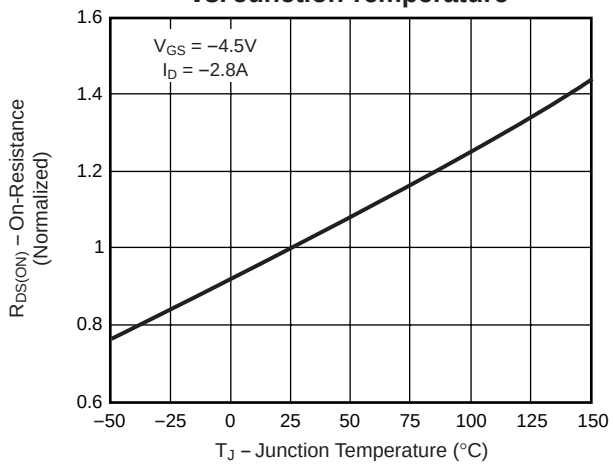

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

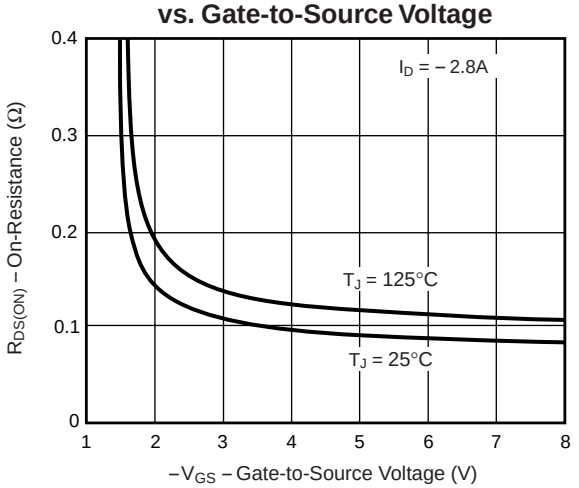

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Fig. 7 – Gate Charge

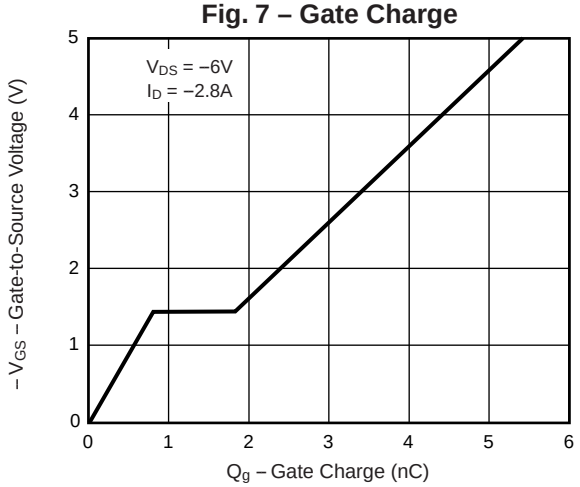

Fig. 8 – Capacitance

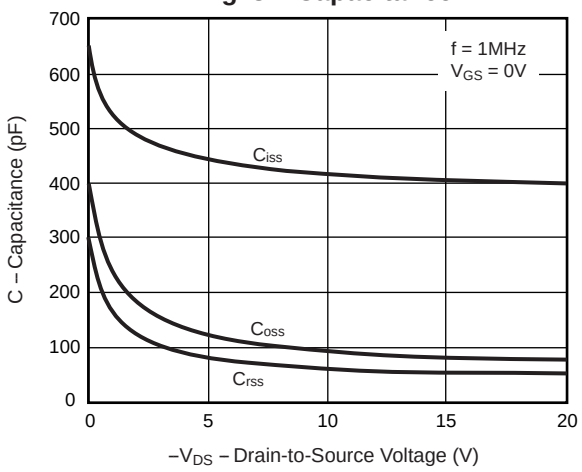

Fig. 9 – Source-Drain Diode Forward Voltage

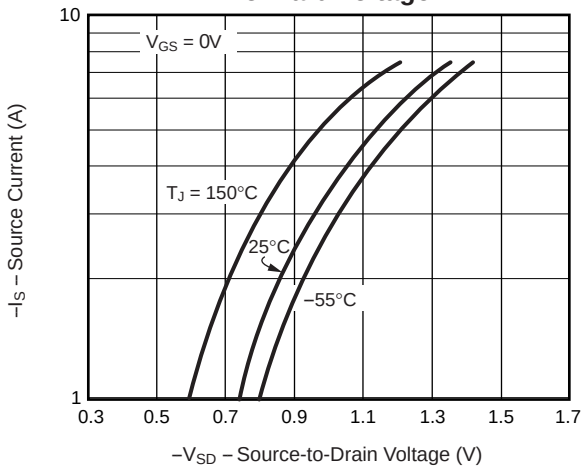

Fig. 10 – Thermal Impedance

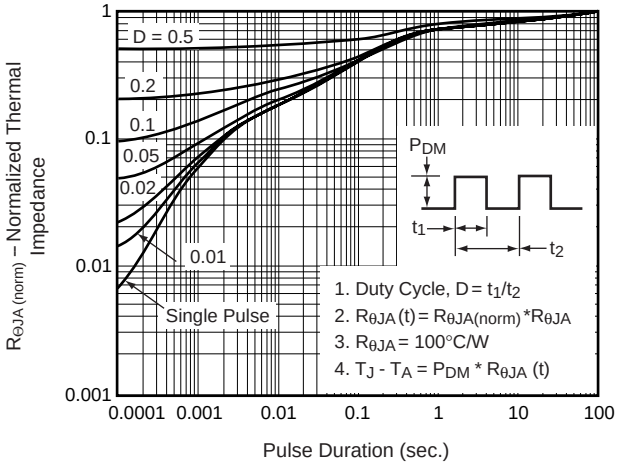

Fig. 11 – Power vs. Pulse Duration

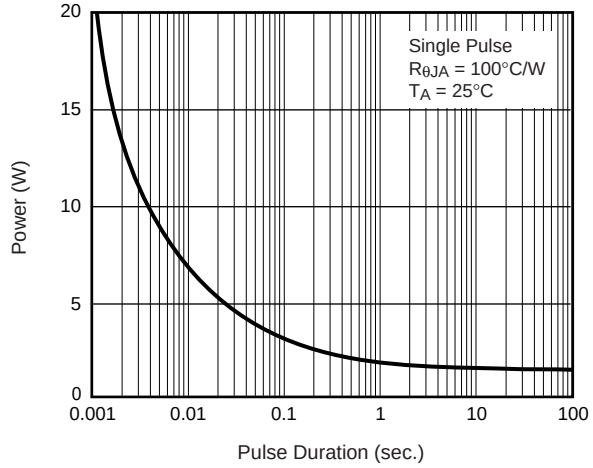

Fig. 12 – Maximum Safe Operating Area