HARRIS **HM-65162/883**

June 1989

2K x 8 Asynchronous CMOS Static RAM

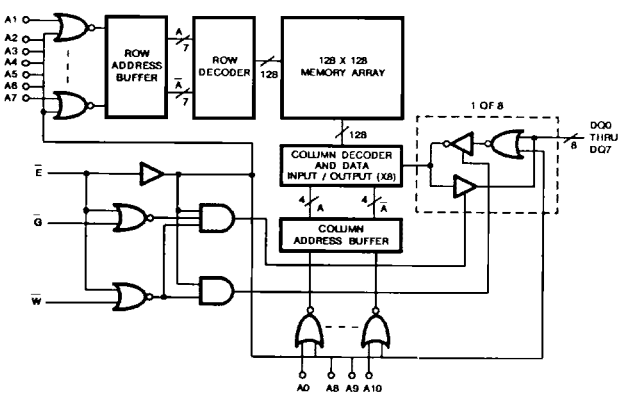
Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Access Time..... 70/90ns Max**
- **Low Standby Current..... 50µA Max**
- **Low Operating Current ..... 70mA Max**
- **Data Retention at 2.0 Volts..... 20µA Max**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout (2716, 6116 Type)**
- **No Clocks or Strobes Required**
- **Wide Temperature Range.....-55°C to +125°C**
- **Equal Cycle and Access Time**
- **Single 5 Volt Supply**
- **Gated Inputs—No Pull-Up or Pull-Down Resistors Required**

Description

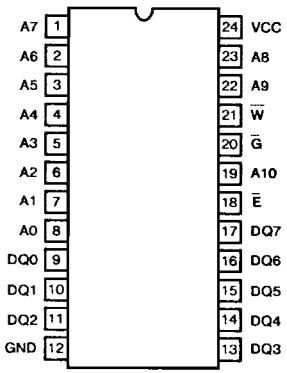
The HM-65162/883 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin DIP, and 32 pad 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162/883 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Functional Diagram

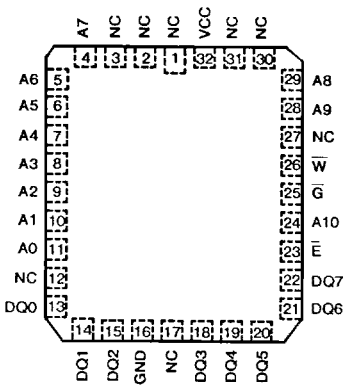


Pinouts

HM1-65162/883 (CERAMIC DIP)
TOP VIEW



HM4-65162/883 (CERAMIC LCC)
TOP VIEW



PIN NAMES

PIN	DESCRIPTION
NC	No Connect
A0 - A10	Address Input
$\overline{E}$	Chip Enable/Power Down
VSS/GND	Ground
DQ0 - DQ7	Data In/Data Out
VCC	Power (+5V)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

3 CMOS MEMORY

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND-0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Operating Temperature Range (T_A) ..... -55°C to +125°C
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns Max

TABLE 1. HM-65162/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	-55°C≤T_A≤+125°C	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	-55°C≤T_A≤+125°C	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	-55°C≤T_A≤+125°C	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	100	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	-55°C≤T_A≤+125°C	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3	-55°C≤T_A≤+125°C	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	-55°C≤T_A≤+125°C	-	40	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	-55°C≤T_A≤+125°C	-	-	-

TABLE 2. HM-65162/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	90	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	90	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C		65	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	-	90	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	65	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	55	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	-55°C≤T_A≤+125°C	15	-	ns

CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

TABLE 3. HM-65162/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6,8	+25°C	-	10	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6,9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6,8	+25°C	-	12	pF
		VCC = Open, F = 1MHz, All Measurements Referenced To Device Grounds	6,9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	0	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	50	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	-	40	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55°C \leq T_A \leq +125°C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55°C \leq T_A \leq +125°C$	VCC -0.4V	-	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5004	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) ..... -55°C to +125°C
Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns (Max)

TABLE 1. HM65162B/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-1.0	1.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-1.0	1.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	50	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3,	$-55^oC \leq T_A \leq +125^oC$	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55^oC \leq T_A \leq +125^oC$	-	20	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55^oC \leq T_A \leq +125^oC$	-	-	-

TABLE 2. HM-65162B/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	70	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	50	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	-	70	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	45	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	50	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	40	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55^oC \leq T_A \leq +125^oC$	10	-	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-65162B/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 8	+25°C	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Refernced to Device Ground	6, 9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	6, 8	+25°C	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	35	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	35	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^{o}C \leq T_A \leq +125^{o}C$	VCC -0.4V	-	V

NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C &D	Samples/5005	1, 7, 9

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input or Output Voltage Applied for all grades ..... GND -0.3V to VCC+0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Junction Temperature ..... +175°C
Typical Derating Factor ..... 5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	48°C/W	8°C/W
Ceramic LCC Package	85°C/W	40°C/W

Maximum Package Power Dissipation at +125°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 0.58W
Gate Count ..... 26000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) ..... -55°C to +125°C
Operating Supply Voltage (VCC) ..... 4.5V to 5.5V
Input Low Voltage (VIL) ..... 0V to +0.8V
Input High Voltage (VIH) ..... +2.2V to VCC
Data Retention Supply Voltage ..... 2.0V to 4.5V
Input Rise and Fall Times ..... 40ns (Max)

TABLE 1. HM-65162C/883 D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH1	VCC = 4.5V, IO = -1.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	2.4	-	V
Low Level Output Voltage	VOL	VCC = 4.5V, IO = 4.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IIOZ	VCC = 5.5V, $\overline{G}$ = 2.2V, or $\overline{E}$ = 2.2V VI/O = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-5.0	5.0	µA
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55°C \le T_A \le +125°C$	-5.0	5.0	µA
Standby Supply Current	ICCSB1	VCC = 5.5V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	900	µA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 2.2V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	8	mA
Operating Supply Current	ICCOP	VCC = 5.5V, $\overline{G}$ = 5.5V, (Note 4), f = 1MHz, $\overline{E}$ = 0.8V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	70	mA
Enable Supply Current	ICCEN	VCC = 5.5V, IO = 0mA, $\overline{E}$ = 0.8V	1, 2, 3,	$-55°C \le T_A \le +125°C$	-	70	mA
Data Retention Supply Current	ICCDR	VCC = 2.0V, IO = 0mA, $\overline{E}$ = VCC -0.3V	1, 2, 3	$-55°C \le T_A \le +125°C$	-	300	µA
Functional Test	FT	VCC = 4.5V (Note 5)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

TABLE 2. HM-65162C/883 A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested

A.C. PARAMETERS	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Read/Write/Cycle Time	TAVAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	90	-	ns
Address Access Time	TAVQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	90	ns
Output Enable Access Time	TGLQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	65	ns
Chip Enable Access Time	TELQV	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	90	ns
Write Enable Read Setup Time	TWHAX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Address Setup Time	TAVWL	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	10	-	ns
Chip Selection to End of Write	TELWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Write Enable Pulse Setup Time	TWLEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Chip Enable Data Setup Time	TDVEH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Address Valid to End of Write	TAVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	65	-	ns
Write Enable Pulse Write	TWLWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	55	-	ns
Data Setup Time	TDVWH	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	30	-	ns
Data Hold Time	TWHDX	VCC = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	15	-	ns

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. HM-65162C/883 ELECTRICAL PERFORMANCE CHARACTERISTICS, A.C. AND D.C. (NOTE 6)

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 8	+25°C	-	10	pF
		VCC = Open, f = 1MHz, All Measurements Refernced to Device Ground	6, 9	+25°C	-	8	pF
I/O Capacitance	CI/O	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	6, 8	+25°C	-	12	pF
		VCC = Open, f = 1MHz All Measurements Referenced to Device Ground	6, 9	+25°C	-	10	pF
Write Enable to Output in High Z	TWLQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Write Enable High to Output ON	TWHQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	0	-	ns
Chip Enable to Output ON	TELQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output Enable to Output ON	TGLQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Chip Enable High to Output ON	TEHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	50	ns
Output Disable to Output in High Z	TGHQZ	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	-	40	ns
Output Hold from Address Change	TAVQX	VCC = 4.5V and 5.5V	6	$-55^{o}C \leq T_A \leq +125^{o}C$	5	-	ns
Output High Voltage	VOH2	VCC = 4.5V, IO = -100µA	6	$-55^{o}C \leq T_A \leq +125^{o}C$	VCC -0.4V	-	V

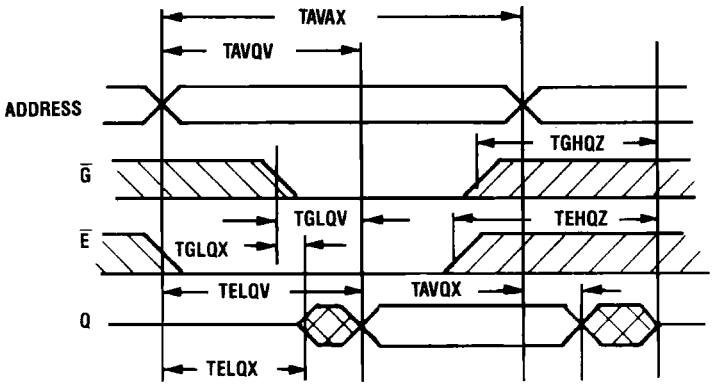
NOTES:
1. All voltages referenced to device GND.
2. AC measurements assume transition time $\leq$ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL $\geq$ 50pF; for CL > 50pF < 300pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.
4. Typical derating = 5mA/MHz increase in ICCOP.
5. Tested as follows: f = 2MHz, VIH = 2.4V, VIL = 0.4V, IOH = -4.0mA, IOL = 4.0mA, VOH $\geq$ 1.5V, and VOL $\leq$ 1.5V.
6. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
7. This is a "typical" value and not a "maximum" value.
8. Applies to DIP device types only.
9. Applies to LCC device types only.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 7, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C &D	Samples/5005	1, 7, 9

Timing Waveforms

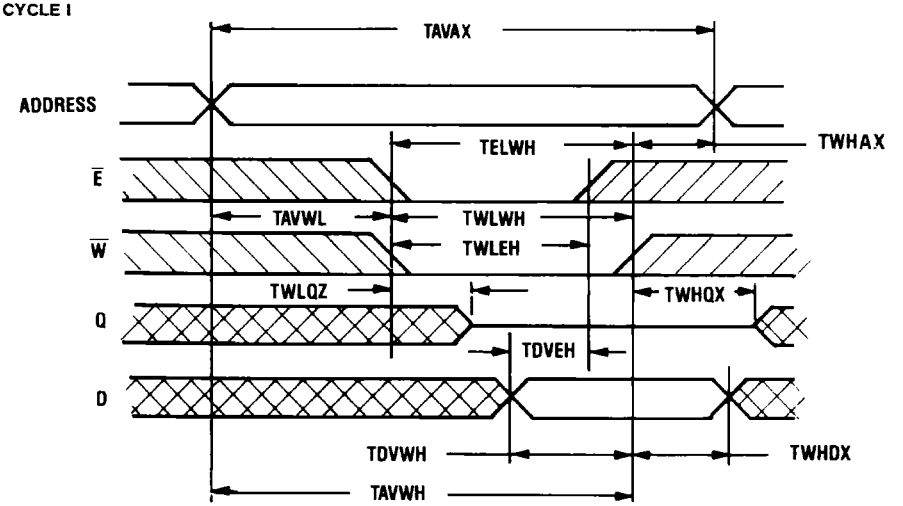
READ CYCLE



NOTE: $\overline{W}$ is High for a Read Cycle

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be $\leq$ VIL and $\overline{W} \geq$ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

WRITE CYCLE I

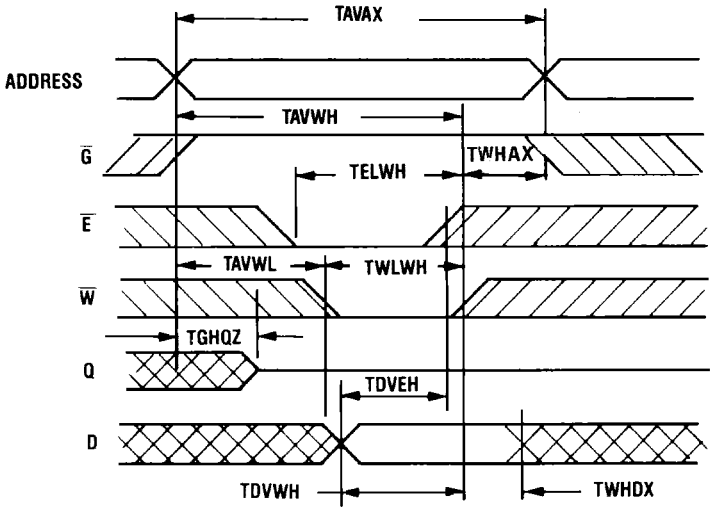


NOTE: $\overline{G}$ is Low Throughout Write Cycle

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the raising edge of $\overline{W}$, (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied, (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

Timing Waveforms (Continued)

WRITE CYCLE II



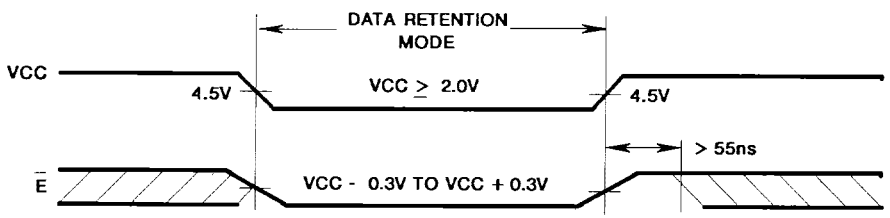
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

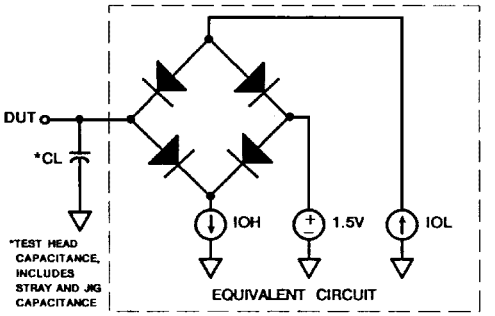
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC - 0.3V to VCC + 0.3V.
2. On RAMs which have selects or output enables (e.g., S, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING

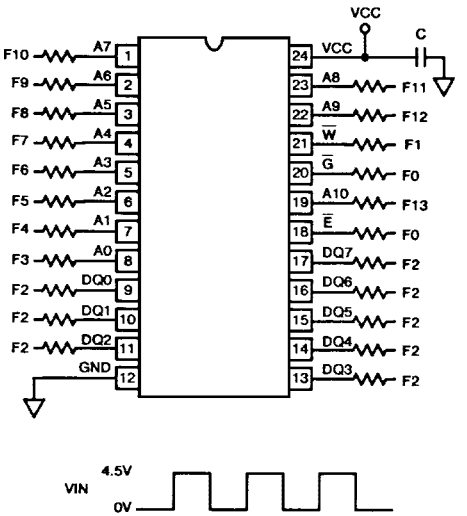


Test Circuit



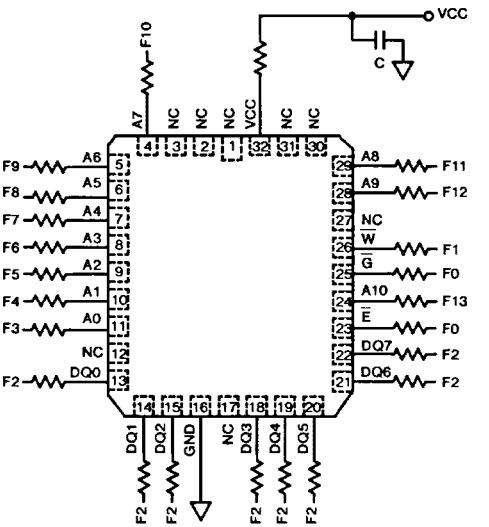
Burn-In Circuits

HM-65162/883 CERAMIC DIP



NOTES:
All Resistors 47kΩ, 5%
F0 = 100kHz ±10%
F1 = F0 + 2, F2 = F1 + 2,
F3 = F2 + 2, . . . F13 = F12 + 2
VCC = 5.5V, ±0.5V
C = 0.01μF (Min)
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V

HM-65162/883 CERAMIC LCC



NOTES:
VCC = 5.5V ±0.5V
VIH = 4.5V ±10%
VIL = -0.2V to +0.4V
F1 = F0 + 2, F2 = F1 + 2,
F3 = F2 + 2, . . . F13 = F12 + 2
F0 = 100kHz ±10%
All Resistors 47kΩ, 5%
C = 0.01μF (Min)

Metal Topology

DIE DIMENSIONS:
186.2 x 200.1 x 19 ±1 mils

METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ± 2kÅ

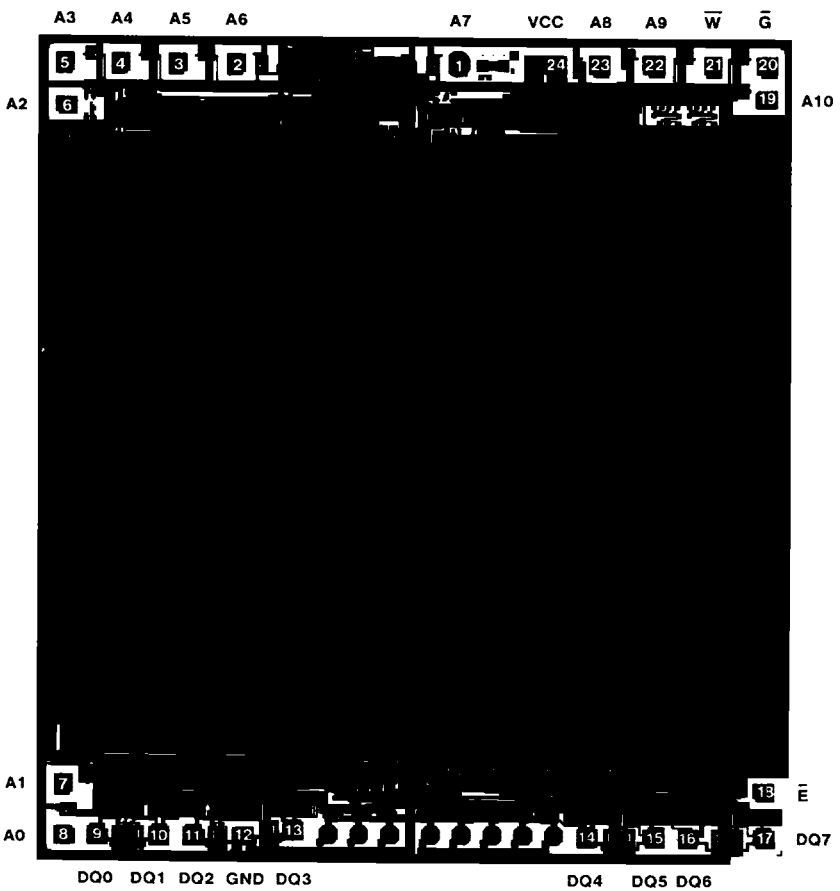
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold - Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

WORST CASE CURRENT DENSITY:
1.7 x 10^5 A/cm^2

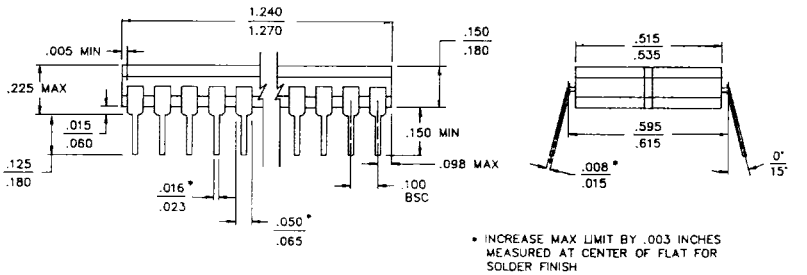
Metallization Mask Layout

HM-65162/883



Packaging†

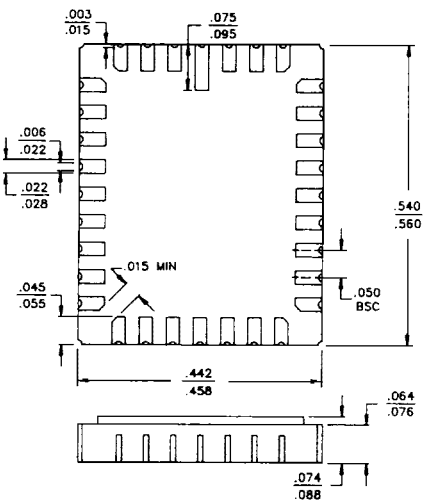
24 PIN CERAMIC DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

32 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-12

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

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TYPICAL ICCDR vs. T_A