2.25-MHz 400-mA and 600-mA DUAL STEP-DOWN CONVERTER

Check for Samples: TPS62400-Q1, TPS62401-Q1, TPS62402-Q1, TPS62403-Q1, TPS62404-Q1, TPS62405-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- High Efficiency—Up to 95%
- V_{IN} Range From 2.5 V to 6 V
- 2.25-MHz Fixed-Frequency Operation
- Output Current 400 mA and 600 mA
- Adjustable Output Voltage From 0.6 V to V_{IN}
- Pin Selectable Output Voltage Supports Simple Dynamic Voltage Scaling
- EasyScale™ Optional One-Pin Serial Interface
- Power-Save Mode at Light Load Currents
- 180° Out-of-Phase Operation
- Output-Voltage Accuracy in PWM Mode ±1%
- Typical 32-µA Quiescent Current for Both Converters
- 100% Duty Cycle for Lowest Dropout
- Available in a 10-Pin QFN (3 mm × 3 mm)

APPLICATIONS

- Battery Applications
- Converters
- Portable Power Applications

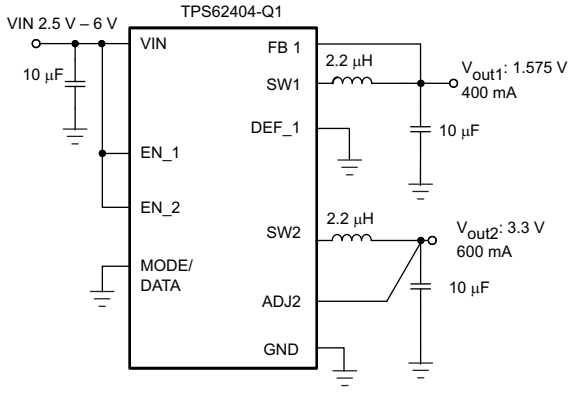
DESCRIPTION

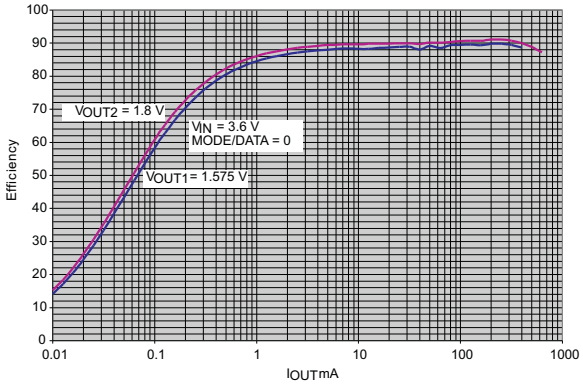
The TPS6240x-Q1 device series are synchronous dual step-down dc-dc converters optimized for battery-powered portable applications. They provide two independent output voltage rails powered by 1-cell li-ion or 3-cell NiMH or NiCd batteries. The devices are also suitable to operate from a standard 3.3-V or 5-V voltage rail.

The EasyScale™ serial interface allows output-voltages modification during operation. The fixed-output-voltage versions, TPS62401-Q1, TPS62402-Q1, TPS62403-Q1, TPS62404-Q1, and TPS62405-Q1, support one-pin-controlled simple dynamic voltage scaling for low-power processors.

The TPS6240x-Q1 operates at 2.25-MHz fixed switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load-current range. For low-noise applications, one can force the devices into fixed-frequency PWM mode by pulling the MODE/DATA pin high. The shutdown mode reduces the current consumption to 1.2-µA, typical. The devices allow the use of small inductors and capacitors to achieve a small solution size.

The TPS62400-Q1 is available in a 10-pin leadless package (3-mm × 3-mm QFN).





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PART NUMBER	DEFAULT OUTPUT VOLTAGE (1)			OUTPUT CURRENT	QFN PACKAGE	ORDERING (2)	TOP-SIDE MARKING
–40°C to 125°C	TPS62400-Q1	OUT1	Adjustable		400 mA	DRC	TPS62400QDRCQ1	SHI
		OUT2			600 mA			
	TPS62401-Q1	OUT1	Fixed default	DEF_1 = High 1.1 V	400 mA	DRC	TPS62401QDRCQ1	PREVIEW
				DEF_1 = Low 1.575 V				
		OUT2	Fixed default 1.8 V		600 mA			
	TPS62402-Q1	OUT1	Fixed default	DEF_1 = High 1.8 V	400 mA	DRC	TPS62402QDRCQ1	SJS
				DEF_1 = Low 1.2 V				
		OUT2	Fixed default 3.3 V		600 mA			
	TPS62403-Q1	OUT1	Fixed default	DEF_1 = High 1.1 V	400 mA	DRC	TPS62403QDRCQ1	PREVIEW
				DEF_1 = Low 1.575 V				
		OUT2	Fixed default 2.8 V		600 mA			
	TPS62404-Q1	OUT1	Fixed default	DEF_1 = High 1.9 V	400 mA	DRC	TPS62404QDRCQ1	OET
				DEF_1 = Low 1.575 V				
		OUT2	Fixed default 3.3 V		600 mA			
	TPS62405-Q1	OUT1	Fixed default	DEF_1 = High 1.925 V	400 mA	DRC	TPS62405QDRCRQ1	SJT
				DEF_1 = Low 1.215 V				
		OUT2	Fixed default 3.35 V		600 mA			

(1) Contact TI for other fixed-output-voltage options.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
	Input voltage range on V_{IN} (2)	–0.3 to 7	V
	Voltage range on EN, MODE/DATA, DEF_1	–0.3 to V_{IN} +0.3, ≤ 7	V
	Current into MODE/DATA	≤ 0.5	mA
	Voltage on SW1, SW2	–0.3 to 7	V
	Voltage on ADJ2, FB1	–0.3 to V_{IN} +0.3, ≤ 7	V
T_J(max)	Maximum operating junction temperature	150	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD ratings	Human-Body Model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-Device Model (CDM) AEC-Q100 Classification Level C4B	750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS6240x-Q1 DRC 10 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	42.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.9	
θ_{JB}	Junction-to-board thermal resistance	18.1	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	18.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.5		6	V
	Output voltage range for adjustable voltage	0.6		V_{IN}	V
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 20 µF, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.5		6	V
I_Q	Operating quiescent current	One converter, I_{OUT} = 0 mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 OR EN2 = 1		19	29	µA
		Two converters, I_{OUT} = 0 mA. PFM mode enabled (Mode = 0) device not switching, EN1 = 1 AND EN2 = 1		32	48	µA
		I_{OUT} = 0 mA, MODE/DATA = GND, for one converter, V_{OUT} 1.575 V(1)		23		µA
		I_{OUT} = 0 mA, MODE/DATA = V_{IN}, for one converter, V_{OUT} 1.575 V (1)		3.6		mA
I_{SD}	Shutdown current	EN1, EN2 = GND, V_{IN} = 3.6 V(2)		1.2	3	µA
		EN1, EN2 = GND, V_{IN} ramped from 0 V to 3.6 V(3)		0.1	1	
V_{UVLO}	Undervoltage lockout threshold	Falling		1.5	2.35	V
		Rising			2.4	
ENABLE EN1, EN2						
V_{IH}	High-level input voltage, EN1, EN2		1.2		V_{IN}	V
V_{IL}	Low-level input voltage, EN1, EN2		0		0.4	V
I_{IN}	Input bias current, EN1, EN2	EN1, EN2 = GND or V_{IN}		0.05	1	µA
DEF_1 INPUT						
V_{DEF_1H}	DEF_1 high level input voltage	DEF_1 pin is a digital input at TPS62401-Q1 fixed output-voltage option.	0.9		V_{IN}	V
V_{DEF_1L}	DEF_1 low level input voltage	DEF_1 pin is a digital input at TPS62401-Q1 fixed output-voltage option.	0		0.4	V

(1) Device is switching with no load on the output, L = 3.3 µH, value includes losses of the coil.
(2) These values are valid after enabling the device one time (EN1 or EN2 = high) and maintaining supply voltage V_{IN}.
(3) These values are valid when the device is disabled (EN1 and EN2 low) and supply voltage V_{IN} is powered up. The values remain valid until enabling the device the first time (EN1 or EN2 = high). After the first enable, Note 3 becomes valid.

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 20 µF, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input bias current DEF_1		DEF_1 GND or V_{IN}		0.01	1	µA
MODE/DATA							
V_{IH}	High-level input voltage, MODE/DATA			1.2		V_{IN}	V
V_{IL}	Low-level input voltage, MODE/DATA			0		0.4	V
I_{IN}	Input bias current, MODE/DATA		MODE/DATA = GND or VIN		0.01	1	µA
V_{OH}	Acknowledge output voltage high		Open drain, through external pullup resistor			V_{IN}	V
V_{OL}	Acknowledge output voltage low		Open drain, sink current 500 µA	0		0.4	V
INTERFACE TIMING							
t_{Start}	Start time			2			µs
t_{H_LB}	High-time low bit, logic 0 detection		Signal level on MODE/DATA pin is > 1.2 V	2		200	µs
t_{L_LB}	Low-time low bit, logic 0 detection		Signal level on MODE/DATA pin < 0.4 V	2 x t_{H_LB}		400	µs
t_{L_HB}	Low-time high bit, logic 1 detection		Signal level on MODE/DATA pin < 0.4 V	2		200	µs
t_{H_HB}	High-time high bit, logic 1 detection		Signal level on MODE/DATA pin is > 1.2 V	2 x t_{L_HB}		400	µs
t_{EOS}	End of stream		T_{EOS}	2			µs
t_{ACKN}	Duration of acknowledge condition (MODE/DATE line pulled low by the device)		V_{IN} 2.5 V to 6 V	400		520	µs
t_{valACK}	Acknowledge valid time					2	µs
$t_{timeout}$	Timeout for entering power-save mode		MODE/DATA pin changes from high to low			520	µs
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on-resistance, converter 1,2		V_{IN} = V_{GS} = 3.6 V		280	620	mΩ
I_{LK_PMOS}	P-channel leakage current		V_{DS} = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance converter 1,2		V_{IN} = V_{GS} = 3.6 V		200	450	mΩ
$I_{LK\_SW1/SW2}$	Leakage current into SW1/SW2 pin		Includes N-channel leakage current, V_{IN} = open, V_{SW} = 6 V, EN = GND(4)		6	7.5	µA
I_{LIMF}	Forward current limit PMOS and NMOS	OUTPUT 1	2.5 V ≤ V_{IN} ≤ 6 V	0.68	0.8	0.92	A
		OUTPUT 2		0.85	1	1.15	
T_{SD}	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C
OSCILLATOR							
f_{SW}	Oscillator frequency		2.5 V ≤ V_{IN} ≤ 6 V	2	2.25	2.5	MHz
OUTPUT							
V_{OUT}	Adjustable output-voltage range			0.6		V_{IN}	V
V_{ref}	Reference voltage				600		mV

(4) An internal resistor of 1MΩ connects pins SW1 and SW2 to GND.

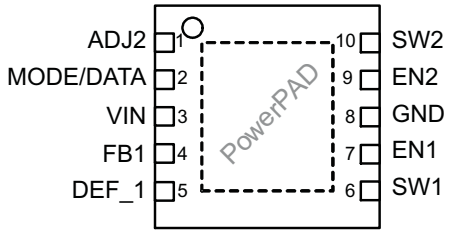
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN = V_{IN}, MODE = GND, L = 2.2 µH, C_{OUT} = 20 µF, T_A = T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT\ (PFM)}$	DC output voltage accuracy adjustable and fixed output voltage(5)	Voltage positioning active, MODE/DATA = GND, device operating in PFM mode, V_{IN} = 2.5 V to 5 V (6) (7)	–1.5%	1.01 V_{OUT}	2.5%	
$V_{OUT(PWM)}$		MODE/DATA = GND; device operating in PWM mode, V_{IN} = 2.5 V to 6 V(7)	–1%	0%	1%	
		V_{IN} = 2.5 V to 6 V, MODE/DATA = V_{IN} , Fixed PWM operation, 0 mA < I_{OUT1} < 400 mA ; 0 mA < I_{OUT2} < 600 mA(8)	–1%	0%	1%	
	DC output voltage load regulation	PWM operation mode			0.5	%/A
$t_{Start\ up}$	Start-up time	Activation time to start switching(9)		170		µs
t_{Ramp}	V_{OUT} Ramp-up time	Time to ramp from 5% to 95% of V_{OUT}		750		µs

(5) Output voltage specification does not include tolerance of external voltage-programming resistors.
(6) Configuration L typ 2.2 µH, C_{OUT} typ 20 µF. See parameter measurement information, the output voltage ripple in PFM mode depends on the effective capacitance of the output capacitor; larger output capacitors lead to tighter output voltage tolerance.
(7) In power-save mode, the device typically enters PWM operation at I_{PSM} = V_{IN} / 32 Ω.
(8) For V_{OUT} > 2 V, V_{IN} min = V_{OUT} + 0.5 V
(9) This time is valid if one converter turns from shutdown mode (EN2 = 0) to active mode (EN2 = 1) with the other converter already enabled (for example, EN1 = 1). In case both converters are turned from shutdown mode (EN1 and EN2 = low) to active mode (EN1 and/or EN2 = 1), a typical value of typ 80 µs for ramp up of internal circuits must be added. After t_{Start}, the converter starts switching and ramps V_{OUT}.

PIN ASSIGNMENTS

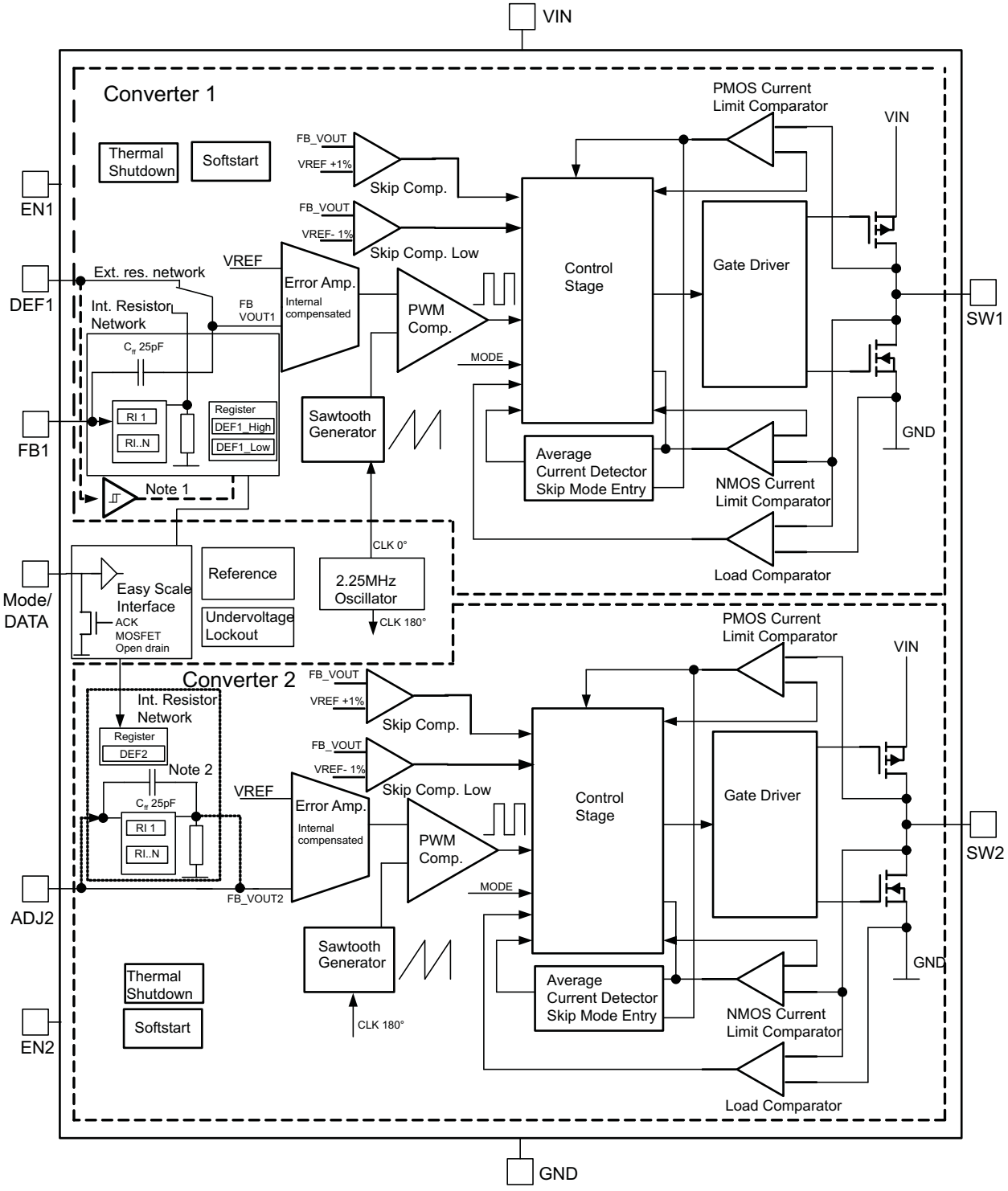


Top view DRC package

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO. (QFN)		
ADJ2	1	I	Input to adjust output voltage of converter 2. In adjustable version (TPS62400-Q1) connect an external resistor divider between VOUT2, this pin and GND to set output voltage between 0.6 V and VIN. In fixed-output-voltage version (TPS62401-Q1) this pin MUST connect directly to the output. If usjng the EasyScale interface converter 2, this pin must connect directly to the output, too.
DEF_1	5	I	This pin defines the output voltage of converter 1. The pin acts either as analog input for output voltage setting via external resistors (TPS62400-Q1), or digital input to select between two fixed default output voltages (TPS62401-Q1, TPS62402-Q1, TPS62403-Q1, TPS62404-Q1). For the TPS62400-Q1, an external resistor network must connect to this pin to adjust the default output voltage. Using the fixed output voltage device options this pin selects between two fixed default output voltages, see table ordering information
EN1	7	I	Enable input for converter 1, active-high
EN2	9	I	Enable input for converter 2, active-high
FB1	4	I	Direct feedback voltage sense input of converter 1, connect directly to VOUT1. An internal feed-forward capacitor connects between this pin and the error amplifier. In case of fixed output voltage versions or when using the interface, this pin connects to an internal resistor divider network.
GND	8		GND for both converters; connect this pin to the thermal pad.
MODE/DATA	2	I/O	This pin has two functions: 1. Operation-mode selection: With low level enables power-save mode where the device operates in PFM mode at light loads and automatically enters PWM mode at heavy loads. Pulling this PIN to high forces the device to operate in PWM mode over the whole load range. 2. EasyScale™ interface function: One-wire serial interface to change the output voltage of both converters. The pin has an open-drain output to provide an acknowledge condition if requested. The current into the open-drain output stage may not exceed 500 µA. The interface is active if either EN1 or EN2 is high.
SW1	6	I/O	Switch pin of converter 1. Connect to inductor
SW2	10	I/O	Switch pin of converter 2. Connect to inductor
VIN	3		Supply voltage, connect to VBAT, 2.5 V to 6 V
Thermal pad			Connect to GND

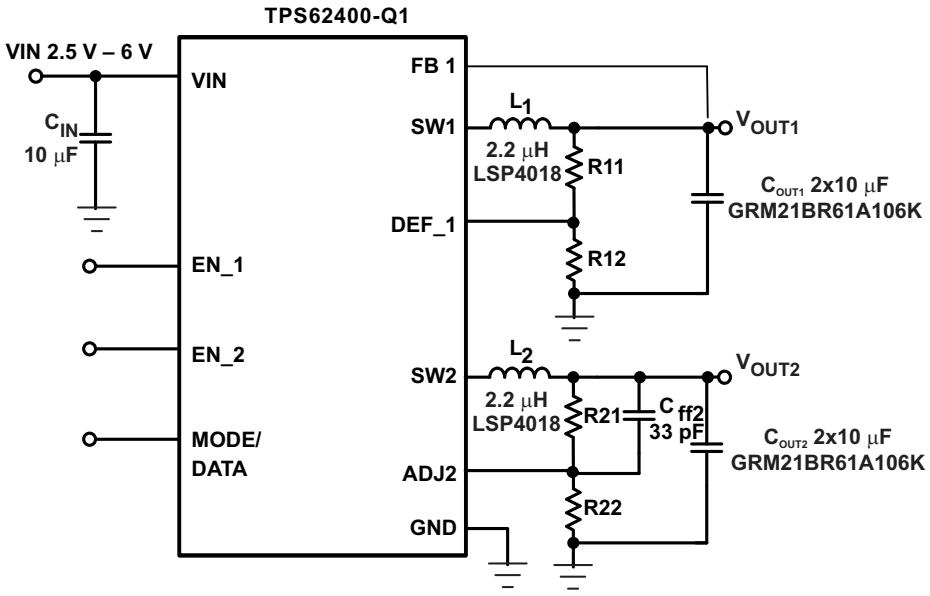
FUNCTIONAL BLOCK DIAGRAM



(1) In fixed output-voltage version, the PIN DEF_1 connects to an internal digital input and disconnects from the error amplifier.

(2) To set the output voltage of converter 2 through the EasyScale™ interface, the ADJ2 pin must directly connect to VOUT2.

PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

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Efficiency TPS62400-Q1 VOUT2 = 3.3 V		4
Efficiency TPS62402-Q1		5
Efficiency TPS62403-Q1		6
Efficiency	vs VIN	7, 8
DC Output Accuracy VOUT1 = 1.1 V		9
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DC Output Accuracy V_{OUT}1 1.575 V, L = 2.2 µH, C_{OUT} = 22 µF		12
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TYPICAL CHARACTERISTICS (continued)

Table 1. TABLE OF GRAPHS AND FIGURES (continued)

	FIGURE NO.
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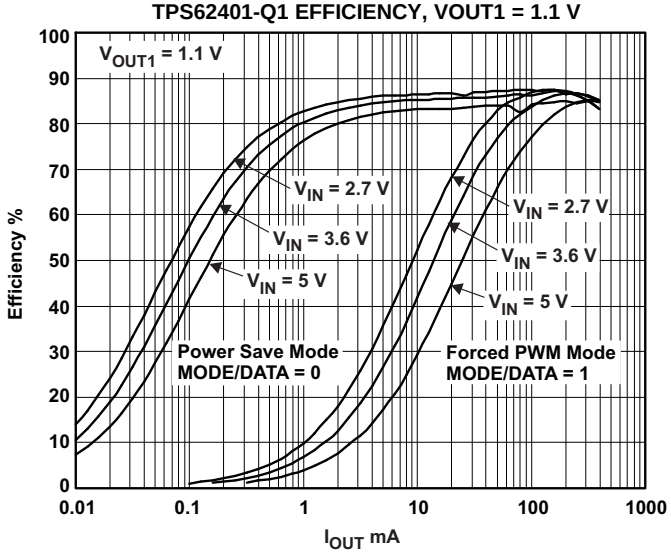


Figure 1.

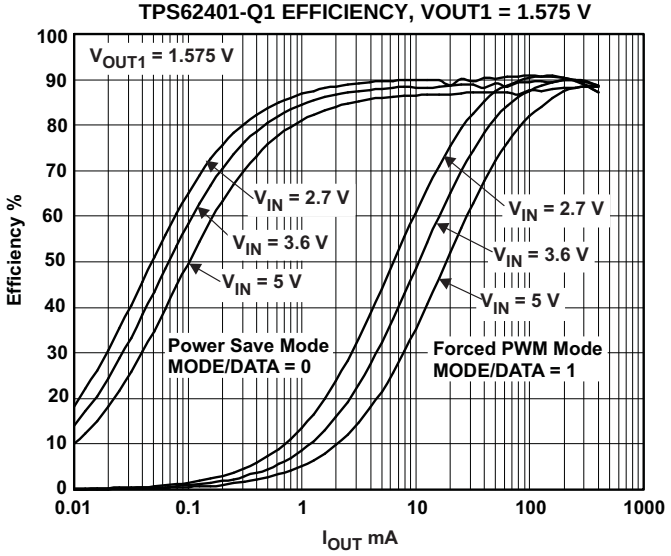


Figure 2.

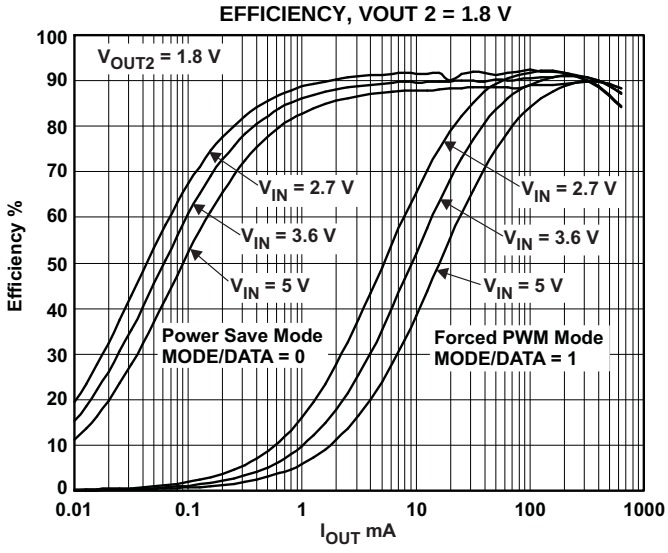


Figure 3.

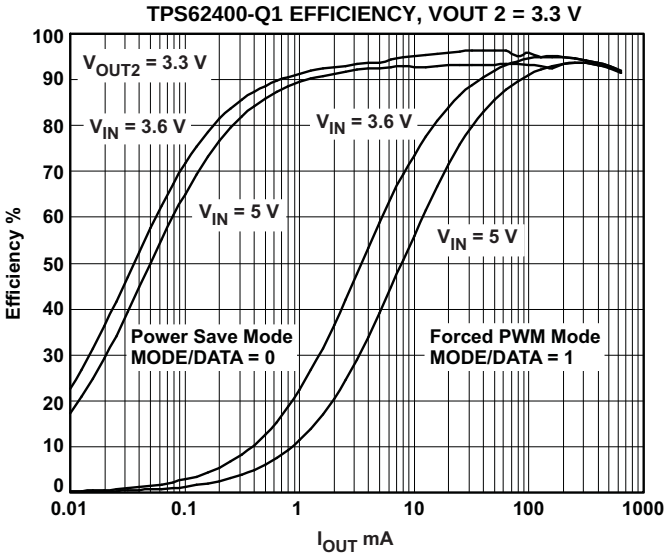


Figure 4.

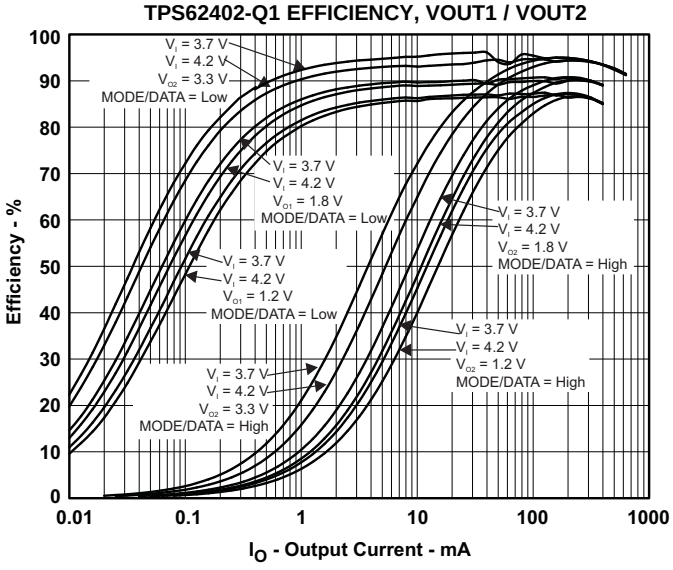


Figure 5.

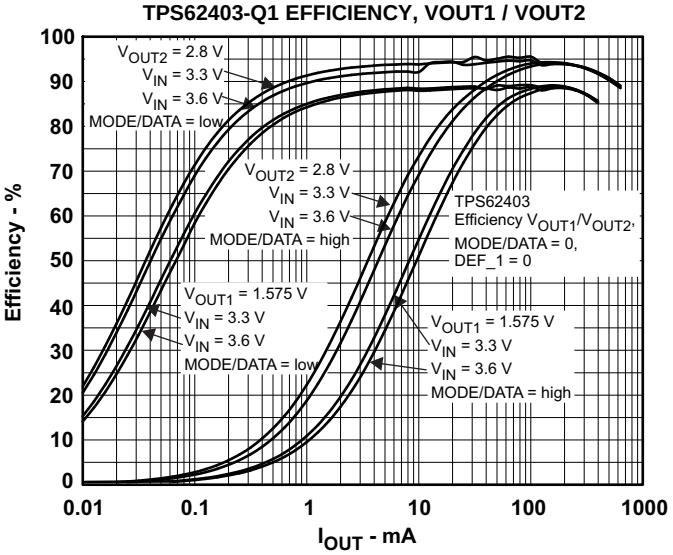


Figure 6.

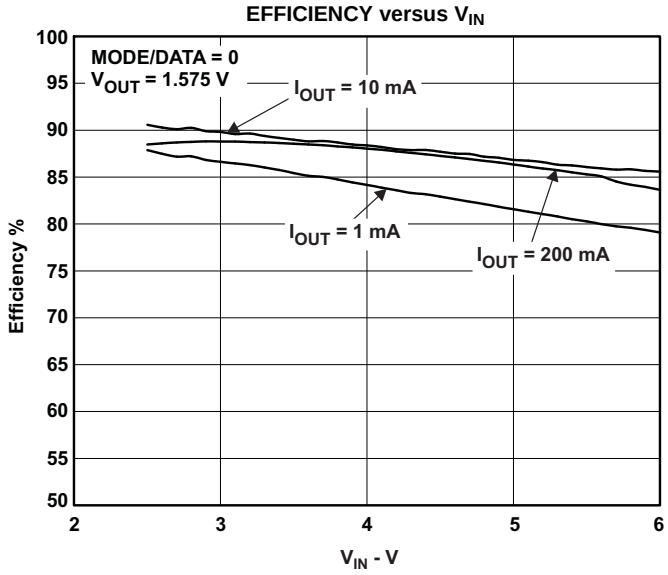


Figure 7.

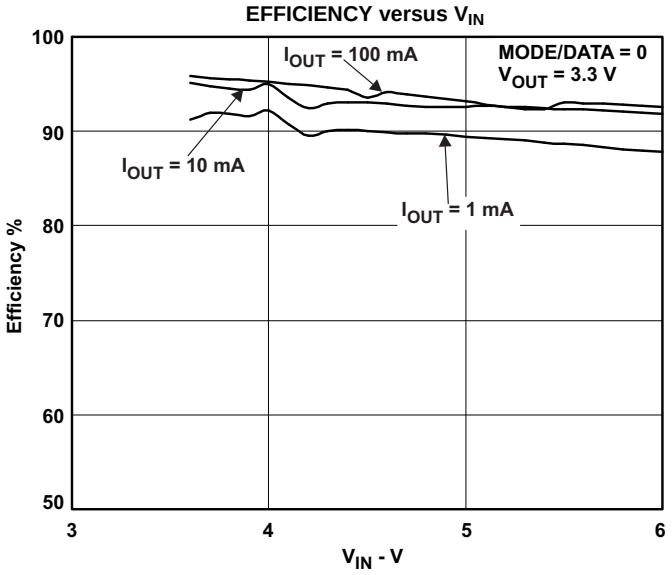


Figure 8.

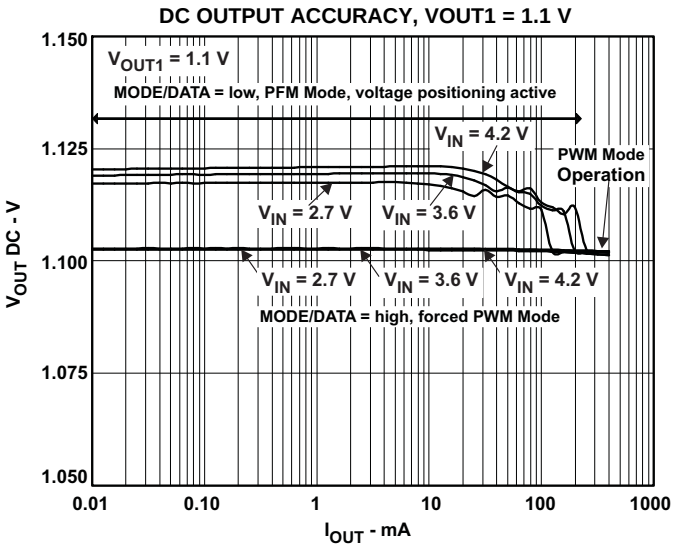


Figure 9.

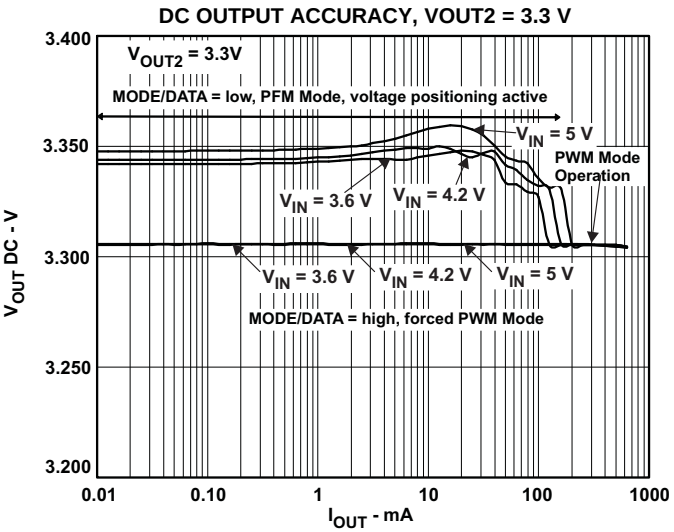


Figure 10.

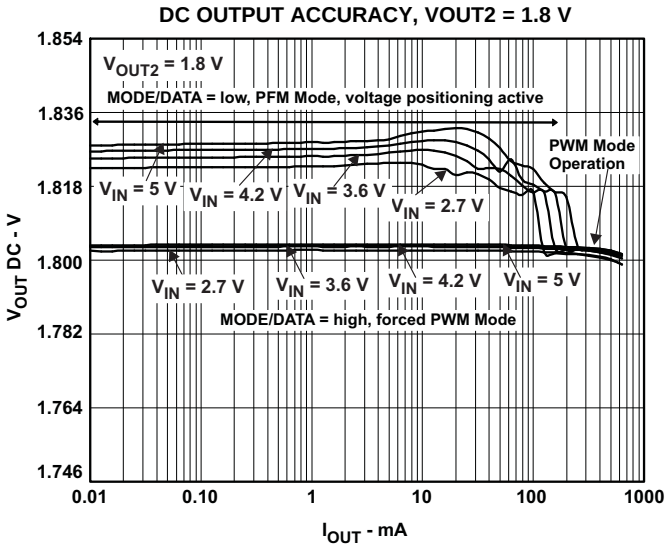


Figure 11.

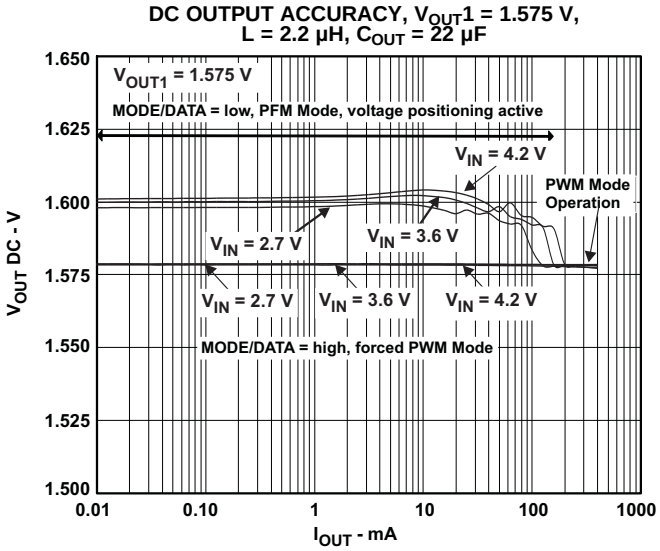


Figure 12.

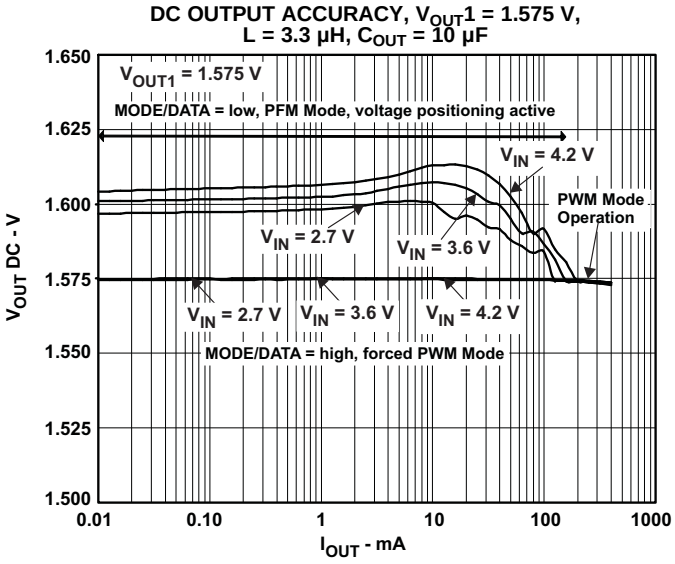


Figure 13.

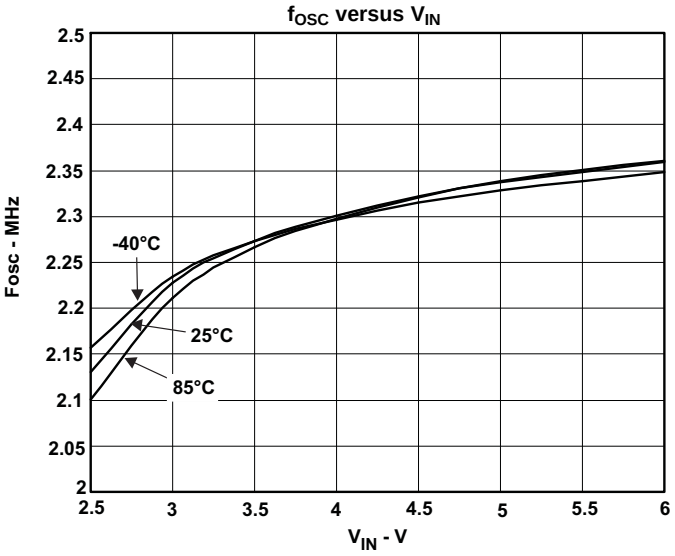


Figure 14.

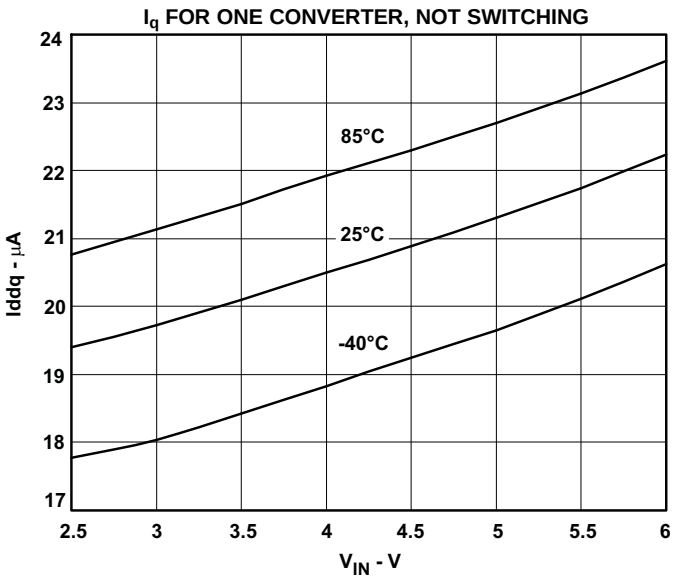


Figure 15.

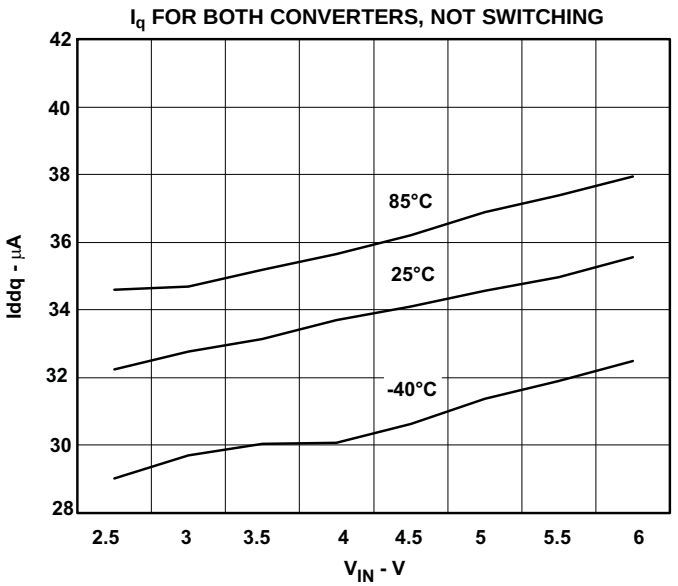


Figure 16.

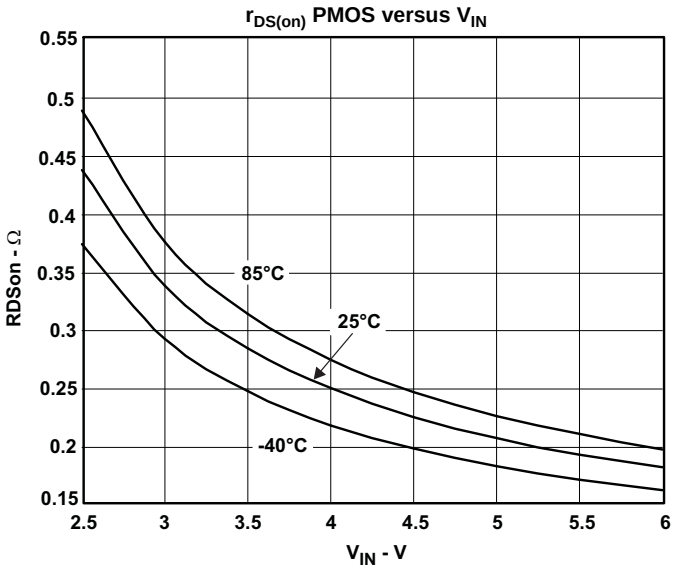


Figure 17.

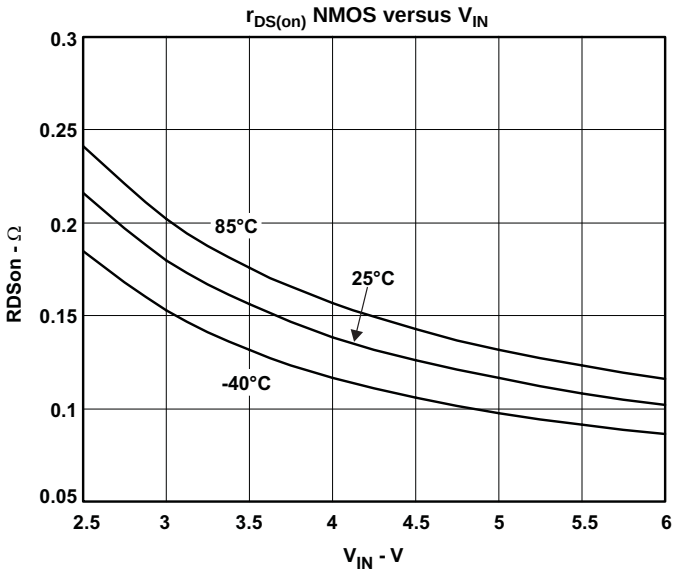
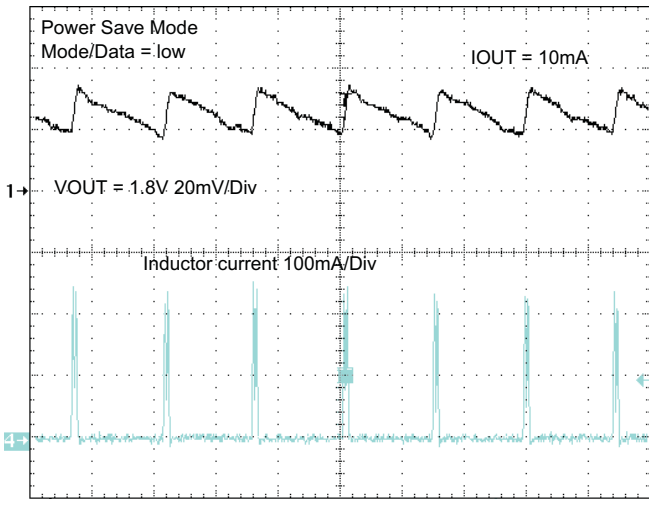


Figure 18.

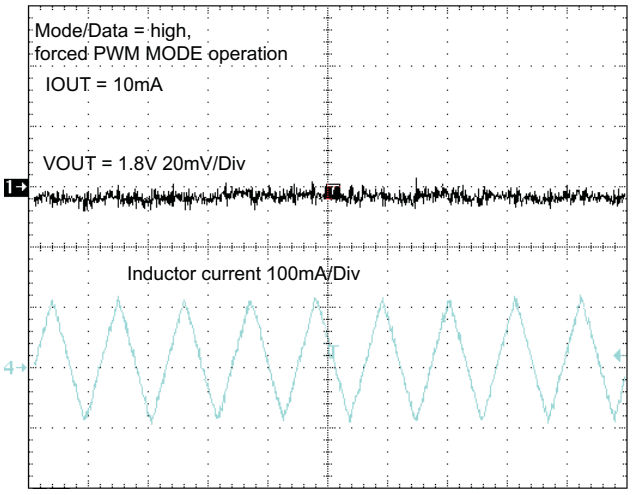
LIGHT-LOAD OUTPUT-VOLTAGE RIPPLE IN POWER SAVE MODE



Time base - 10 µs/Div

Figure 19.

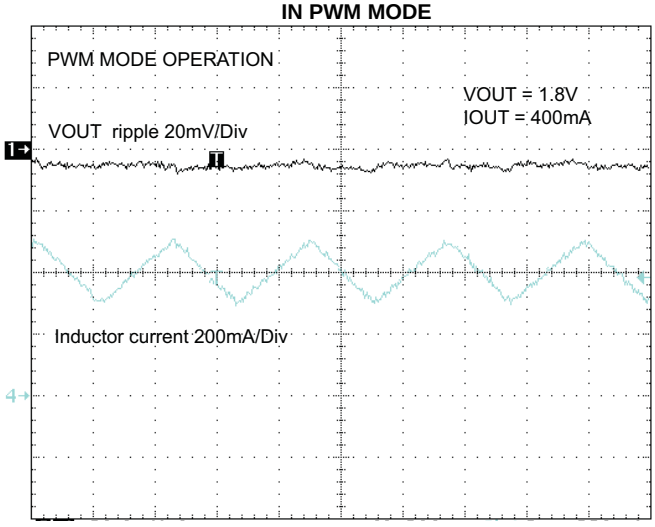
OUTPUT-VOLTAGE RIPPLE IN FORCED-PWM MODE



Time base - 400 ns/Div

Figure 20.

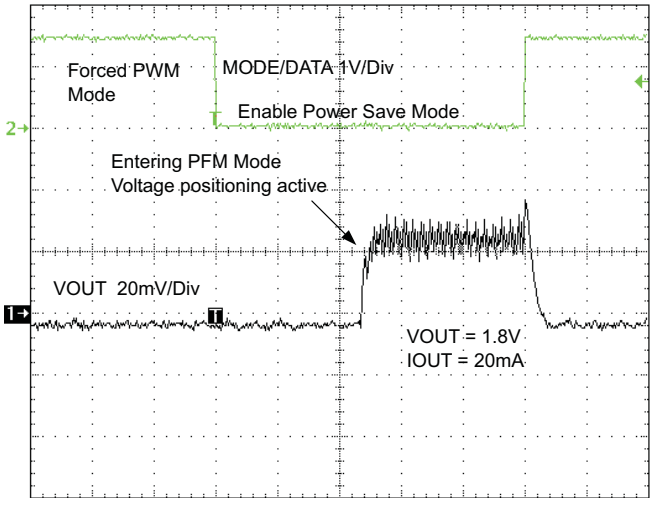
OUTPUT-VOLTAGE RIPPLE IN PWM MODE



Time base - 200 ns/Div

Figure 21.

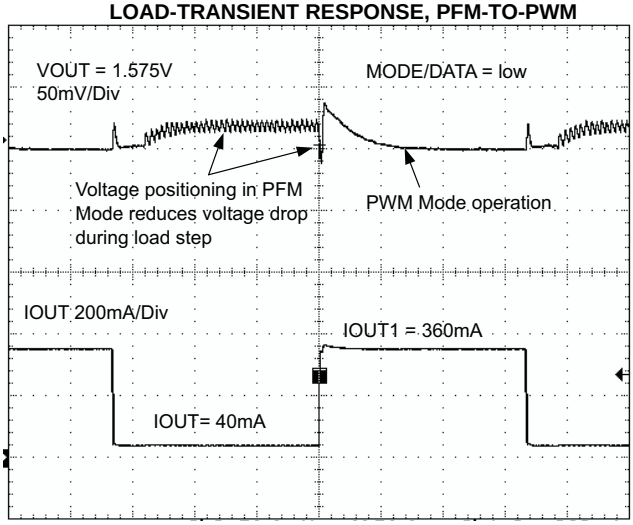
FORCED PWM-TO-PFM MODE TRANSITION



Time base - 200 µs/Div

Figure 22.

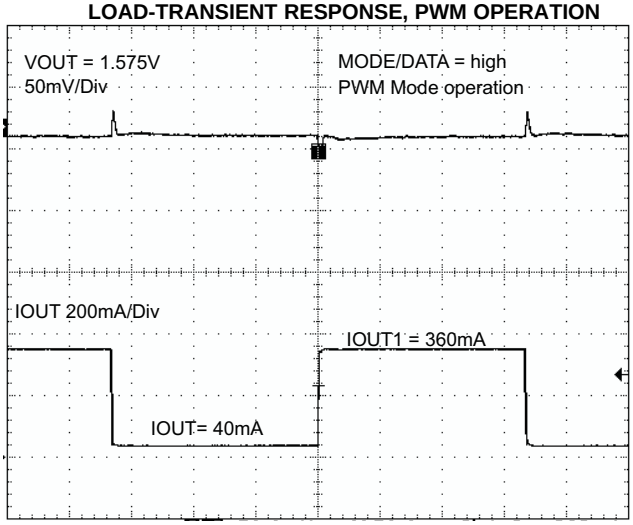
LOAD-TRANSIENT RESPONSE, PFM-TO-PWM



Time base - 50 µs/Div

Figure 23.

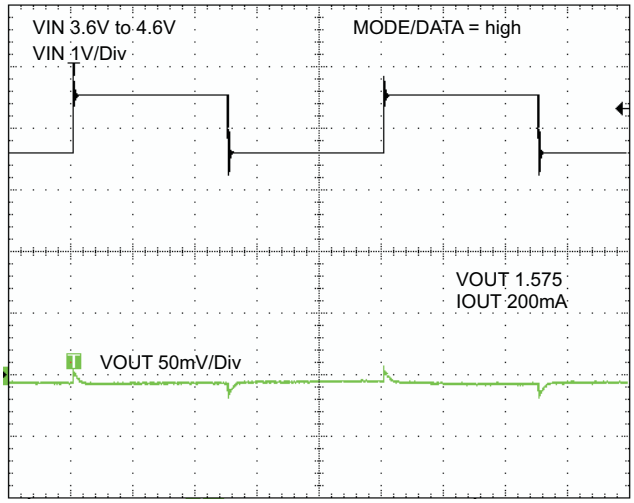
LOAD-TRANSIENT RESPONSE, PWM OPERATION



Time base - 50 µs/Div

Figure 24.

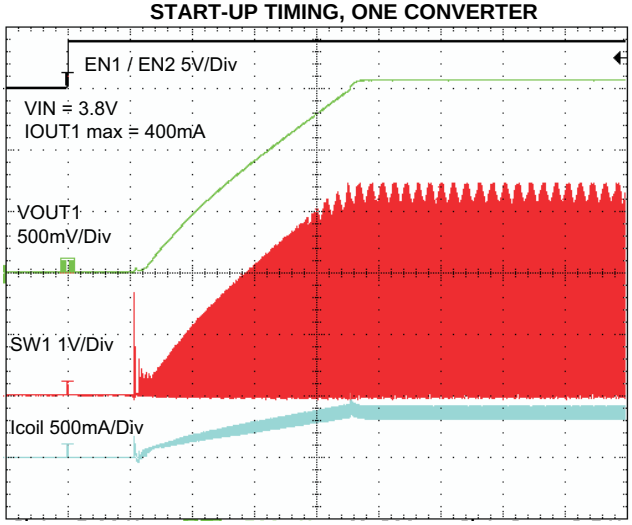
LINE-TRANSIENT RESPONSE



Time base - 400 µs/Div

Figure 25.

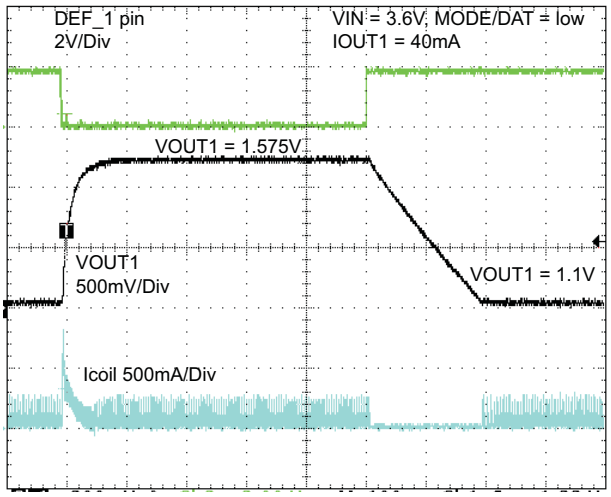
START-UP TIMING, ONE CONVERTER



Time base - 200 µs/Div

Figure 26.

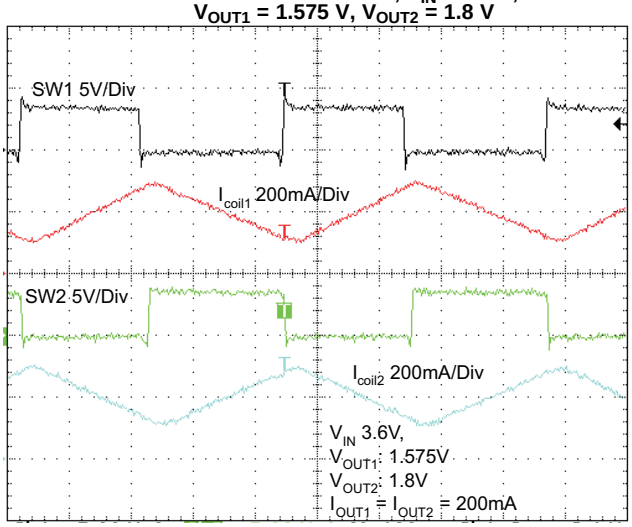
TPS62401-Q1 DEF1_PIN FUNCTION FOR OUTPUT-VOLTAGE SELECTION



Time base - 100 µs/Div

Figure 27.

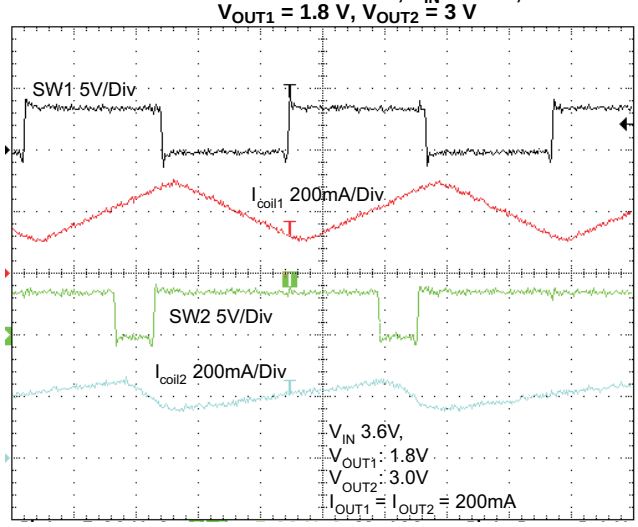
TYPICAL OPERATION, V_{IN} = 3.6 V, V_{OUT1} = 1.575 V, V_{OUT2} = 1.8 V



Time base - 100 ns/Div

Figure 28.

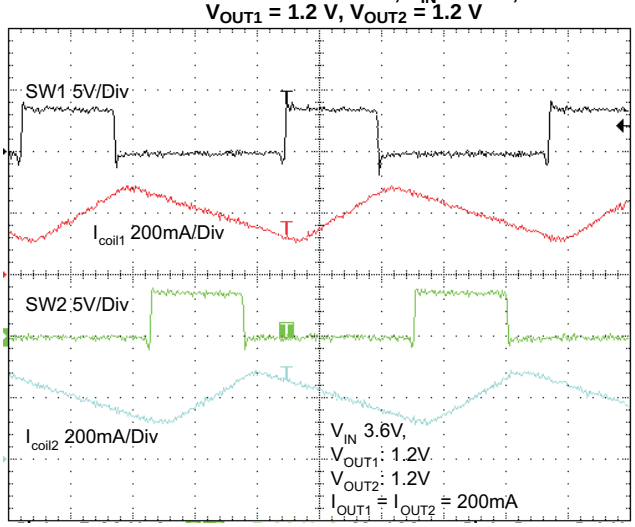
TYPICAL OPERATION, V_{IN} = 3.6 V, V_{OUT1} = 1.8 V, V_{OUT2} = 3 V



Time base - 100 ns/Div

Figure 29.

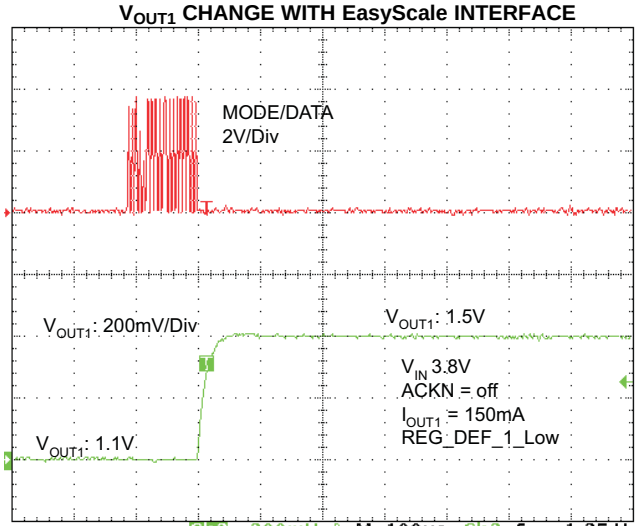
TYPICAL OPERATION, V_{IN} = 3.6 V, V_{OUT1} = 1.2 V, V_{OUT2} = 1.2 V



Time base - 100 ns/Div

Figure 30.

V_{OUT1} CHANGE WITH EasyScale INTERFACE



Time base - 100 µs/Div

Figure 31.

DETAILED DESCRIPTION

OPERATION

The TPS62400-Q1 includes two synchronous step-down converters. The converters operate with typically 2.25-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. With the power-safe mode enabled, the converters automatically enter power-save mode at light load currents and operate in PFM (pulse frequency modulation).

During PWM operation, the converters use a unique fast-response voltage-mode controller scheme with input-voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch turns on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

Each converter integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET turns off and the N-channel MOSFET turns on. If the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit.

The two dc-dc converters operate synchronized to each other. A 180° phase shift between converter 1 and converter 2 decreases the input rms current.

Converter 1

In the adjustable output voltage version, TPS62400-Q1, one can set the converter 1 default output voltage via an external resistor network on the DEF_1 pin, which operates as an analog input. In this case, one can set the output voltage in the range of 0.6 V to VIN V. The FB1 pin must directly connect to the converter 1 output voltage V_{OUT1}. It feeds back the output voltage directly to the regulation loop.

One can also change the output voltage of converter 1 with the EasyScale serial Interface. This makes the device very flexible for output-voltage adjustment. In this case, the device uses an internal resistor network.

In the fixed default output voltage version, TPS62401-Q1, the DEF_1 pin configuration is as a digital input. Converter 1 defaults to 1.1 V or **1.575** V, depending on the level of the DEF_1 pin. If DEF_1 is low, the default is **1.575** V; if high, the default is **1.1** V. With the EasyScale interface, one can change the output voltage for each DEF_1 pin condition (high or low).

Converter 2

In the adjustable output voltage version, TPS62400-Q1, an external resistor divider connected to ADJ2 pin sets the converter 2 output voltage. The converter uses an external feed-forward capacitor of 33 pF.

In fixed output-voltage version TPS62401-Q1, the fixed default output voltage is fixed to 1.8 V. In this case, the ADJ2 pin must connect directly to the converter 2 output voltage,V_{OUT2}.

It is also possible to change the output voltage of converter 2 via the EasyScale interface. In this case, the ADJ2 pin must connect directly to converter 2 output voltage V_{OUT2}, with no connection of external resistors permitted.

POWER-SAVE MODE

Setting the MODE/DATA pin to low for both converters enables power-save mode. If the load current of a converter decreases, this converter enters power-save-mode operation automatically. The transition of a converter to power-save mode is independent from the operating condition of the other converter. During power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage in PFM mode to typically 1.01 × V_{OUT}. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load, the device monitors average inductor current. The device changes from PWM mode to power-save mode if in PWM mode the inductor current falls below a certain threshold. The typical output current threshold, which one can calculate according to Equation 1 for each converter, depends on VIN.

Equation 1: Average output current threshold to enter PFM mode

$$I_{OUT\_PFM\_enter} = \frac{VIN_{DCDC}}{32\ \Omega} \quad (1)$$

Equation 2: Average output current threshold to leave PFM mode

$$I_{OUT\_PFM\_leave} = \frac{VIN_{DCDC}}{24\ \Omega} \quad (2)$$

In order to keep the output-voltage ripple in power-save mode low, a single threshold comparator (skip comparator) monitors the output voltage. As the output voltage falls below the skip-comparator threshold (skip comp) of 1.01 × $V_{OUTnominal}$, the corresponding converter starts switching for a minimum time period of typically 1 µs and provides current to the load and the output capacitor. Therefore, the output voltage increases and the device maintains switching until the output voltage trips the skip comparator threshold (skip comp) again. At this moment, all switching activity stops and the quiescent current reduces to minimum. The output capacitor supplies the load until the output voltage has dropped below the threshold again. Hereupon, the device starts switching again.

The power-save mode is left and PWM Mode entered in case the output current exceeds the current IOUT_PFM_leave or if the output voltage falls below a second comparator threshold, called skip comparator low (Skip Comp Low) threshold. This skip comparator low threshold is 2% below nominal V_{OUT} and enables a fast transition from power-save mode to PWM mode during a load step.

Power-save mode typically reduces the quiescent current to 19 µA for one converter and 32 µA for both converters active. This single-skip comparator threshold method in power-save mode results in a very low output-voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing output capacitor values minimizes the output ripple. One can disable the power-save mode by setting the MODE/DATA pin to high. Both converters then operate in fixed PWM mode. Power-save mode enable or disable applies to both converters.

Dynamic Voltage Positioning

This feature reduces the voltage under- and overshoots at load steps from light to heavy load and vice versa. Power-save-mode operation activates dynamic voltage positioning. It provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off. This improves load-transient behavior.

At light loads, in which the converter operates in PFM mode, the output voltage regulation is typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the skip comparator low threshold set to 2% below the nominal value and enters PWM mode. During a load throw-off from heavy load to light load, the device also minimizes voltage overshoot due to active regulation turning on the N-channel switch.

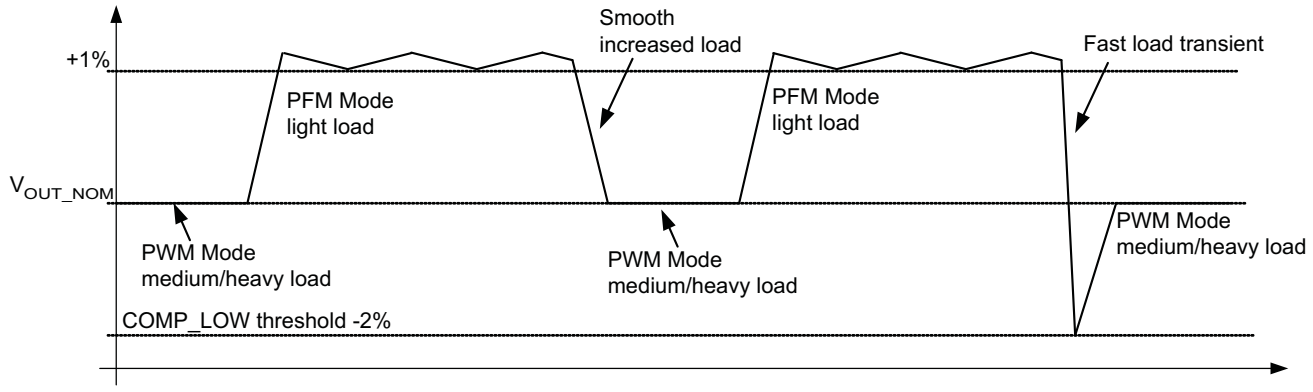


Figure 32. Dynamic Voltage Positioning

Soft Start

The two converters have an internal soft-start circuit that limits the inrush current during start-up. Figure 33 shows control of the output-voltage ramp-up during soft start.

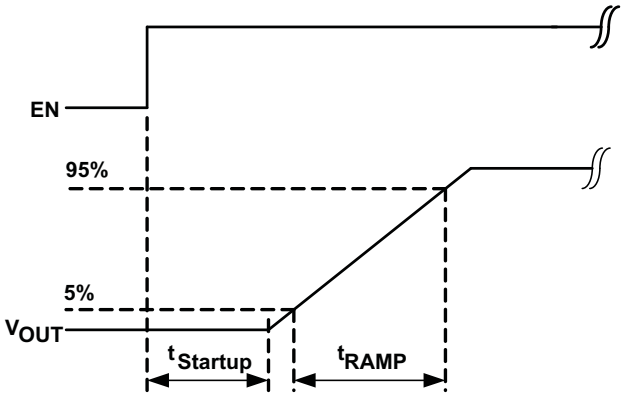


Figure 33. Soft Start

100% Duty-Cycle Low-Dropout Operation

The converters offer a low input-to-output voltage difference while still maintaining operation with the use of the 100% duty-cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage, which one can calculate as:

$$Vin_{min} = Vout_{max} + Iout_{max} \times \left(RDSon_{max} + R_L\right) \quad (3)$$

with:

$Iout_{max}$ = maximum output current plus inductor ripple current

$RDSon_{max}$ = maximum P-channel switch $r_{DS(on)}$.

R_L = dc resistance of the inductor

$Vout_{max}$ = nominal output voltage plus maximum output-voltage tolerance

With decreasing load current, the device automatically switches into pulse-skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized and the device runs with a minimum quiescent current, maintaining high efficiency.

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages, and from excessive discharge of the battery, and disables the converters. The undervoltage lockout threshold is typically 1.5 V; maximum of 2.35 V. In case the interface overwrites the default register values, the new values in the registers REG_DEF_1_High, REG_DEF_1_Low and REG_DEF_2 remain valid as long the supply voltage does not fall below the undervoltage lockout threshold, independent of disabling of the converters.

MODE SELECTION

The MODE/DATA pin allows mode selection between forced PWM mode and power-save mode for both converters. Furthermore, this pin is a multipurpose pin and provides (besides mode selection) a one-pin interface to receive serial data from a host to set the output voltage. The EasyScale Interface section describes this.

Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converters operate in fixed-frequency PWM mode at moderate-to-heavy loads, and in the PFM mode during light loads, maintaining high efficiency over a wide load-current range.

Pulling the MODE/DATA pin high forces both converters to operate constantly in the PWM mode, even at light load currents. The advantage is that the converters operate with a fixed frequency, allowing simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

In the case of changing the operation mode from forced PWM mode (MODE/DATA = high) to power-save mode (MODE/DATA = 0), enabling the power-save mode occurs after a delay time of $t_{timeout}$, which is 520 µs maximum.

Setting the MODE/DATA to 1 enables forced-PWM-mode operation immediately.

ENABLE

The device has a separate EN pin for each converter to start up each converter independently. If EN1 or EN2 is set to high, the corresponding converter starts up with soft start as previously described.

Pulling EN1 and EN2 pin low forces the device into shutdown, with a shutdown quiescent current of typically 1.2 µA. In this mode, the P- and N-Channel MOSFETs turn off and the entire internal control circuitry switches off. For proper operation, terminate the EN1 and EN2 pins, do not leave them floating.

DEF_1 PIN FUNCTION

The DEF_1 pin, dedicated to converter 1, makes the output voltage selection very flexible to support dynamic voltage management.

Depending on the device version, this pin works either as:

1. Analog input for adjustable output voltage setting (TPS62400-Q1):
   - Connecting an external resistor network to this pin adjusts the default output voltage to any value starting from 0.6 V to V_{IN}.
2. Digital input for fixed default output voltage selection (TPS62401-Q1):
   - Having this pin tied to a low level sets the output voltage according to the value in register REG_DEF_1_Low. The default voltage is **1.575** V. having the pin tied to a high level sets the output voltage according to the value in register REG_DEF_1_High. The default value in this case is **1.1** V. The level of the DEF_1 pin selects between the two registers, REG_DEF_1_Low and REG_DEF_1_High, for the output-voltage setting. One can change the content of each register (and therefore output voltage) individually through the EasyScale interface. This makes the device very flexible in terms of output voltage setting; see Table 5.

180° OUT-OF-PHASE OPERATION

In PWM mode, the converters operate with a 180° turn-on phase shift of the PMOS (high side) transistors. This prevents the high-side switches of both converters from turning on simultaneously, and therefore smooths the input current. This feature reduces the surge current drawn from the supply.

SHORT-CIRCUIT PROTECTION

Both outputs are short-circuit protected with maximum output current = I_{LIMF}(P-MOS and N-MOS). Once the PMOS switch reaches its current limit, it turns off and the NMOS switch turns on. The PMOS only turns on again once the current in the NMOS decreases below the NMOS current limit.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the P- and N-Channel MOSFETs turn off. The device continues its operation when the junction temperature falls below the thermal-shutdown hysteresis.

EasyScale Interface: One-Pin Serial Interface for Dynamic Output Voltage Adjustment

General

The EasyScale interface is a simple but very flexible one-pin interface to configure the output voltage of both dc-dc converters. A master-slave structure is the basis of the interface, where the master is typically a microcontroller or application processor. Figure 34 and Table 4 give an overview of the protocol. The protocol consists of a device-specific address byte and a data byte. The device-specific address byte is fixed to 4E hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the **R**equest **F**or **A**cknowledge condition. The acknowledge condition only applies if the protocol was received correctly.

The advantage of the EasyScale interface compared to other one-pin interfaces is that its bit detection is to a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kb/s and up to 160kb/s. Furthermore, the interface shares the MODE/DATA pin and requires no additional pin.

Protocol

Transmission of all bits is MSB first and LSB last. Figure 35 shows the protocol without the acknowledge request (bit RFA = 0), Figure 36 with the acknowledge request (bit RFA = 1).

Prior to both bytes, device address byte and data byte, one must apply a start condition. For this, pull the MODE/DATA pin high for at least t_{Start} before the bit transmission starts with the falling edge. In case the MODE/DATA line was already at a high level (forced PWM mode selection), the device requires no application of a start condition prior to the device address byte.

Close the transmission of each byte with an end-of-stream condition for at least t_{EOS}.

Addressable Registers

Three registers with a data content of 5 bits are addressable. With 5-bit data content, 32 different values for each register are available. Table 2 shows the addressable registers to set the output voltage when the DEF_1 pin works as a digital input. In this case, converter 1 has a related register for each DEF_1 pin condition, and one register for converter 2. A high or low condition on pin DEF_1 (TPS62401-Q1) selects either the content of register REG_DEF_1_high or REG_DEF1_low, thus setting the output voltage of converter 1 according to the values in Table 5.

Table 3 shows the addressable registers if the DEF_1 pin acts as an analog input with external resistors connected. In this case, one register is available for each converter. The values in Table 6 set the output voltage of converter 1. Table 7 shows the available voltages for converter 2. Use of a precise internal resistor divider network to generate these output voltages makes external resistors unnecessary (less board space) and provides higher output voltage accuracy. Enabling at least one of the converters (EN1 or EN2 is high) activates the interface. After the startup-time t_{Start} (170 µs), the interface is ready for data reception.

Table 2. Addressable Registers for Default Fixed-Output Voltage Options (PIN DEF_1 = Digital Input)

DEVICE	REGISTER	DESCRIPTION	DEF_1 PIN	A1	A0	D4	D3	D2	D1	D0
TPS62401-Q1, TPS62402-Q1, TPS62403-Q1, TPS62404-Q1, TPS62405-Q1	REG_DEF_1_High	Converter 1 output voltage setting for DEF_1 = High condition. The content of the register is active with the DEF_1 pin high.	High	0	1	Output voltage setting, see Table 5				
	REG_DEF_1_Low	Converter 1 output voltage setting for DEF_1 = Low condition.	Low	0	0	Output voltage setting, see Table 5				
	REG_DEF_2	Converter 2 output voltage	Not applicable	1	0	Output voltage setting, see Table 7				
		Do no't use		1	1					

Table 3. Addressable Registers for Adjustable-Output Voltage Options (PIN DEF_1 = Analog Input)

DEVICE	REGISTER	DESCRIPTION	A1	A0	D4	D3	D2	D1	D0
TPS62400-Q1	REG_DEF_1_High	Not available							
	REG_DEF_1_Low	Converter 1 output-voltage setting	0	0	see Table 6				
	REG_DEF_2	Converter 2 output voltage	1	0	see Table 7				
		Don't use	1	1					

Bit Decoding

The bit detection is based on a PWM scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High bit: $t_{High} > t_{Low}$, but with t_{High} at least 2× t_{Low}, see Figure 34.

Low bit: $t_{Low} > t_{High}$, but with t_{Low} at least 2× t_{High}, see Figure 34.

The bit detection starts with a falling edge on the MODE/DATA pin and ends with the next falling edge. Detection of a 0 or 1 depends on the relation between t_{Low} and t_{High}.

Acknowledge

The device only applies the acknowledge condition if:

- A set RFA bit requests an acknowledge
- The transmitted device address matches with the device address of the device
- Correct reception of 16 bits occurred

In this case, the device turns on the internal ACKN-MOSFET and pulls the MODE/DATA pin low for the time t_{ACKN}, which is 520 µs maximum. The acknowledge condition is valid after an internal delay time t_{valACK}. This means the internal ACKN-MOSFET turns on after t_{valACK}, on detection of the last falling edge of the protocol. The master controller keeps the line low during this time.

The master device can detect the acknowledge condition with its input by releasing the MODE/DATA pin after t_{valACK} and reading back a 0.

In case of an invalid device address, or not-correctly-received protocol, application of a no-acknowledge condition does not occur; thus, the internal MOSFET does not turn on, and the external pullup resistor pulls the MODE/DATA pin high after t_{valACK}. One can use the MODE/DATA pin again after the acknowledge condition ends.

NOTE

The master device must have an open-drain output in order to request the acknowledge condition.

In case of a push-pull output stage, TI recommends using a series resistor in the MODE/DATA line to limit the current to 500 µA in case of an accidentally requested acknowledge, to protect the internal ACKN-MOSFET.

MODE Selection

Use of the MODE/DATA pin for two functions, interface and a MODE selection, necessitates a determination of when it to decode the bit stream or to change the operation mode.

The device enters forced PWM mode operation immediately whenever the MODE/DATA pin turns to high level. The device also stays in forced PWM mode during the entire protocol reception time.

With a falling edge on the MODE/DATA pin, the device starts bit decoding. If the MODE/DATA pin stays low for at least $t_{timeout}$, the device gets an internal time-out and enables power-save-mode operation.

The device ignores a protocol sent within this time because the first interpretation of a falling edge for the mode change is as the start of the first bit. In this case, TI recommends sending the protocol first, and then changing at the end of the protocol to power-save mode.

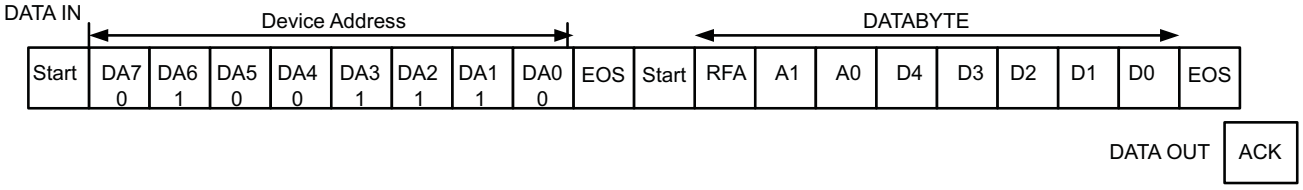


Figure 34. EasyScale Protocol Overview

Table 4. EasyScale Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device address byte	7	DA7	IN	0 MSB device address
	6	DA6	IN	1
	5	DA5	IN	0
	4	DA4	IN	0
4E hex	3	DA3	IN	1
	2	DA2	IN	1
	1	DA1	IN	1
	0	DA0	IN	0 LSB device address
Data byte	7 (MSB)	RFA	IN	Request for acknowledge; if high, the device applies an acknowledge condition
	6	A1		Address bit 1
	5	A0		Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, the device applies this condition only in the case of a set RFA bit. Open-drain output, the host must pull the line high with a pullup resistor. One can only use this feature if the master has an open-drain output stage. In case of a push pull-output stage, do not request an acknowledge condition.

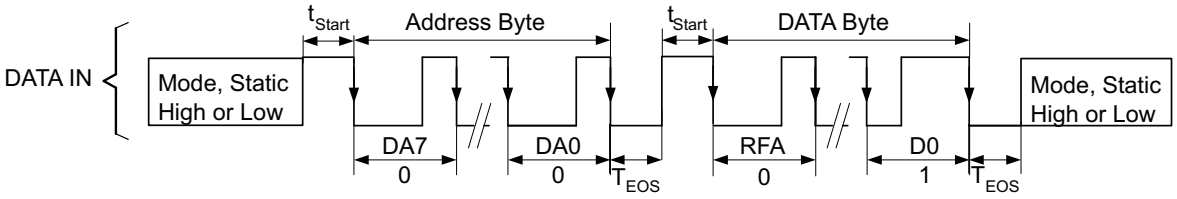


Figure 35. EasyScale Protocol Without Acknowledge

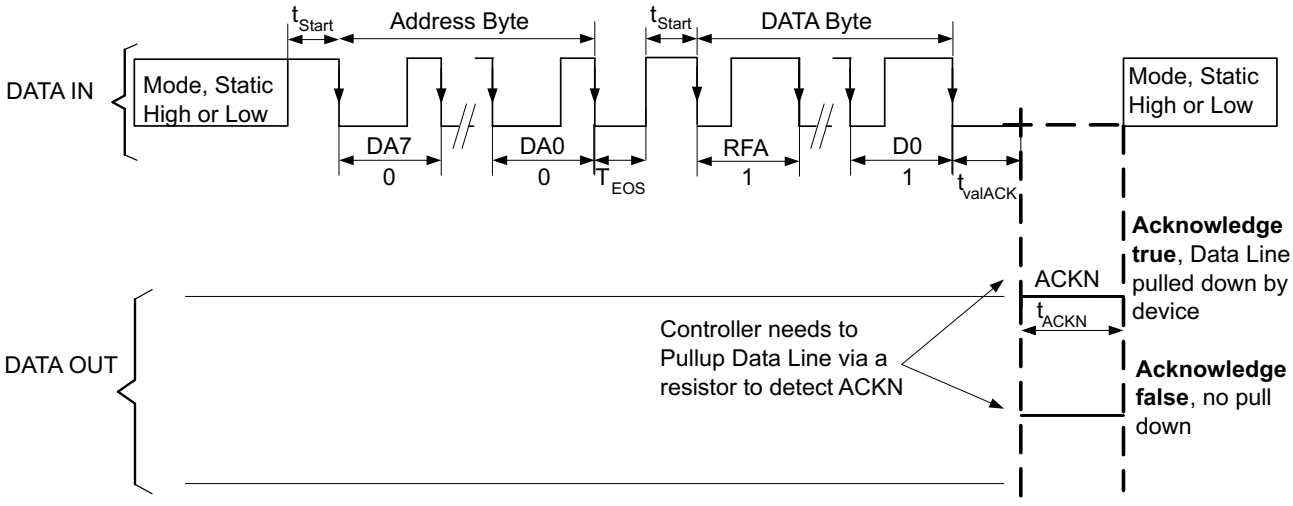


Figure 36. EasyScale Protocol Including Acknowledge

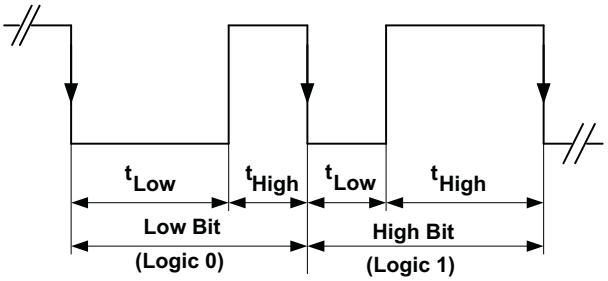


Figure 37. EasyScale – Bit Coding

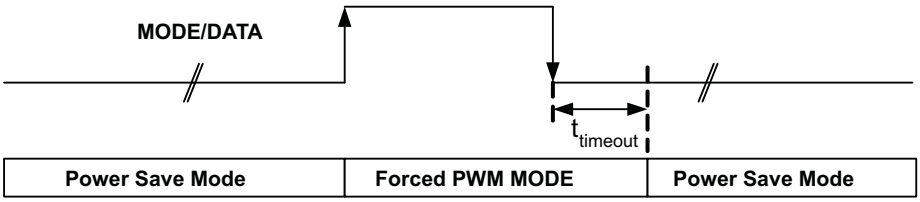


Figure 38. MODE/DATA PIN: Mode Selection

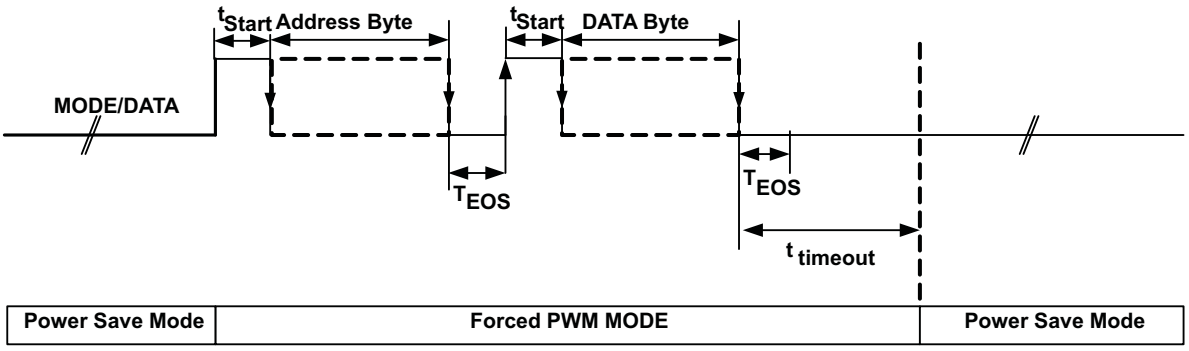


Figure 39. MODE/DATA Pin: Power-Save-Mode and Interface Communication

Table 5. Selectable Output Voltages for Converter 1, With Pin DEF_1 as Digital Input (TPS62401-Q1)

	TPS62401-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	TPS62401-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_HIGH	D4	D3	D2	D1	D0
0	0.8	0.9	0	0	0	0	0
1	0.825	0.925	0	0	0	0	1
2	0.85	0.95	0	0	0	1	0
3	0.875	0.975	0	0	0	1	1
4	0.9	1.0	0	0	1	0	0
5	0.925	1.025	0	0	1	0	1
6	0.95	1.050	0	0	1	1	0
7	0.975	1.075	0	0	1	1	1
8	1.0	**1.1 (default TPS62401-Q1, TPS62403-Q1)**	**0**	**1**	**0**	**0**	**0**
9	1.025	1.125	0	1	0	0	1
10	1.050	1.150	0	1	0	1	0
11	1.075	1.175	0	1	0	1	1
12	1.1	1.2	0	1	1	0	0
13	1.125	1.225	0	1	1	0	1
14	1.150	1.25	0	1	1	1	0
15	1.175	1.275	0	1	1	1	1
16	1.2 **(default TPS62402-Q1)** 1.215 **(default TPS62405-Q1)**	1.3	1	0	0	0	0
17	1.225	1.325	1	0	0	0	1
18	1.25	1.350	1	0	0	1	0
19	1.275	1.375	1	0	0	1	1
20	1.3	1.4	1	0	1	0	0
21	1.325	1.425	1	0	1	0	1
22	1.350	1.450	1	0	1	1	0
23	1.375	1.475	1	0	1	1	1
24	1.4	1.5	1	1	0	0	0
25	1.425	1.525	1	1	0	0	1
26	1.450	1.55	1	1	0	1	0
27	1.475	1.575	1	1	0	1	1
28	1.5	1.6	1	1	1	0	0
29	1.525	1.7	1	1	1	0	1
30	1.55	1.8 **(default TPS62402-Q1)**	1	1	1	1	0
31	1.575 **(default TPS62401-Q1, TPS62403-Q1, TPS62404-Q1)**	1.9 **(default TPS62402-Q1)** 1.925 **(default TPS62405-Q1)**	**1**	**1**	**1**	**1**	**1**

Table 6. Selectable Output Voltages for Converter 1, With DEF1 Pin as Analog Input (Adjustable, TPS62400-Q1)

	TPS62400-Q1 OUTPUT VOLTAGE [V] REGISTER REG_DEF_1_LOW	D4	D3	D2	D1	D0
0	**V_{OUT1} Adjustable with Resistor Network on DEF_1 Pin (default TPS62400-Q1)**	**0**	**0**	**0**	**0**	**0**
	0.6 V with DEF_1 connected to V_{OUT1} (default TPS62400-Q1)					
1	0.825	0	0	0	0	1
2	0.85	0	0	0	1	0
3	0.875	0	0	0	1	1
4	0.9	0	0	1	0	0
5	0.925	0	0	1	0	1
6	0.95	0	0	1	1	0
7	0.975	0	0	1	1	1
8	1.0	0	1	0	0	0
9	1.025	0	1	0	0	1
10	1.050	0	1	0	1	0
11	1.075	0	1	0	1	1
12	1.1	0	1	1	0	0
13	1.125	0	1	1	0	1
14	1.150	0	1	1	1	0
15	1.175	0	1	1	1	1
16	1.2	1	0	0	0	0
17	1.225	1	0	0	0	1
18	1.25	1	0	0	1	0
19	1.275	1	0	0	1	1
20	1.3	1	0	1	0	0
21	1.325	1	0	1	0	1
22	1.350	1	0	1	1	0
23	1.375	1	0	1	1	1
24	1.4	1	1	0	0	0
25	1.425	1	1	0	0	1
26	1.450	1	1	0	1	0
27	1.475	1	1	0	1	1
28	1.5	1	1	1	0	0
29	1.525	1	1	1	0	1
30	1.55	1	1	1	1	0
31	1.575	1	1	1	1	1

Table 7. Selectable Output Voltages for Converter 2, (ADJ2 Connected to V_{OUT})

	OUTPUT VOLTAGE [V] FOR REGISTER REG_DEF_2	D4	D3	D2	D1	D0
0	**V_{OUT2} Adjustable with resistor network and C_{ff} on ADJ2 pin (default TPS62400-Q1)**	**0**	**0**	**0**	**0**	**0**
	0.6 V with ADJ2 pin directly connected to V_{OUT2} (default TPS62400-Q1)					
1	0.85	0	0	0	0	1
2	0.9	0	0	0	1	0
3	0.95	0	0	0	1	1
4	1	0	0	1	0	0
5	1.05	0	0	1	0	1
6	1.1	0	0	1	1	0
7	1.15	0	0	1	1	1
8	1.2	0	1	0	0	0
9	1.25	0	1	0	0	1
10	1.3	0	1	0	1	0
11	1.35	0	1	0	1	1
12	1.4	0	1	1	0	0
13	1.45	0	1	1	0	1
14	1.5	0	1	1	1	0
15	1.55	0	1	1	1	1
16	1.6	1	0	0	0	0
17	1.7	1	0	0	0	1
18	**1.8 (default TPS62401-Q1)**	1	0	0	1	0
19	1.85	1	0	0	1	1
20	2	1	0	1	0	0
21	2.1	1	0	1	0	1
22	2.2	1	0	1	1	0
23	2.3	1	0	1	1	1
24	2.4	1	1	0	0	0
25	2.5	1	1	0	0	1
26	2.6	1	1	0	1	0
27	2.7	1	1	0	1	1
28	**2.8 (default TPS62403-Q1)**	1	1	1	0	0
29	2.85	1	1	1	0	1
30	3	1	1	1	1	0
31	3.3 **(default TPS62402-Q1, TPS62404-Q1)** 3.35 **(default TPS62405-Q1)**	1	1	1	1	1

APPLICATION INFORMATION

OUTPUT VOLTAGE SETTING

Converter 1 Adjustable Default Output-Voltage Setting: TPS62400-Q1

Calculate the output voltage as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{11}}{R_{12}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (4)$$

To keep the operating current to a minimum, TI recommends selecting R12 within a range of 180 kΩ to 360 kΩ. The sum of R_{12} and R_{11} should not exceed approximately 1 MΩ. For higher output voltages than 3.3 V, TI recommends choosing lower values than 180 kΩ for R12. Route the DEF_1 line away from noise sources, such as the inductor or the SW1 line. The FB1 line requires a direct connection to the output capacitor. A feedforward capacitor is not necessary.

Converter 1 Fixed Default Output-Voltage Setting (TPS62401-Q1, TPS62402-Q1, TPS62403-Q1, TPS62404-Q1, TPS62405-Q1)

The DEF_1 pin selects output voltage $\mathbf{V_{OUT1}}$.

Pin DEF_1 = low:

TPS62401-Q1, TPS62403-Q1, TPS62404-Q1 = 1.575 V

TPS62402-Q1 = 1.2 V

TPS62405-Q1 = 1.215 V

Pin DEF_1 = high:

TPS62401-Q1, TPS62403-Q1 = 1.1 V

TPS62402-Q1: = 1.8 V

TPS62404-Q1 = 1.9

TPS62405-Q1 : = 1.925 V

Converter 2 Adjustable Default Output-Voltage Setting (TPS62400-Q1):

One can set the output voltage of converter 2 by an external resistor network. For converter 2, the same recommendations apply as for converter 1. In addition to that, use a 33-pF feedforward capacitor C_{ff2} for good load transient response. Calculate the output voltage as:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{21}}{R_{22}}\right) \text{ with an internal reference voltage } V_{REF} \text{ typical 0.6V} \quad (5)$$

Converter 2 Fixed Default Output-Voltage Setting

ADJ2 pin must be directly connected with V_{OUT2}

TPS62401-Q1, V_{OUT2} default = 1.8 V

TPS62403-Q1, V_{OUT2} default = 2.8 V

TPS62402-Q1, V_{OUT2} default = 3.3 V

TPS62404-Q1, V_{OUT2} default = 3.3 V

TPS62405-Q1, V_{OUT2} default = 3.35 V

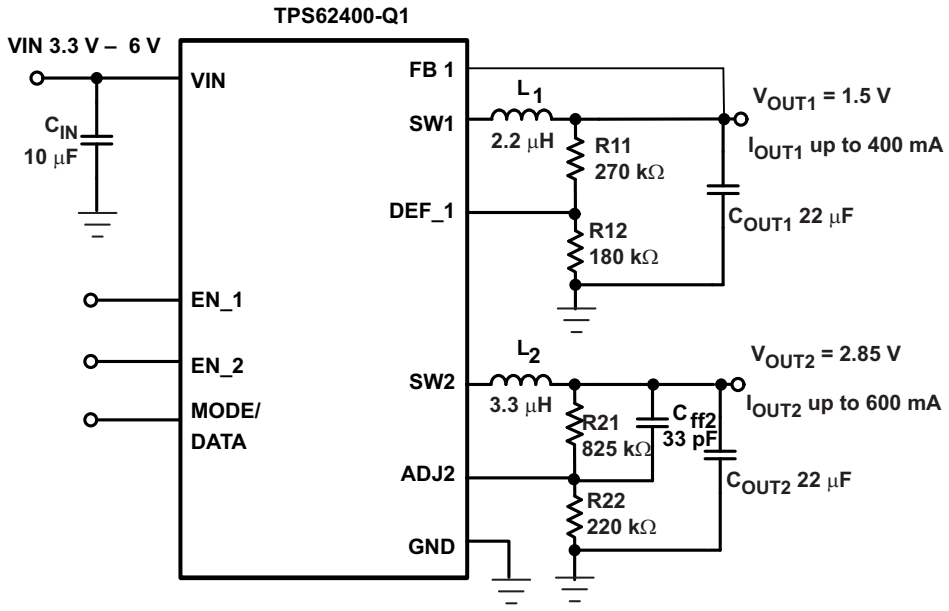


Figure 40. Typical Application Circuit 1.5-V and 2.85-V Adjustable Outputs, Low PFM Voltage Ripple Optimized

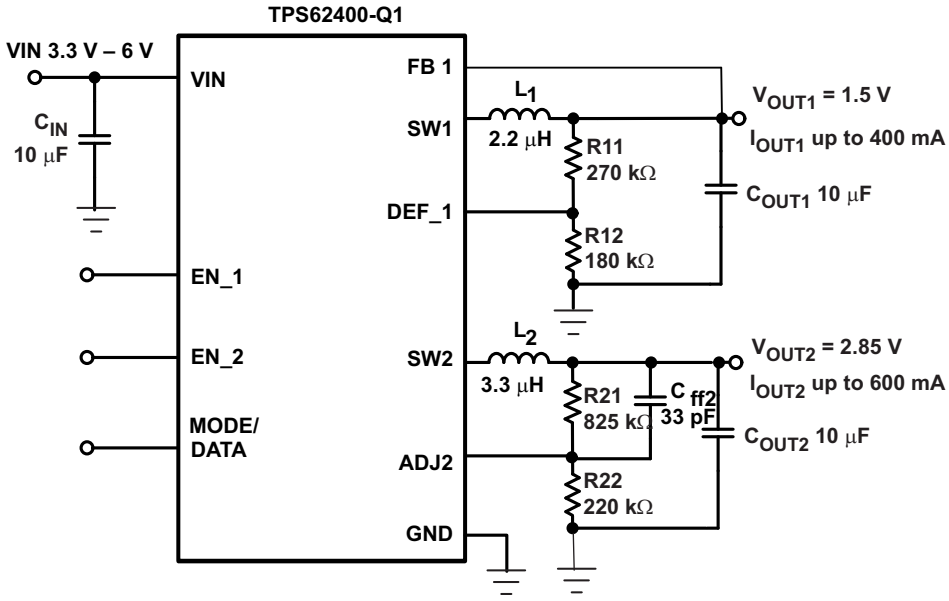


Figure 41. Typical Application Circuit 1.5-V and 2.85-V Adjustable Outputs

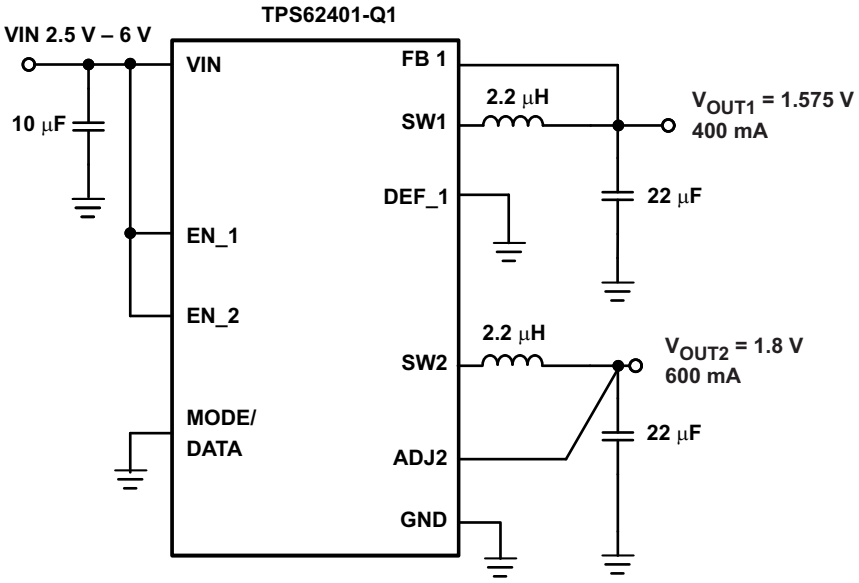


Figure 42. TPS62401-Q1 Fixed 1.575-V and 1.8-V Outputs, Low PFM Voltage Ripple Optimized

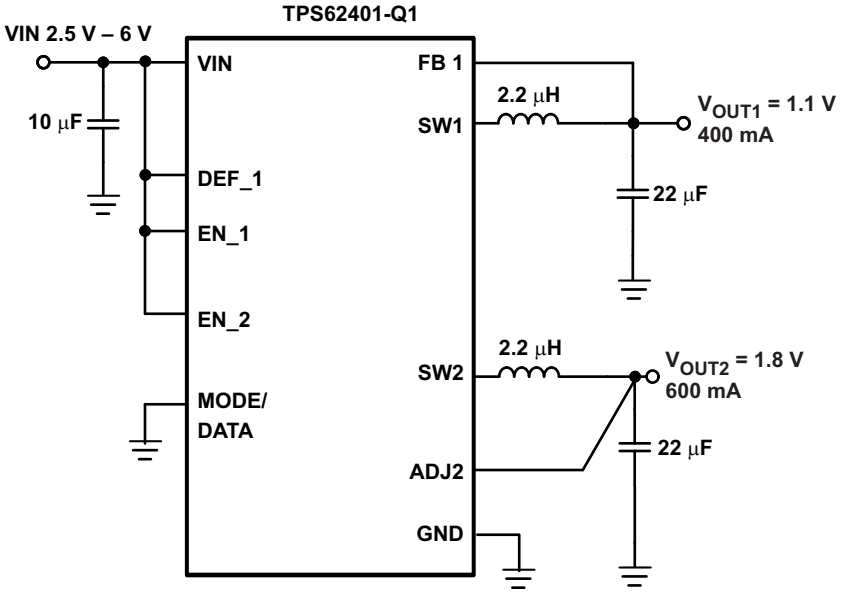


Figure 43. TPS62401-Q1 Fixed 1.1-V and 1.8-V Outputs, Low PFM Ripple Voltage Optimized

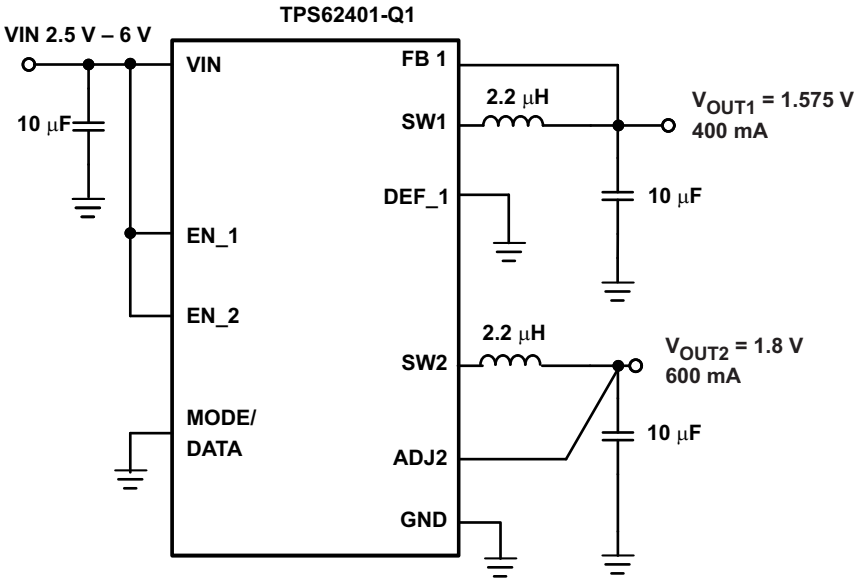


Figure 44. TPS62401-Q1 Fixed 1.575-V and 1.8-V Outputs

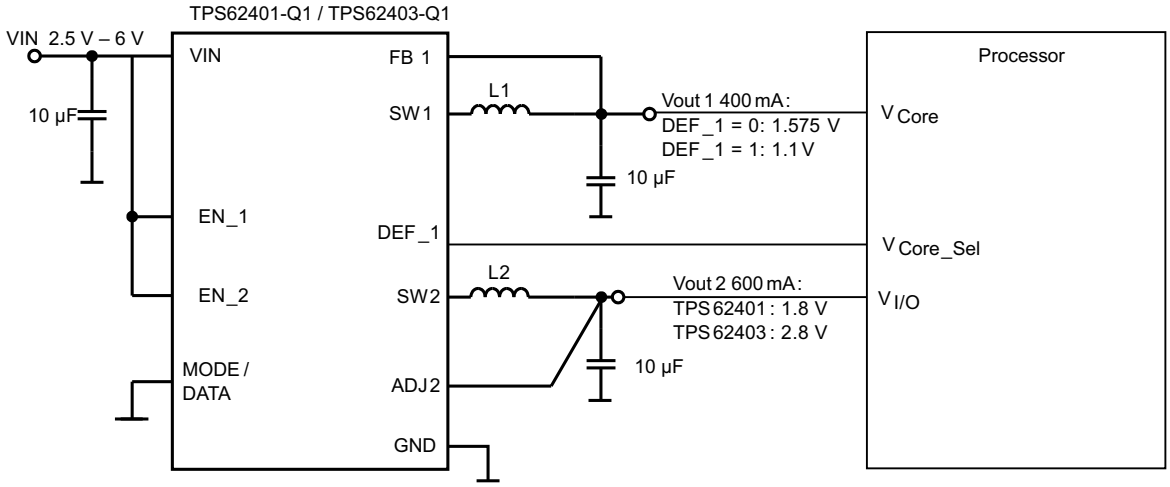


Figure 45. Dynamic Voltage Scaling on V_{OUT1} Controlled by DEF_1 Pin

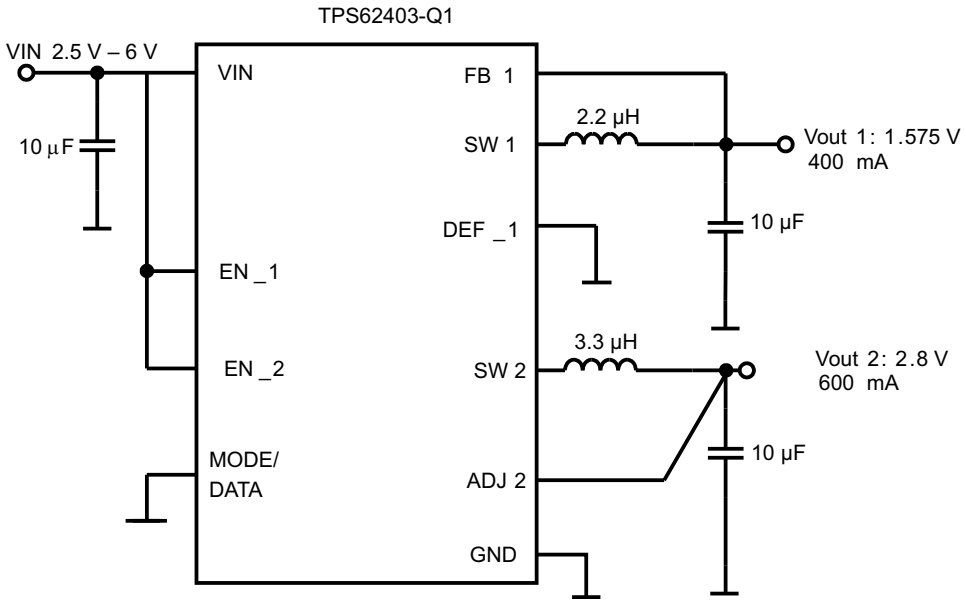


Figure 46. TPS62403-Q1 1.575-V and 2.8-V Outputs

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The converters operate with a minimum inductance of 1.75 µH and minimum capacitance of 6 µF. The device operation is optimum with inductors of 2.2 µH to 4.7 µH and output capacitors of 10 µF to 22 µF.

Inductor Selection

Select the inductor based on its ratings for dc resistance and saturation current. The dc resistance of the inductor directly influences the efficiency of the converter. Therefore, select an inductor with lowest dc resistance for highest efficiency.

Equation 6 calculates the maximum inductor current under static load conditions. The saturation-current rating of the inductor should be higher than the maximum inductor current as calculated with Equation 7. TI makes this recommendation because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (6)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (7)$$

with:

f = Switching frequency (2.25 MHz typical)

L = Inductor value

ΔI_L = Peak-to-peak inductor ripple current

I_{Lmax} = Maximum inductor current

The highest inductor current occurs at maximum Vin.

Open-core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Take into consideration that the core material from inductor to inductor differs, and this difference has an impact on the efficiency.

See Table 8 and the typical application circuit examples for possible inductors.

Table 8. List of Inductors

DIMENSIONS [mm]	INDUCTOR TYPE	SUPPLIER
3.2 × 2.6 × 1	MIPW3226	FDK
3 × 3 × 0.9	LPS3010	Coilcraft
2.8 × 2.6 × 1	VLF3010	TDK
2.8 x 2.6 × 1.4	VLF3014	TDK
3 × 3 × 1.4	LPS3015	Coilcraft
3.9 × 3.9 × 1.7	LPS4018	Coilcraft

Output-Capacitor Selection

The advanced fast-response voltage-mode control scheme of the converters allows the use of tiny ceramic capacitors with a typical value of 10 µF to 22 µF, without having large output-voltage under- and overshoots during heavy load transients. Ceramic capacitors with low ESR values result in lowest output-voltage ripple, and TI therefore recommends them. The output capacitor requires either X7R or X5R dielectric. TI does not recommend Y5V and Z5U dielectric capacitors due to their wide variation in capacitance.

If using ceramic output capacitors, the capacitor rms ripple-current rating always meets the application requirements. The rms ripple current calculation is:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR, plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (9)$$

where the highest output-voltage ripple occurs at the highest input voltage, Vin.

At light load currents, the converters operate in power-save mode and the output-voltage ripple depends on the output-capacitor value. The internal comparator delay and the external capacitor set the output-voltage ripple. Higher output capacitors like 22 µF values minimize the voltage ripple in PFM mode and tighten dc output accuracy in PFM mode.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, the device requires a low-ESR input capacitor to prevent large voltage transients that can cause misbehavior of the device or interference with other circuits in the system. An input capacitor of 10 µF is sufficient.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Take care in board layout to get the specified performance. Without careful layout, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold in Figure 47.

Place the input capacitor as close as possible to the IC pins VIN and GND, the inductor and output capacitor as close as possible to the pins SW1 and GND.

Connect the GND pin of the device to the PowerPAD of the PCB and use this pad as a star point. For each converter, use a common power GND node and a different node for the signal GND to minimize the effects of ground noise. Connect these ground nodes together to the PowerPAD (star point) underneath the IC. Keep the common path to the GND PIN, which returns the small signal components and the high current of the output capacitors, as short as possible to avoid ground noise. Connect the output voltage-sense lines (FB 1, DEF_1, ADJ2) right to the output capacitor and route them away from noisy components and traces (for example, the SW1 and SW2 lines). If operating the EasyScale interface with high transmission rates, route the MODE/DATA trace away from the ADJ2 line to avoid capacitive coupling into the ADJ2 pin. A GND guard ring between the MODE/DATA pin and ADJ2 pin avoids potential noise coupling.

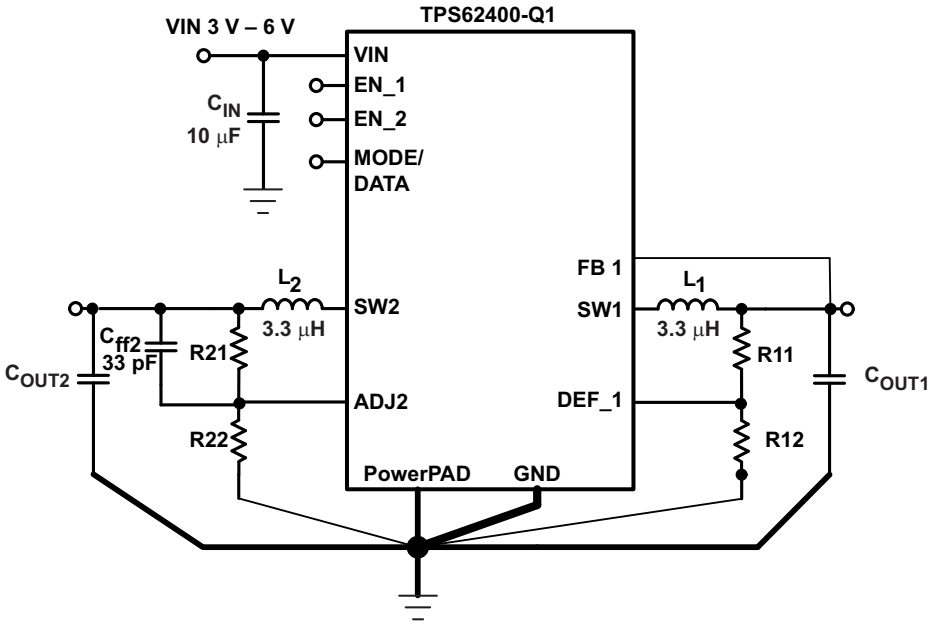


Figure 47. Layout Diagram

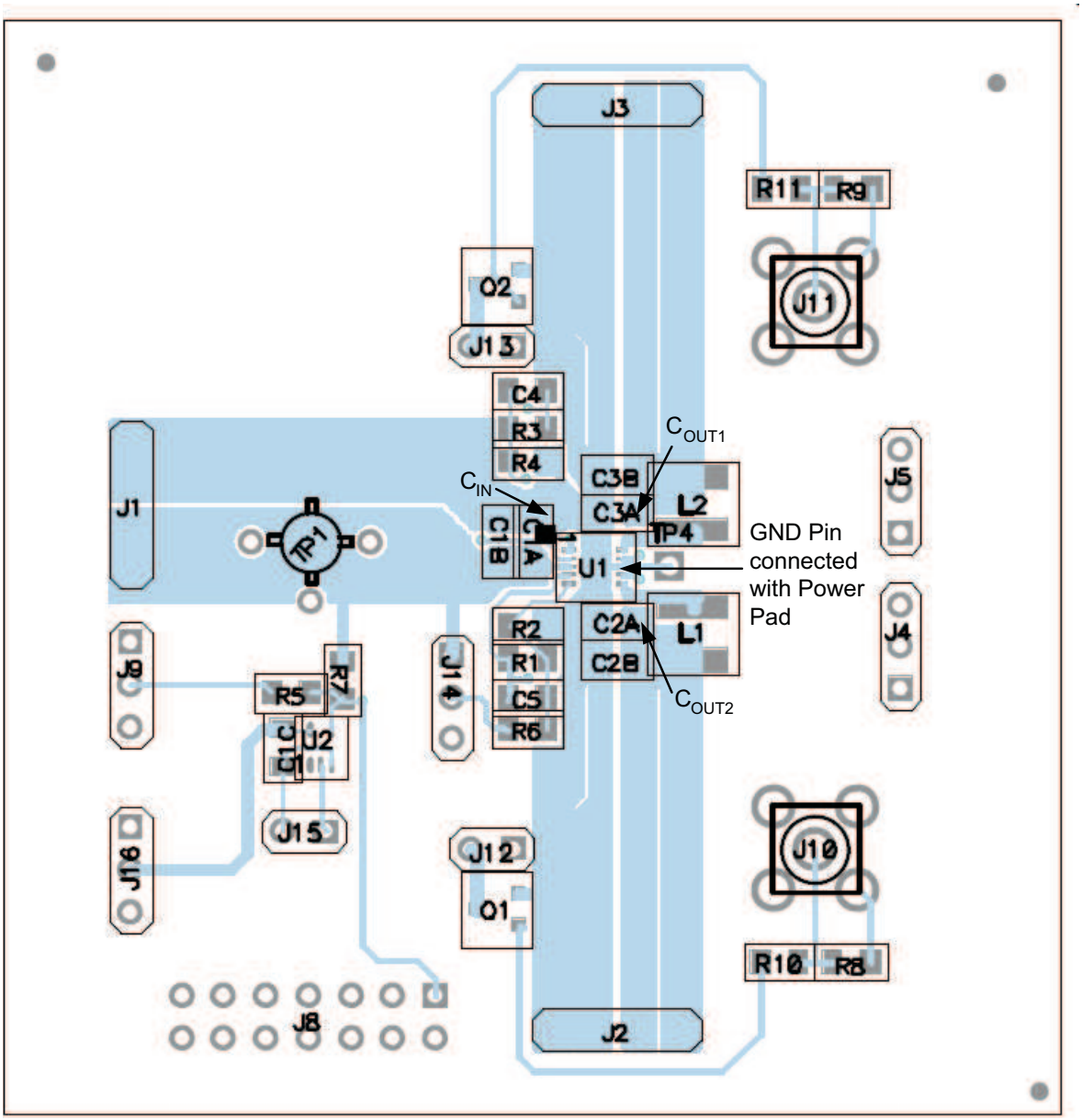


Figure 48. PCB Layout

REVISION HISTORY

Changes from Revision A (March, 2013) to Revision B **Page**

- Changed Ordering Information table 2
- Changed OUT1 from DEF_1 = High 1.9 V to DEF_1 = High 1.925 V and DEF_1 = Low 1.575 V to DEF_1 = Low 1.215 V. Changed OUT2 from Fixed default 5 V to Fixed default 3.35 V. 2
- Added part number to Device column 22
- Added 1.215 (default TPS62405-Q1) in row 16, Table 5. 26
- Added part number to Table 5 26
- Removed TPS62405-Q1 from Table 5. 26
- Added 1.925 (default TPS62405-Q1) in row 31, Table 5. 26
- Added part number to row 31, Table 5 28
- Added part number to Converter 1 Fixed Default Output-Voltage Setting heading 29
- Added voltage for TPS62402-Q1 to Converter 1 Fixed for DEF_1 = low 29
- Changed voltage from 1.2 V to 1.215 V for Pin DEF_1 = low 29
- Added part number TPS62405-Q1 for Pin DEF_1 = high 29
- Added part number and voltage to Converter 2 Fixed Default Output-Voltage Setting section 29
- Changed TPS62405-Q1, V_{OUT2} default = 5 V to 3.35 V. 29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62400QDRCRQ1	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	SHI	Samples
TPS62402QDRCRQ1	PREVIEW	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	SJS	
TPS62404QDRCRQ1	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OET	Samples
TPS62405QDRCRQ1	PREVIEW	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	SJT	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62400-Q1, TPS62402-Q1, TPS62404-Q1 :

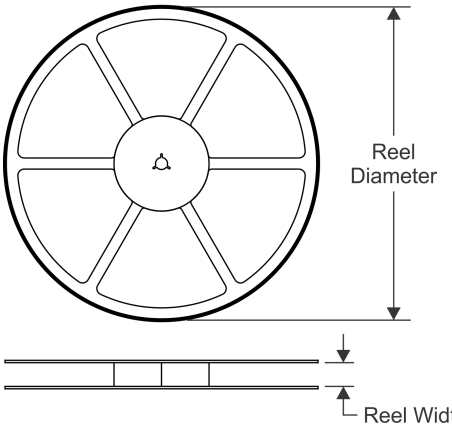
- Catalog: TPS62400, TPS62402, TPS62404

NOTE: Qualified Version Definitions:

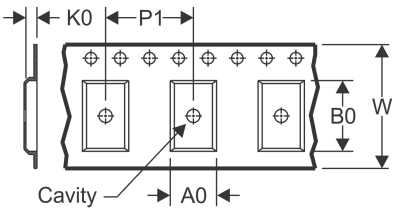
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

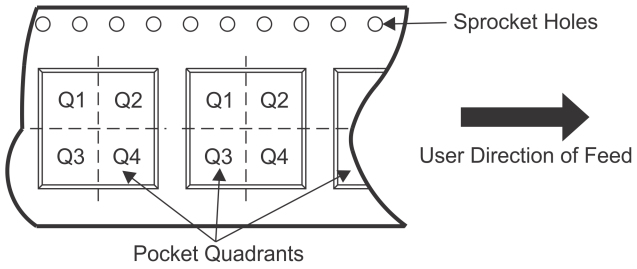


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

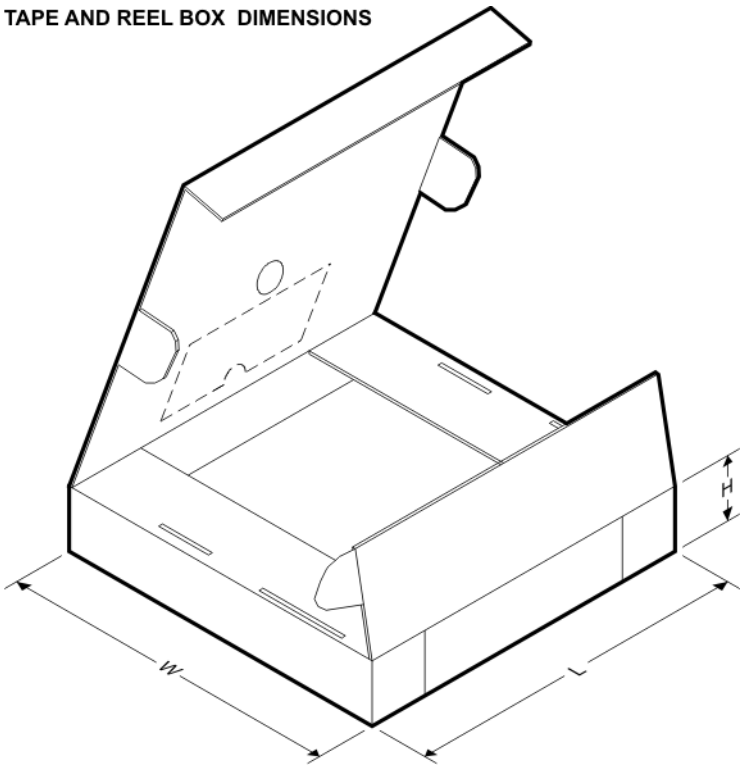
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62400QDRCRQ1	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62404QDRCRQ1	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

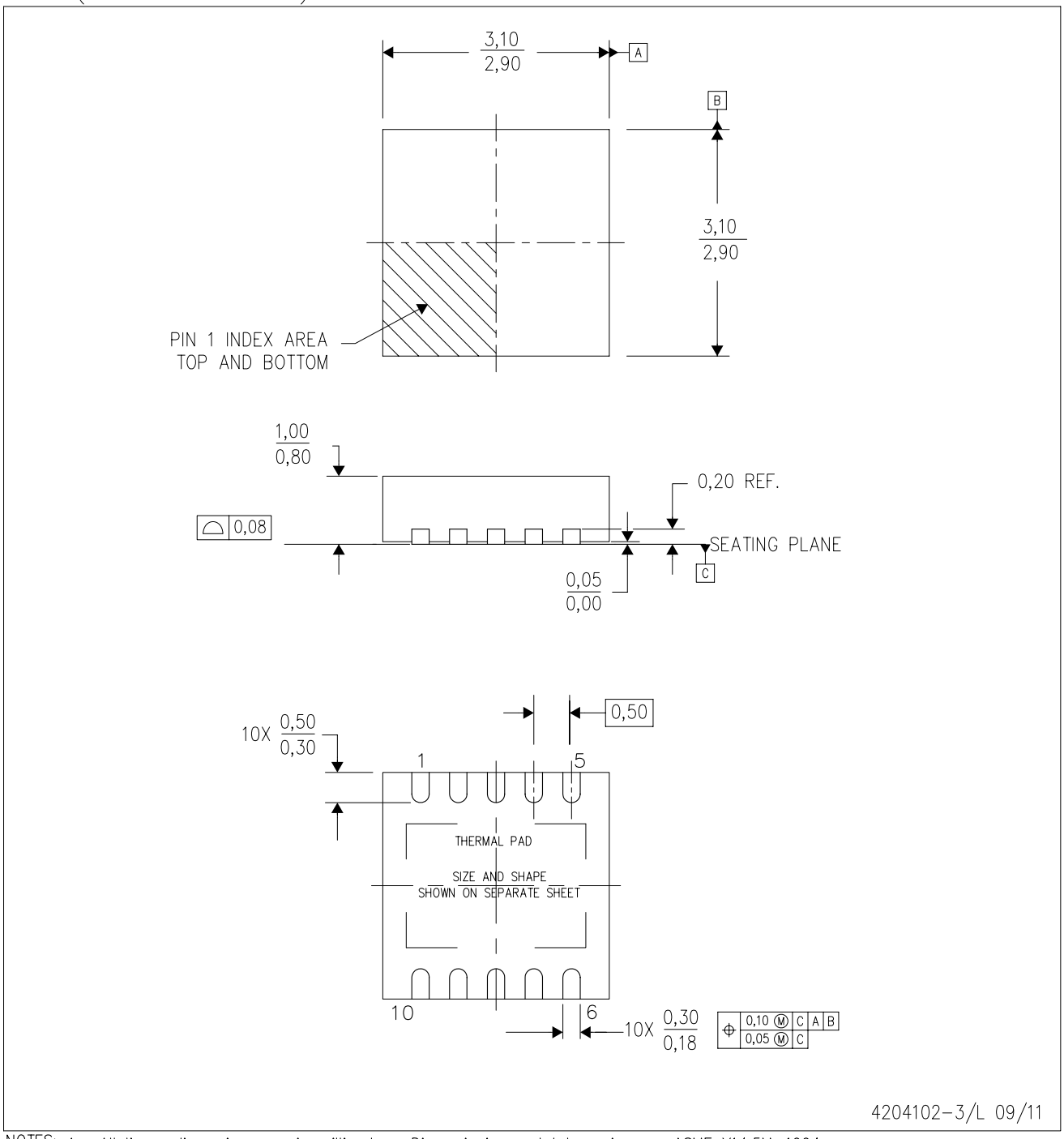
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62400QDRCRQ1	SON	DRC	10	3000	367.0	367.0	35.0
TPS62404QDRCRQ1	SON	DRC	10	3000	367.0	367.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

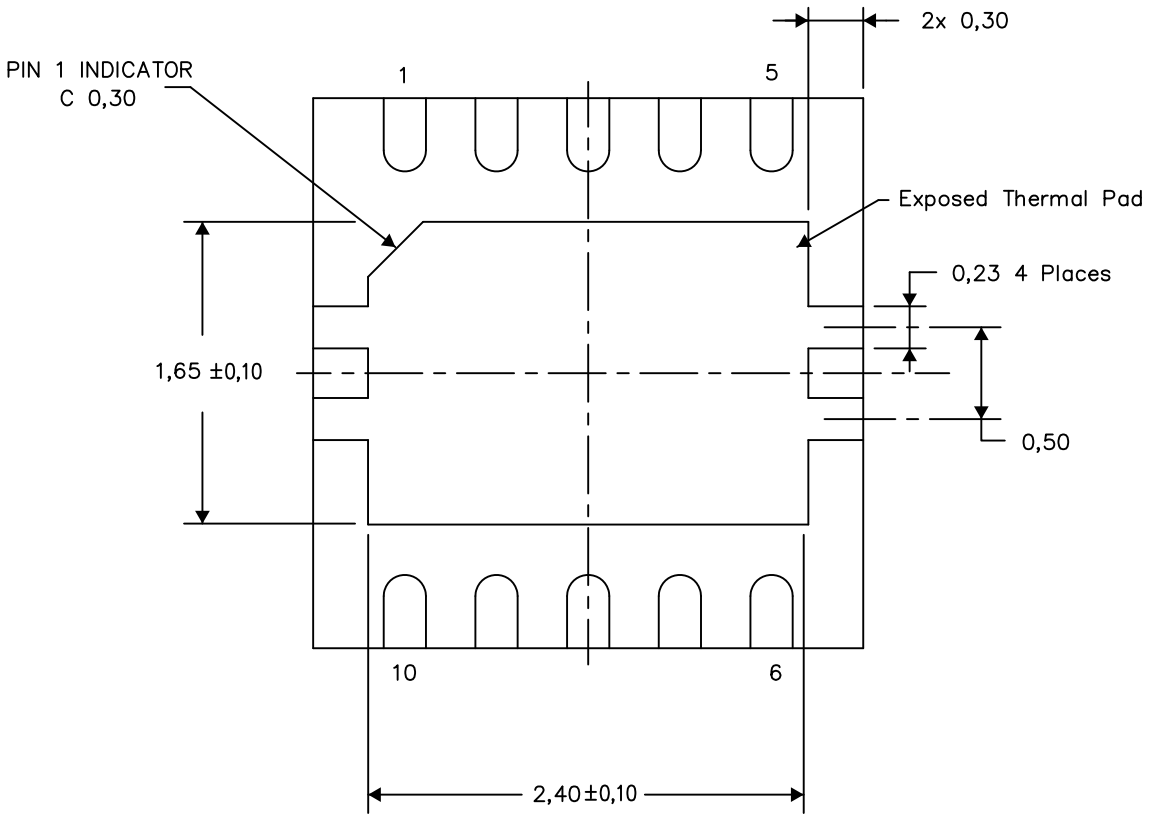
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



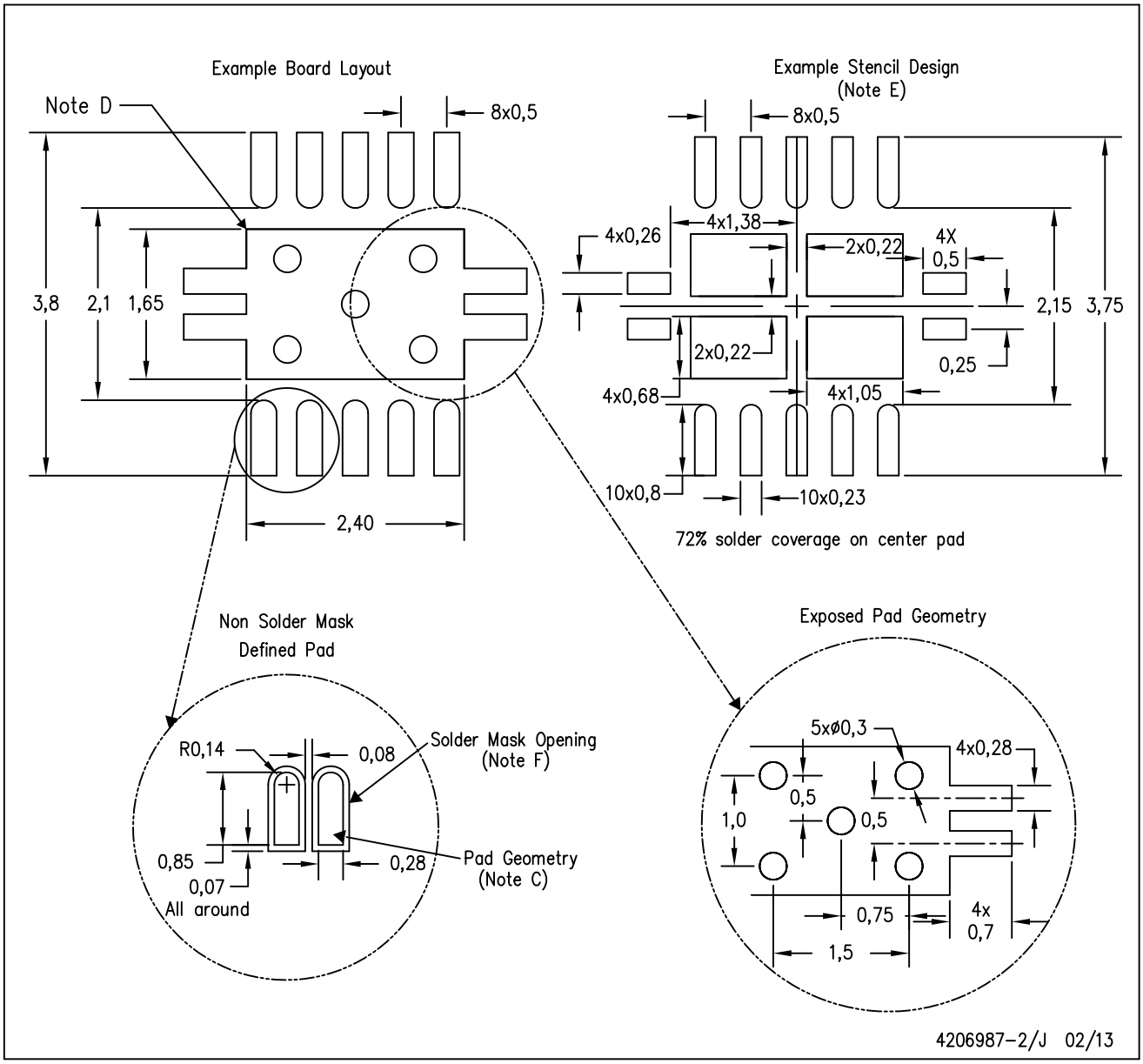
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/R 03/13

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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