TARGET SPEC

M5M4V181600AJ,TP,RT-6,-7,-8

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

MITSUBISHI (MEMORY/ASIC)

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V181600AXX-6	60	15	30	15	120	300
M5M4V181600AXX-7	70	20	35	20	140	260
M5M4V181600AXX-8	80	20	40	20	160	160

XX=J,TP,RT

- Standard 42 pin SOJ,50 pin TSOP
- Single 3.3V ±0.3V supply
- Low stand-by power dissipation
  3.6mW (Max) ····· CMOS Input level
- Low operating power dissipation
  M5M4V181600Axx- 6 ---------- 360.0mW (Max)
  M5M4V181600Axx- 7 ---------- 310.0mW (Max)
  M5M4V181600Axx- 8 ---------- 270.0mW (Max)

- Fast-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~ A_9)

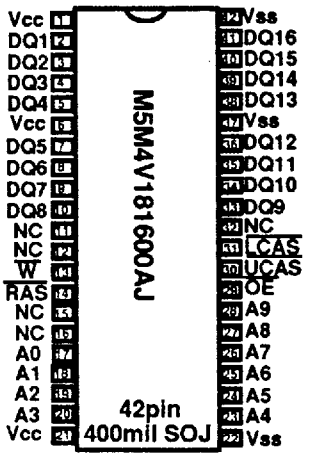
APPLICATION

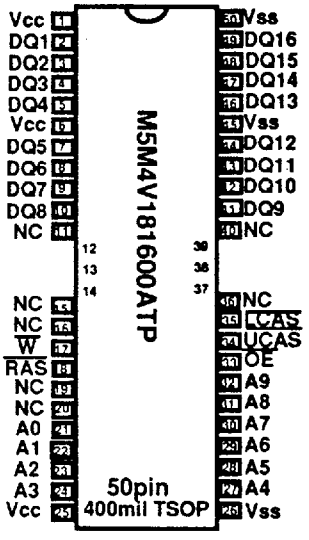
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

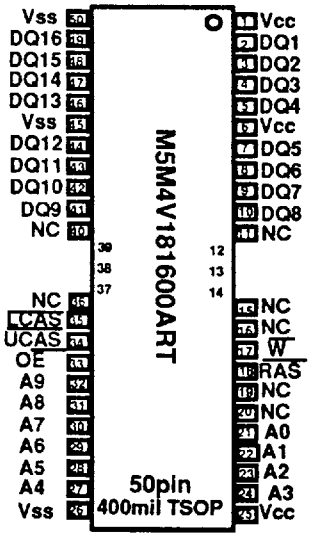
PIN DESCRIPTION

Pin Name	Function
A_0-A_9	Address Inputs
DQ_1-DQ_{16}	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{UCAS}$	Upper Bite Control Column Address Strobe Input
$\overline{LCAS}$	Lower Bite Control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)







MITSUBISHI ELECTRIC

M5M4V181600AJ,TP,RT-6,-7,-8

MITSUBISHI (MEMORY/ASIC)

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

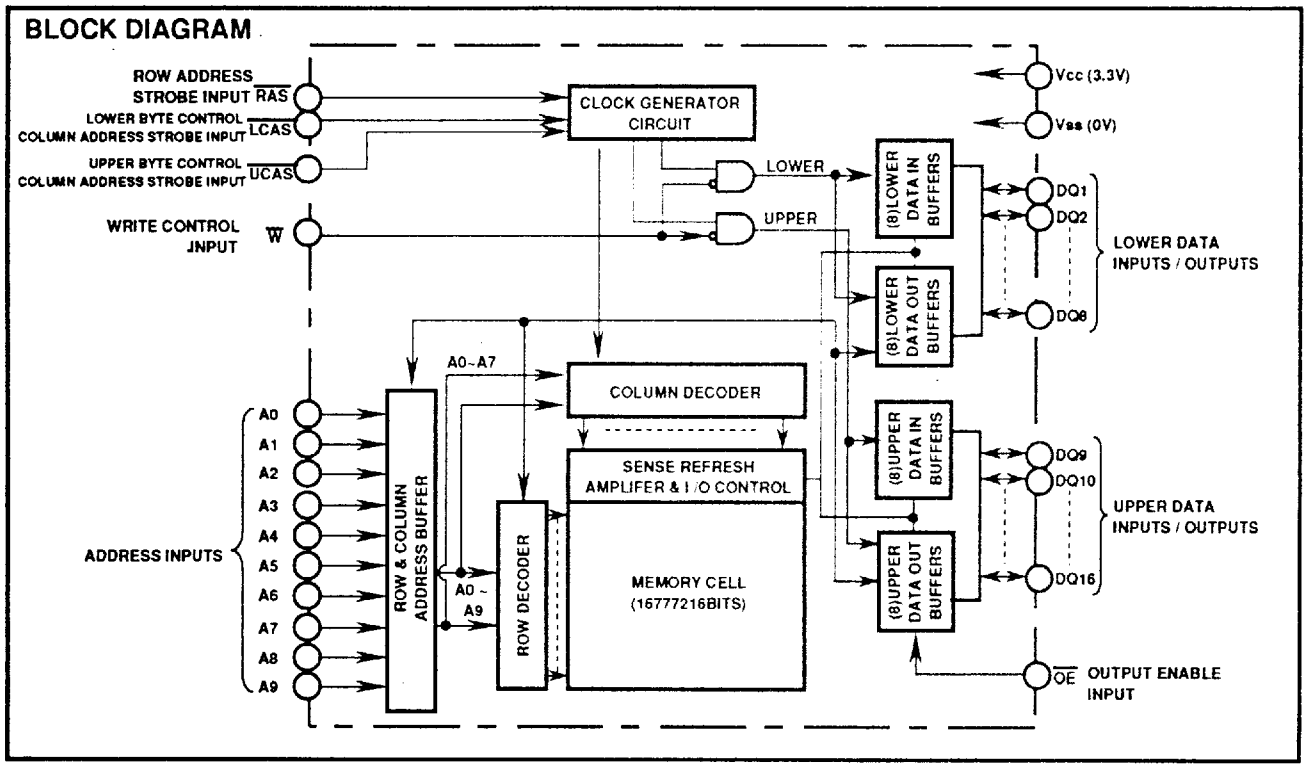
The M5M4V181600AJ, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid,APD : applied, OPN : open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-0.5～4.6	V
V1	Input voltage		-0.5～4.6	V
V0	Output voltage		-0.5～4.6	V
I0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	3.0	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		3.6	V
V_{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-3.3mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.8mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	-10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M4V181600A-6	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V181600A-7				160	
		M5M4V181600A-8				145	
I_{CC2}	Supply current from Vcc , stand-by (Note 5)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH} output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$≧Vcc -0.2			0.5	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M4V181600A-6	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			180	mA
		M5M4V181600A-7				160	
		M5M4V181600A-8				145	
I_{CC4}(AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4,5)	M5M4V181600A-6	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			180	mA
		M5M4V181600A-7				160	
		M5M4V181600A-8				145	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4V181600A-6	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			160	mA
		M5M4V181600A-7				145	
		M5M4V181600A-8				135	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while RAS=V_{IL} and LCAS/UCAS=V_{IH} .

CAPACITANCE (Ta=0～70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M4V181600AJ, TP, RT	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
$C_{I/O}$	Input/Output capacitance, data ports					7	pF

SWITCHING CHARACTERISTICS (Ta=0～ 70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits						Unit
			M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note7,8)		15		20		20	ns
tRAC	Access time from $\overline{RAS}$	(Note7,9)		60		70		80	ns
tAA	Columu address access time	(Note 7,10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12)	0	15	0	20	0	20	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)	0	15	0	20	0	20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
7: Measured with a load circuit equivalent to 2TTL loads and 100pF.
8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.
10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.
11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.
12: $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10$ μA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0～ 70°C, Vcc=3.3V ±0.3V, Vss=0V, unless otherwise noted, see notes 12,13)

Symbol	Parameter		Limits						Unit
			M5M4V181600A-6		M5M4V181600A-7		M5M4V181500A-8		
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time								ms
tRP	$\overline{RAS}$ high pulse width		40		50		60		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note15)	20	45	20	50	20	60	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note16)	15	30	15	35	15	40	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note17)	0	10	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note19)	15		20		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note19)	15		20		20		ns
tT	Transition time	(Note20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT =5ns.
14: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.
15: $t_{RCD(max)}$ is specified as a reference point only. If tRCD is less than $t_{RCD(max)}$, access time is tRAC. If tRCD is greater than $t_{RCD(max)}$, access time is controlled exclusively by tCAC or tAA. $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_{H} + t_{ASC(min)}$.
16: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by tAA.
17: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	120		140		160		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		25		ns
t_{RCS}	Read Setup time after $\overline{CAS}$ high	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ low (Note 21)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ low (Note 21)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		25		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		25		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	120		140		160		ns
t_{RAS}	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	15	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	10		15		20		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		25		ns
t_{WP}	Write pulse width	10		15		20		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		15		20		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
		Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time (Note22)	160		185		210		ns
t_{RAS}	$\overline{RAS}$ low pulse width	95	10000	115	10000	135	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	50	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	95		115		135		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	50		65		80		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note23)	30		40		50		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note23)	75		90		105		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note23)	45		55		65		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low	15		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low	15		20		25		ns
t_{WP}	Write pulse width	10		15		20		ns
t_{DS}	Data setup time before $\overline{W}$ low	0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low	10		15		20		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low	15		15		15		ns

Note 22: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
		Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	75		95		115		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note25)	100	100000	115	100000	130	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note26)	10	15	10	15	10	15	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note23)	35		40		45		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

26: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M4V181600A-6		M5M4V181600A-7		M5M4V181600A-8		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		20		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		20		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

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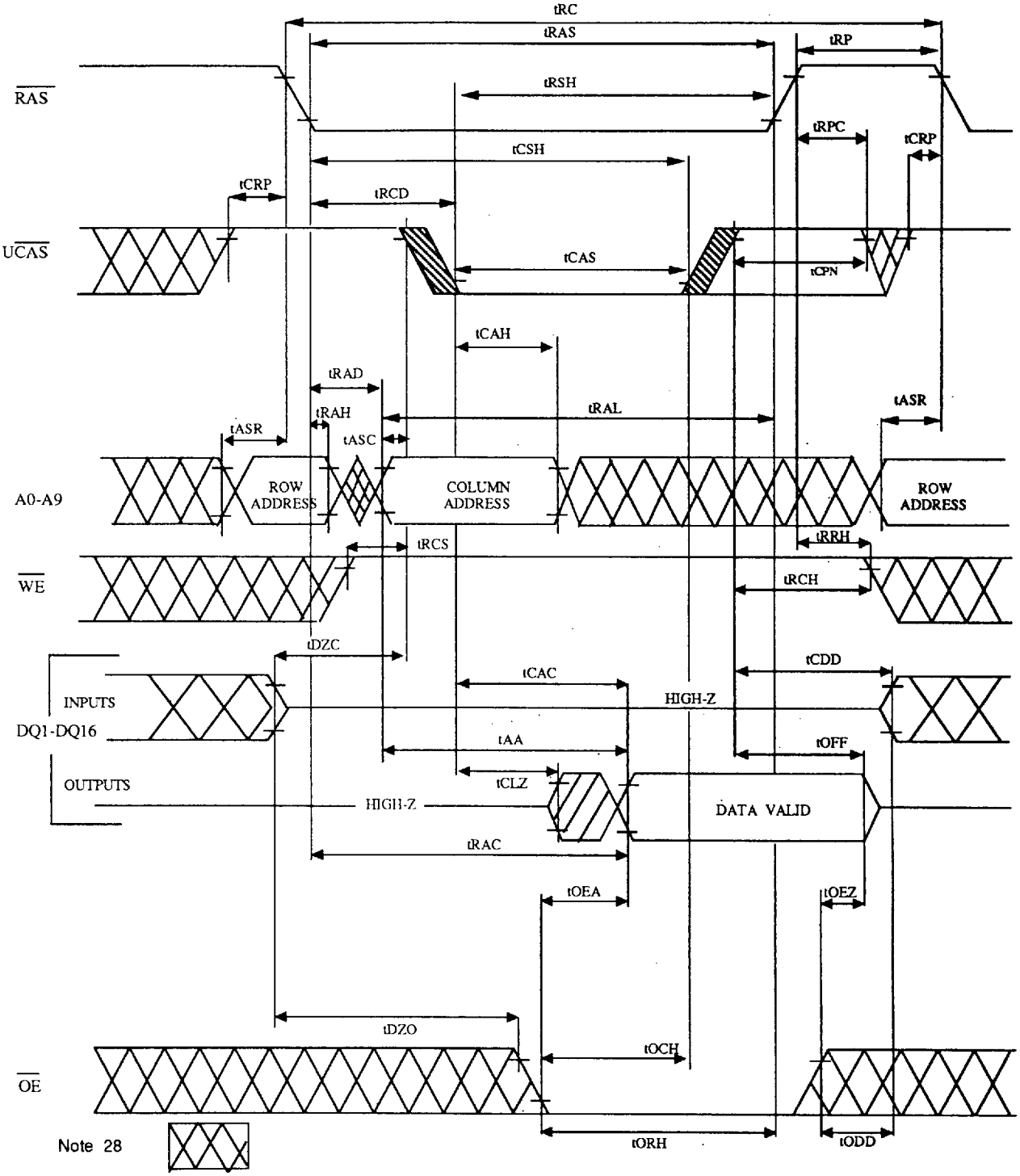
Timing Diagrams (Note 28)
Read Cycle



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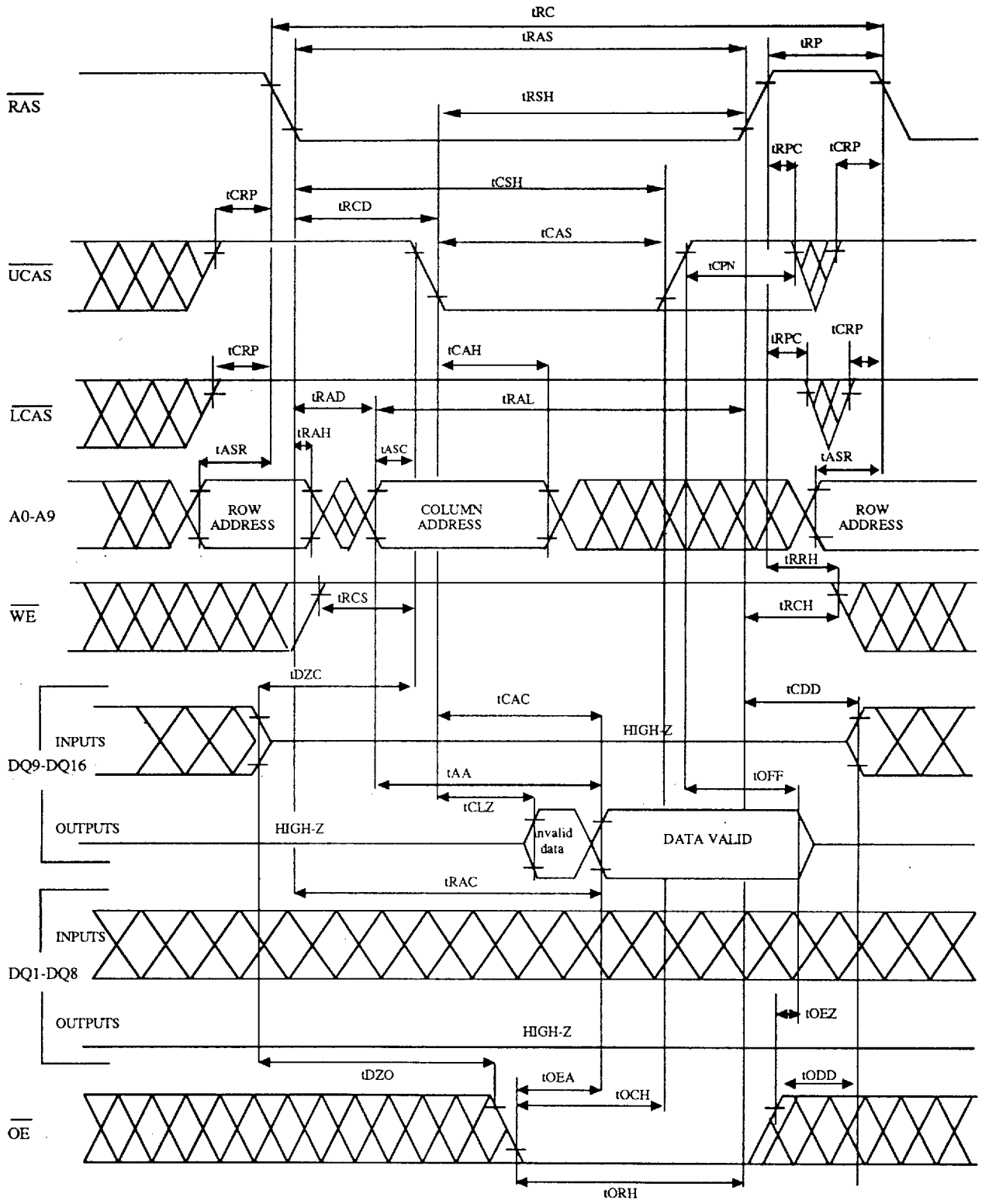
FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Byte Read Cycle



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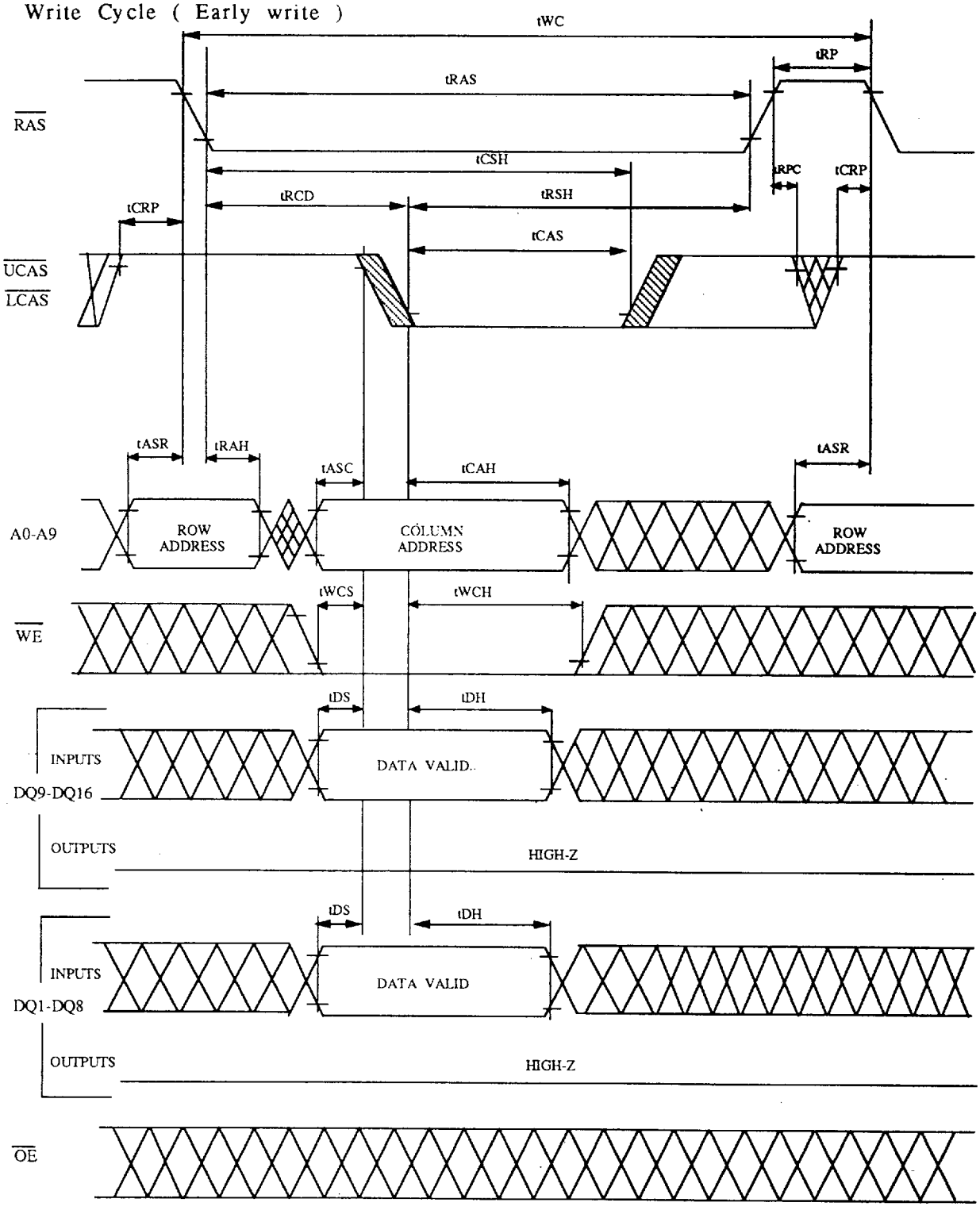
Write Cycle (Early write)



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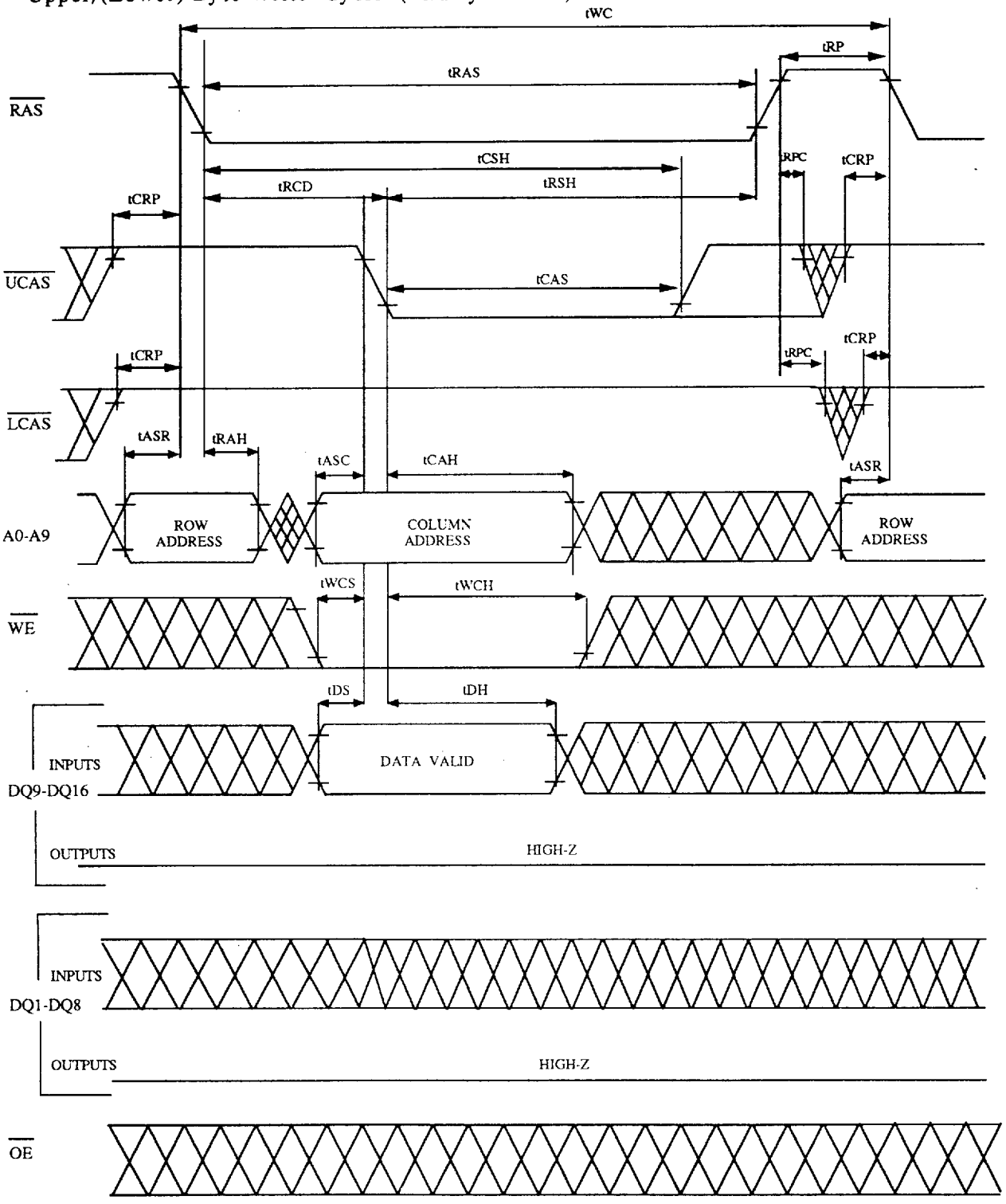
FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Byte Write Cycle (Early write)



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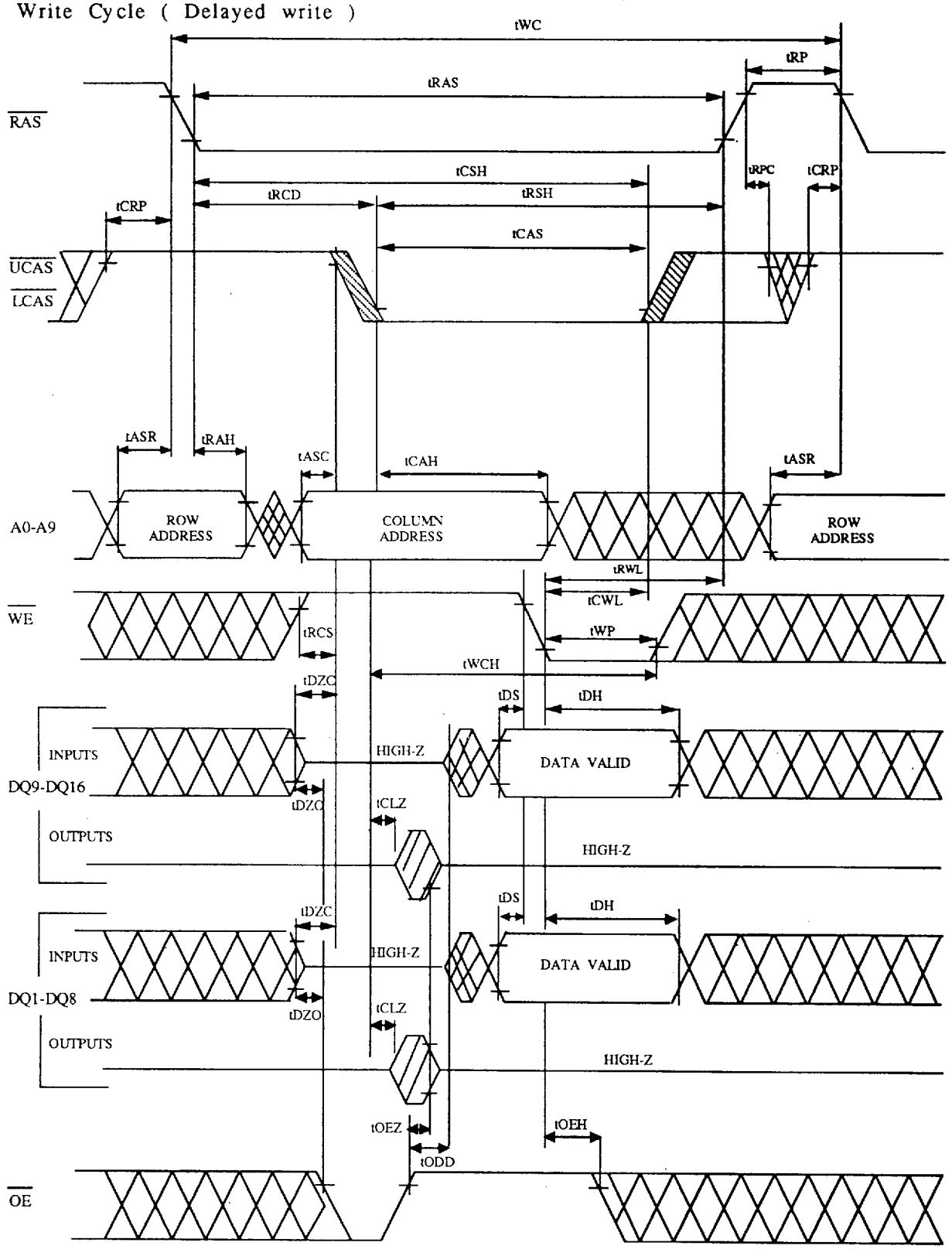
FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

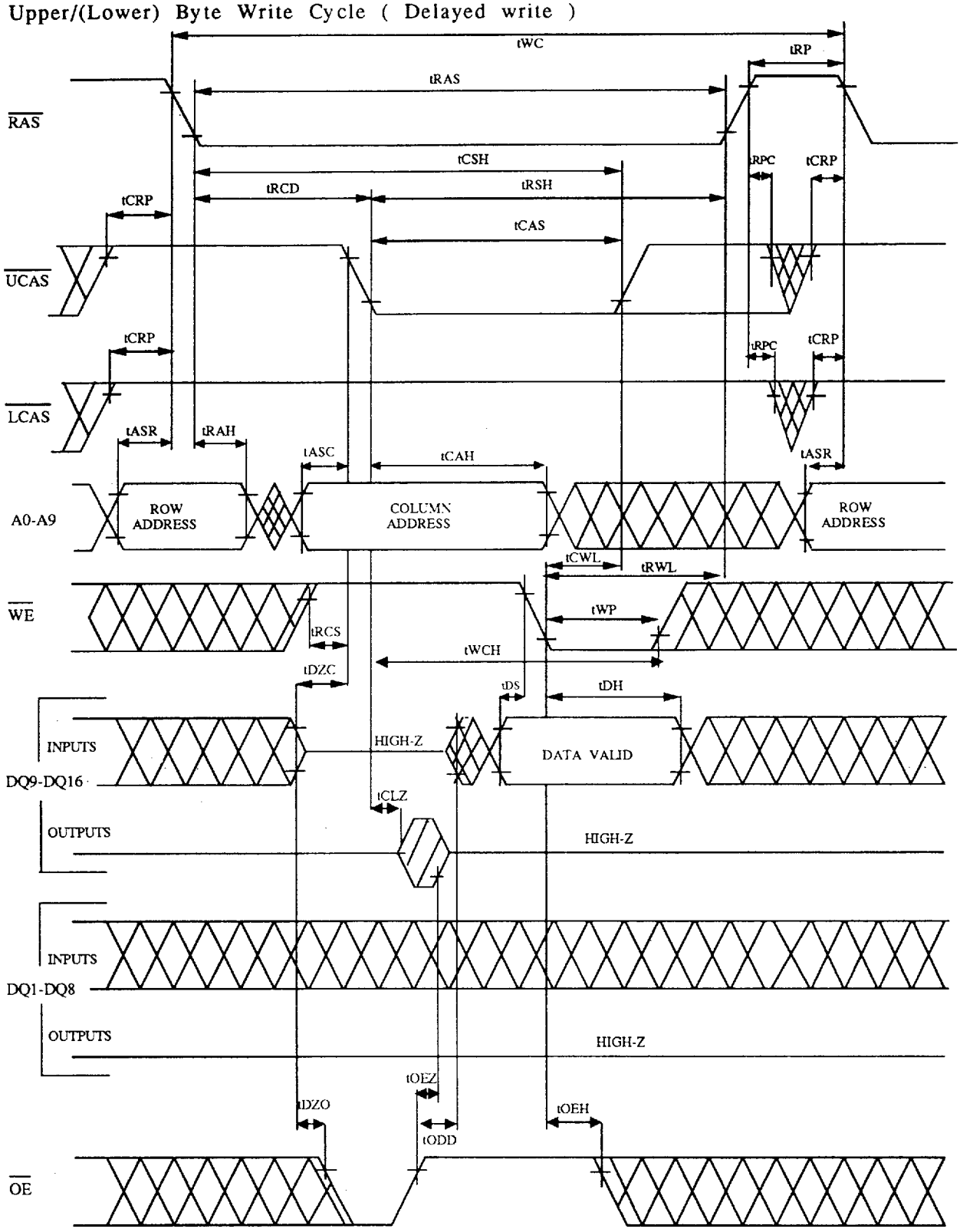
Write Cycle (Delayed write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

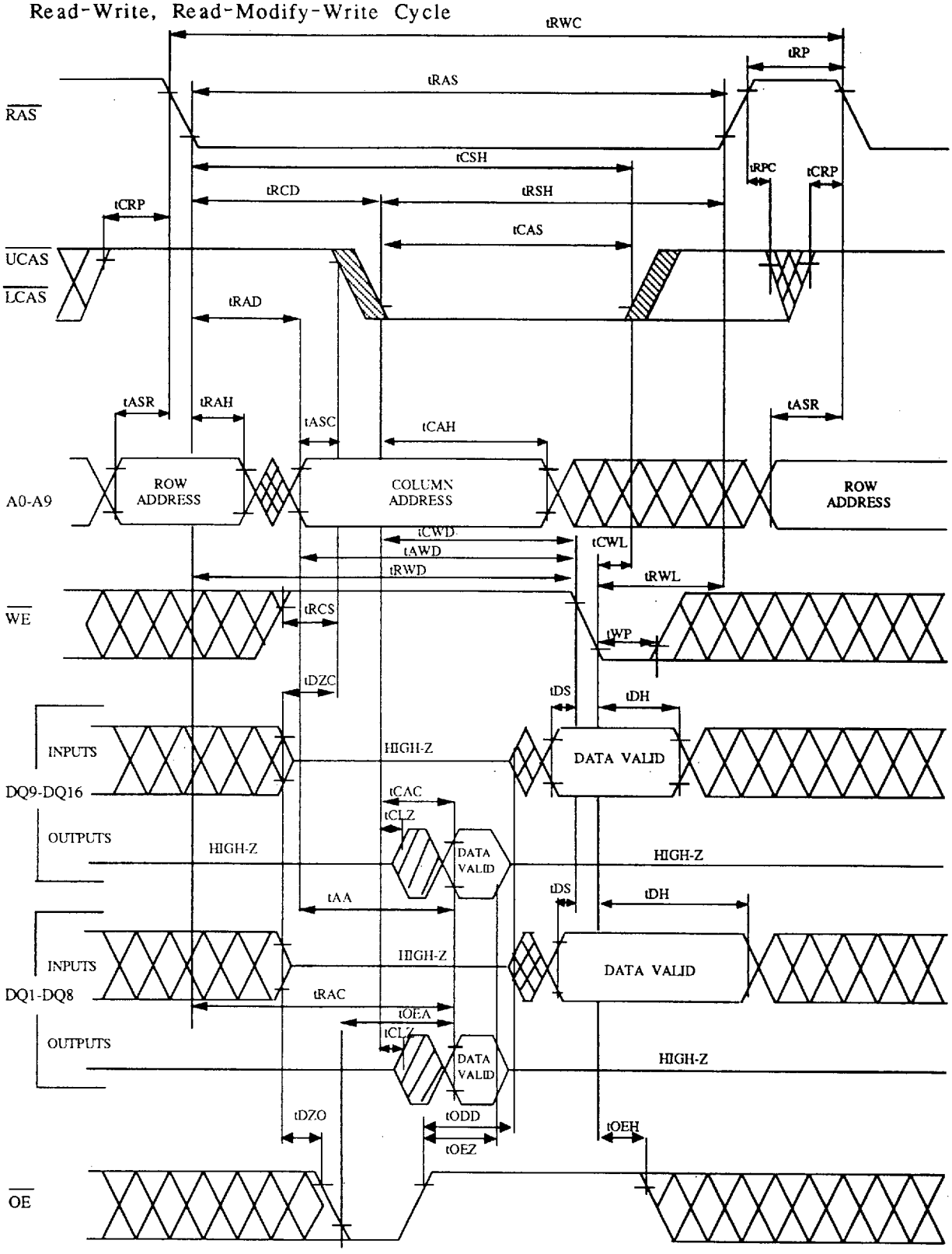
Upper/(Lower) Byte Write Cycle (Delayed write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

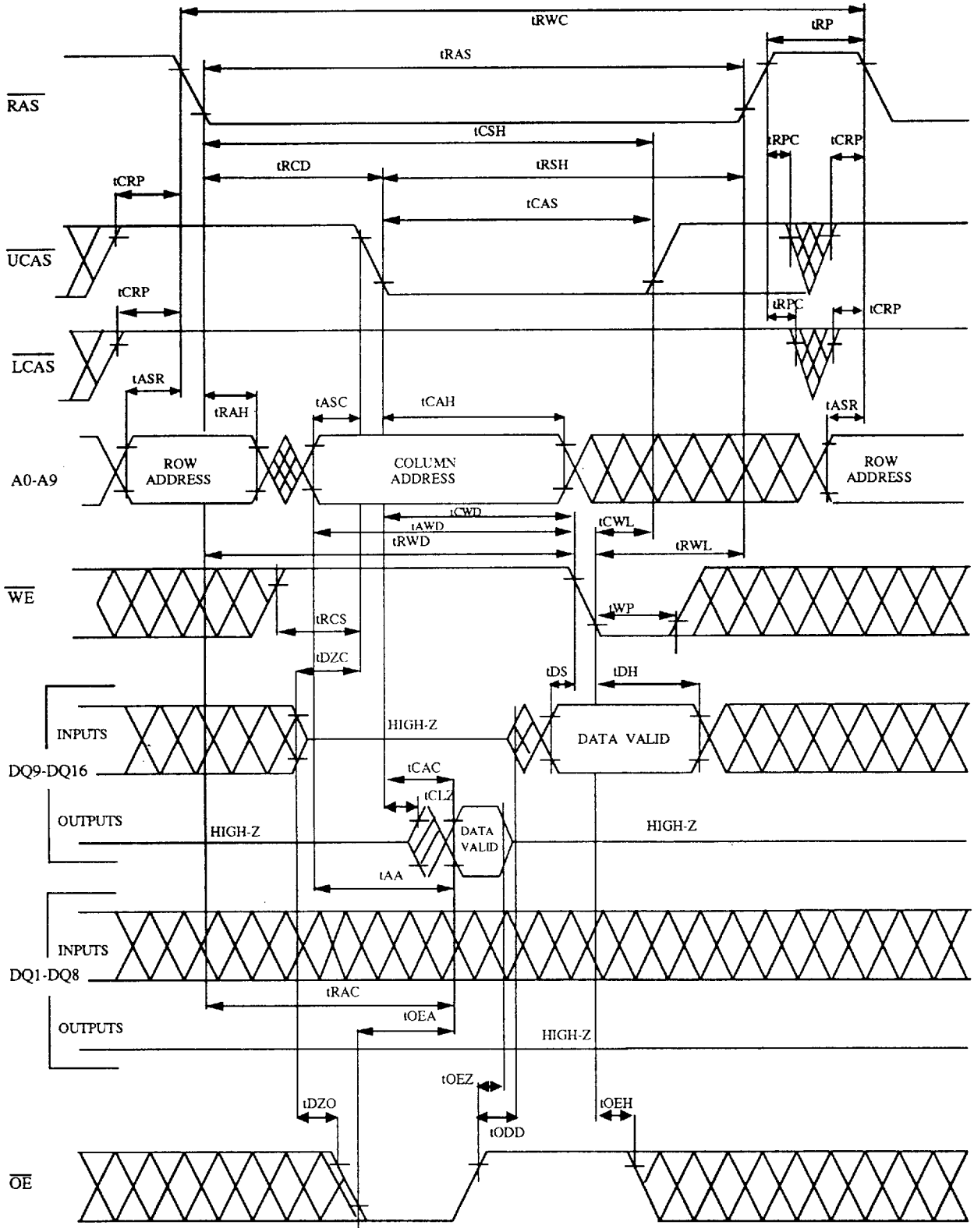
Read-Write, Read-Modify-Write Cycle



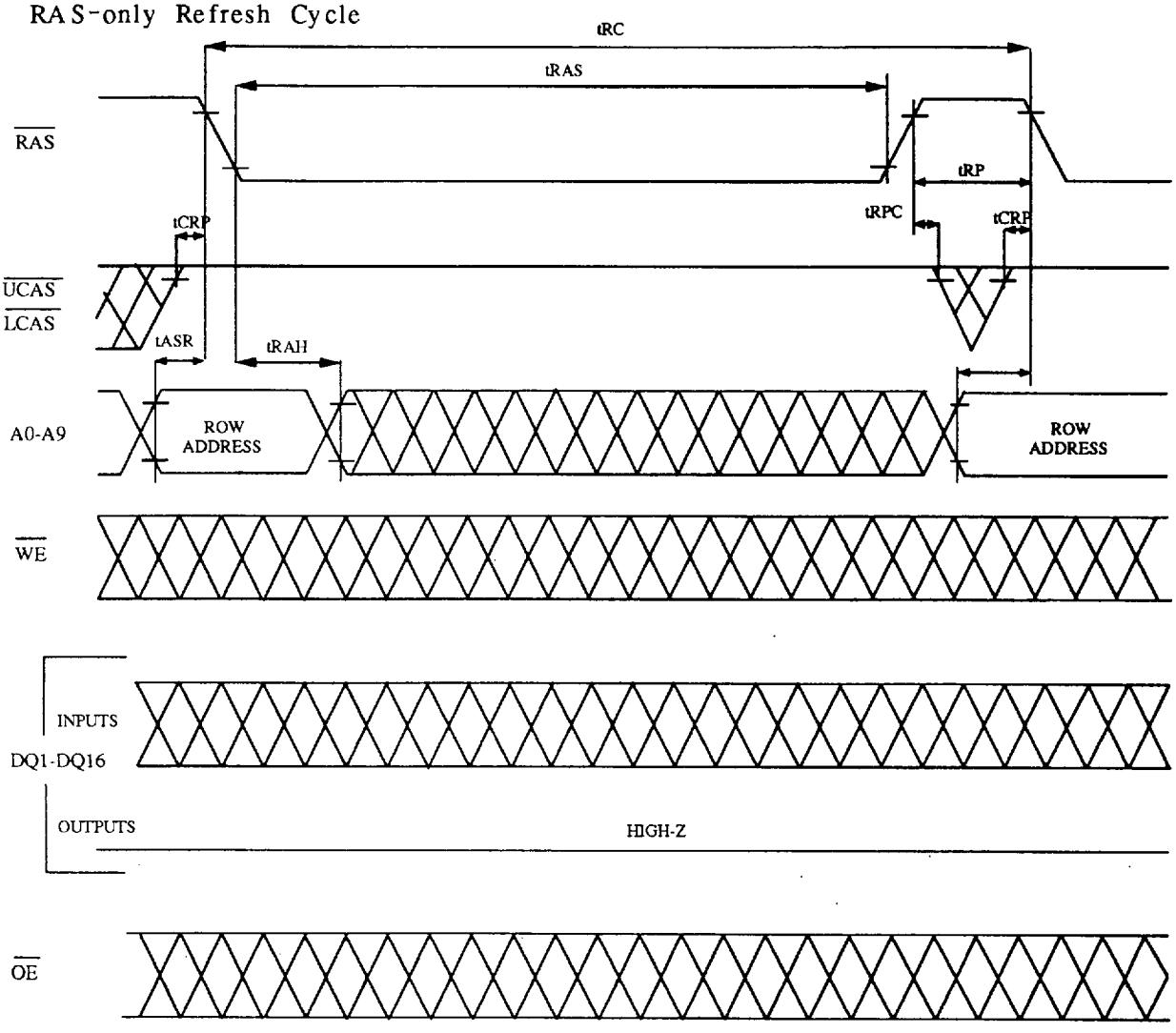
M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



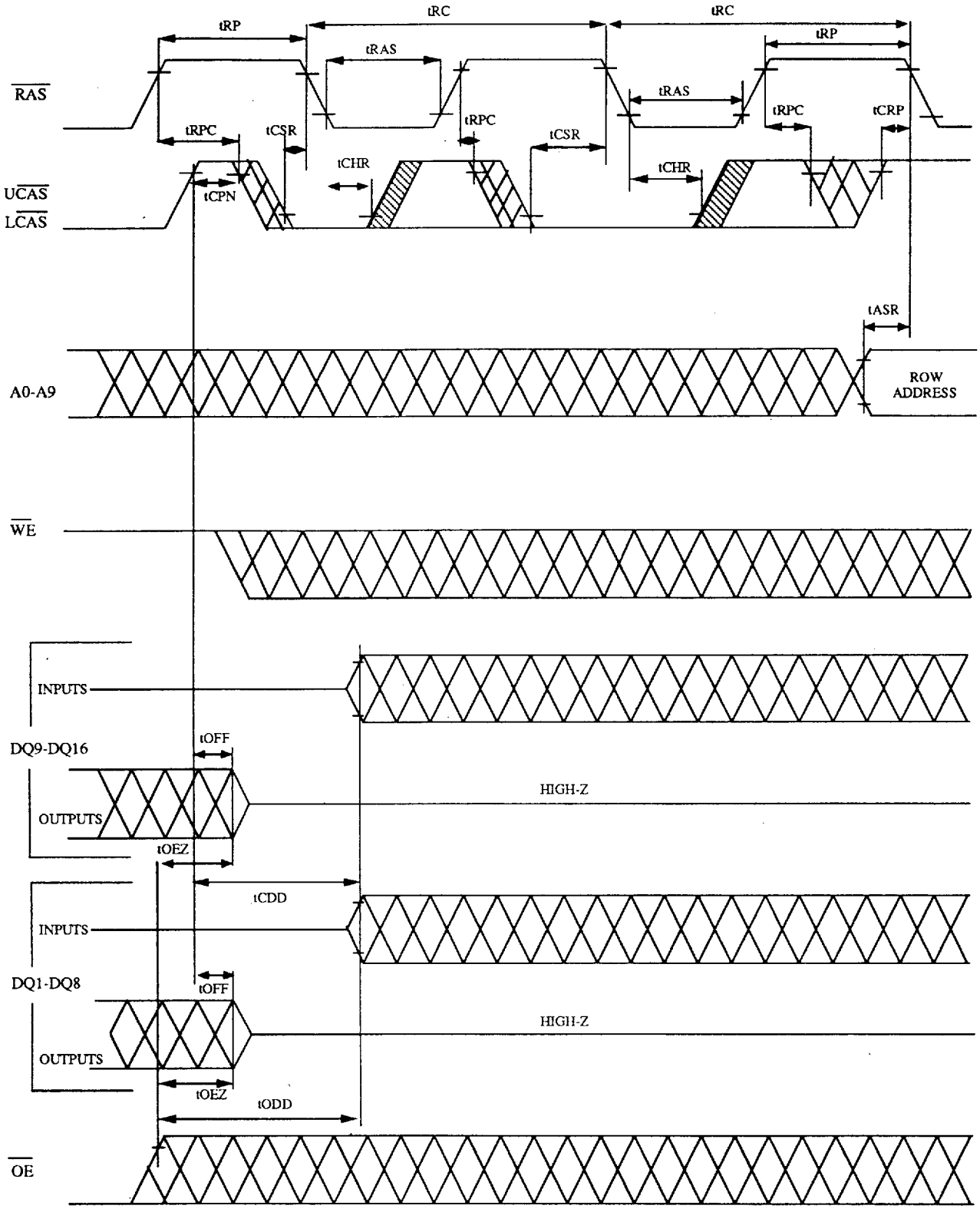
$\overline{\text{RAS}}$-only Refresh Cycle



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

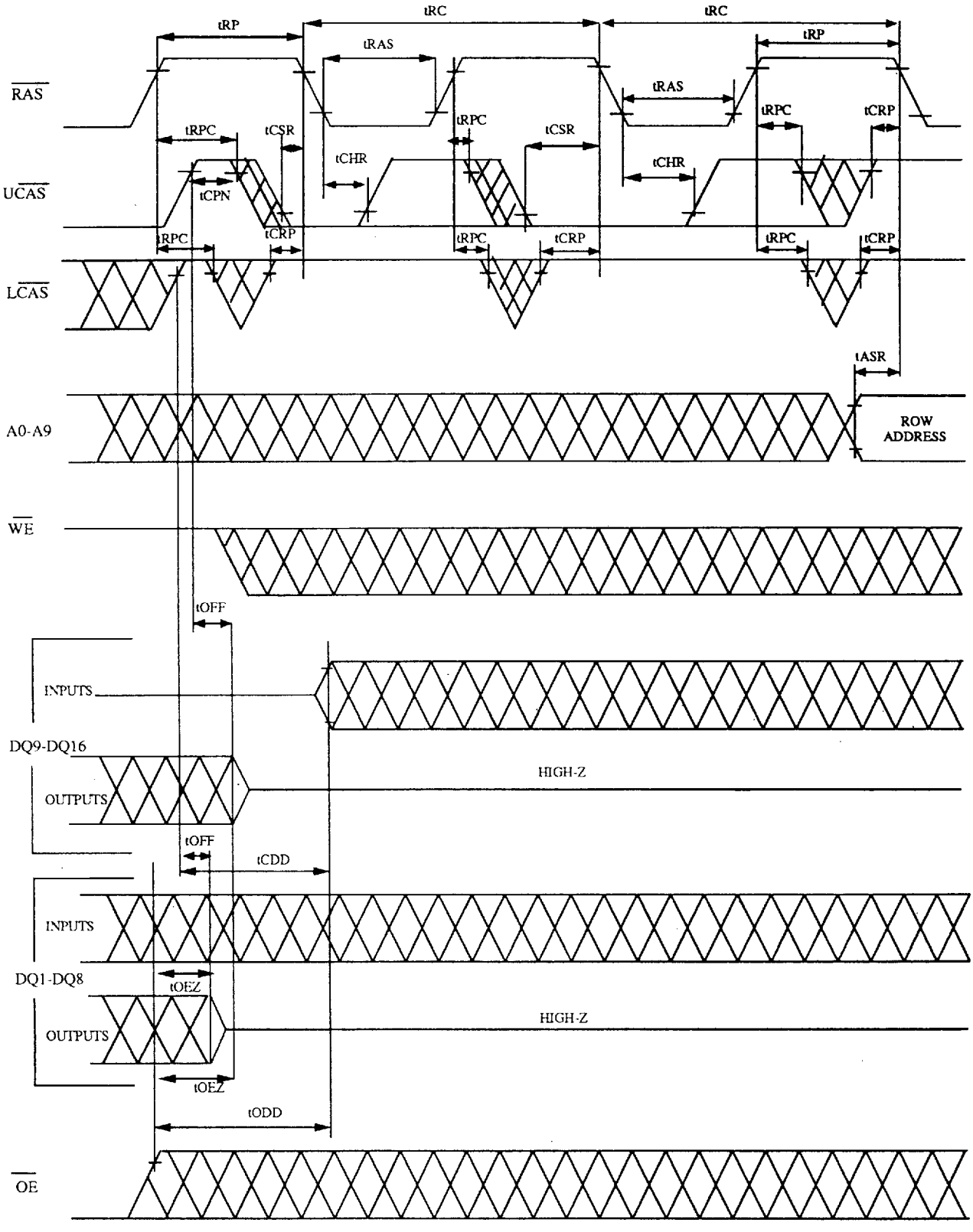
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle , Extended Refresh Cycle *



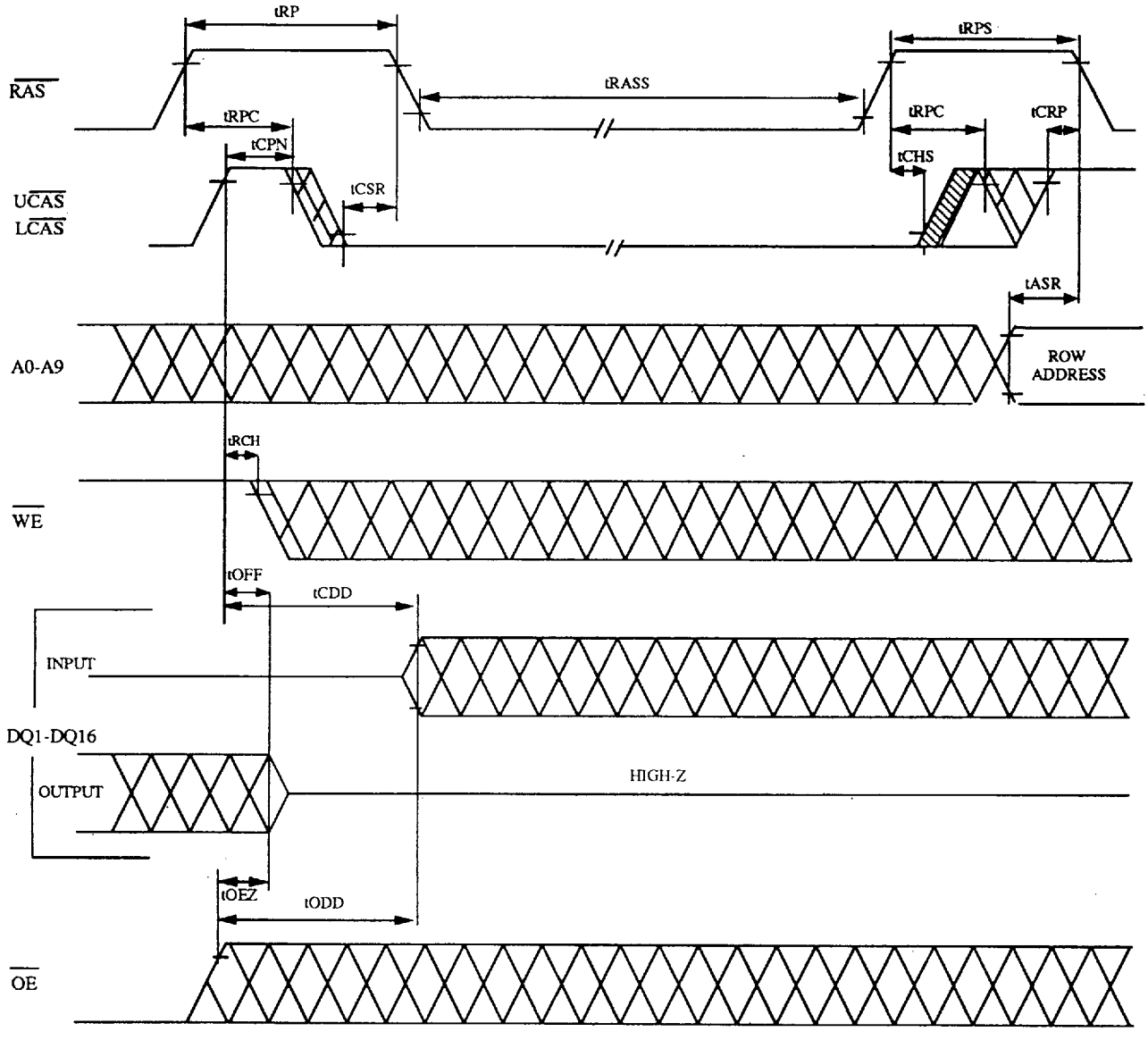
M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

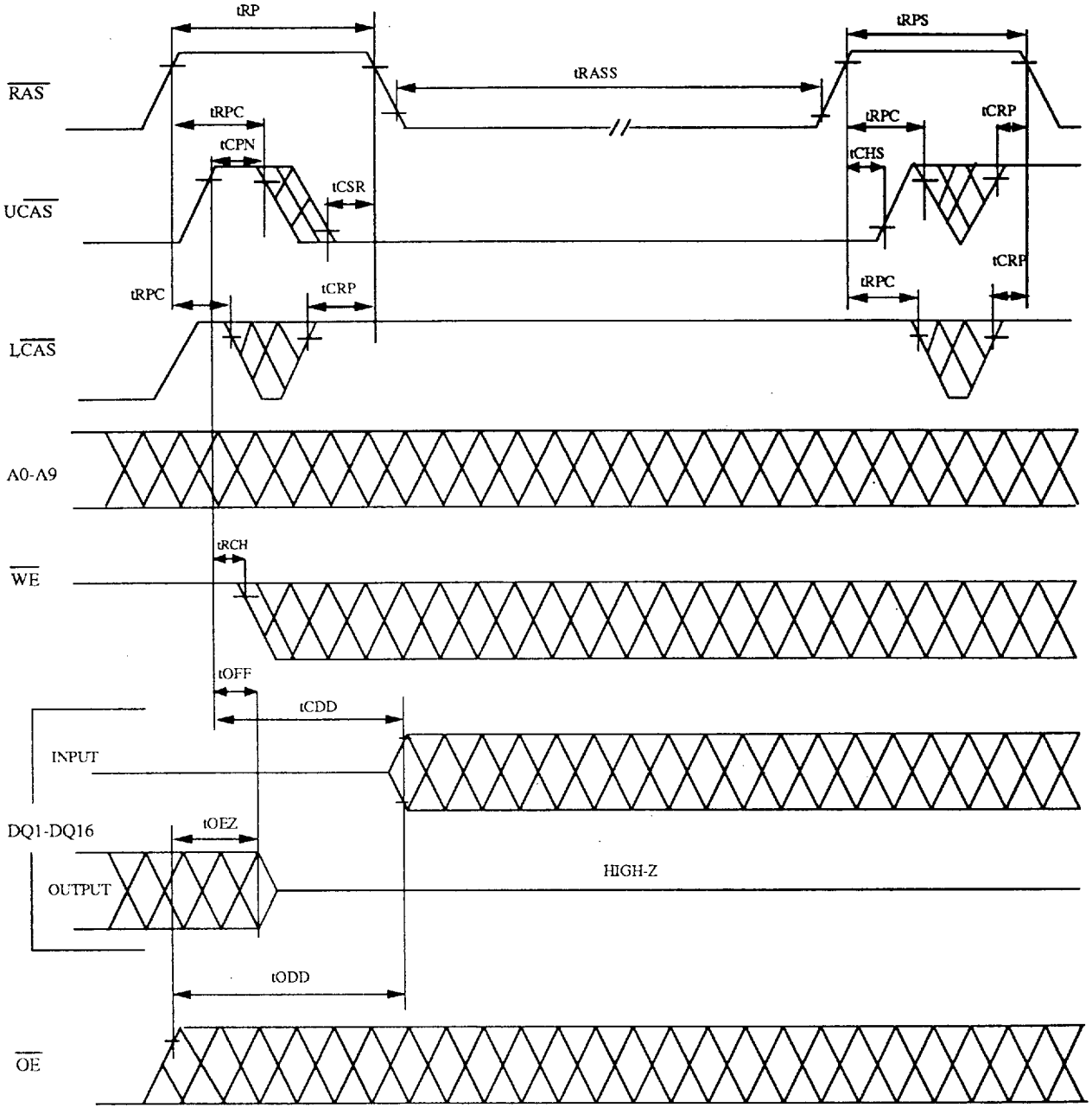
Upper/(Lower) $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle ,Extended Refresh Cycle



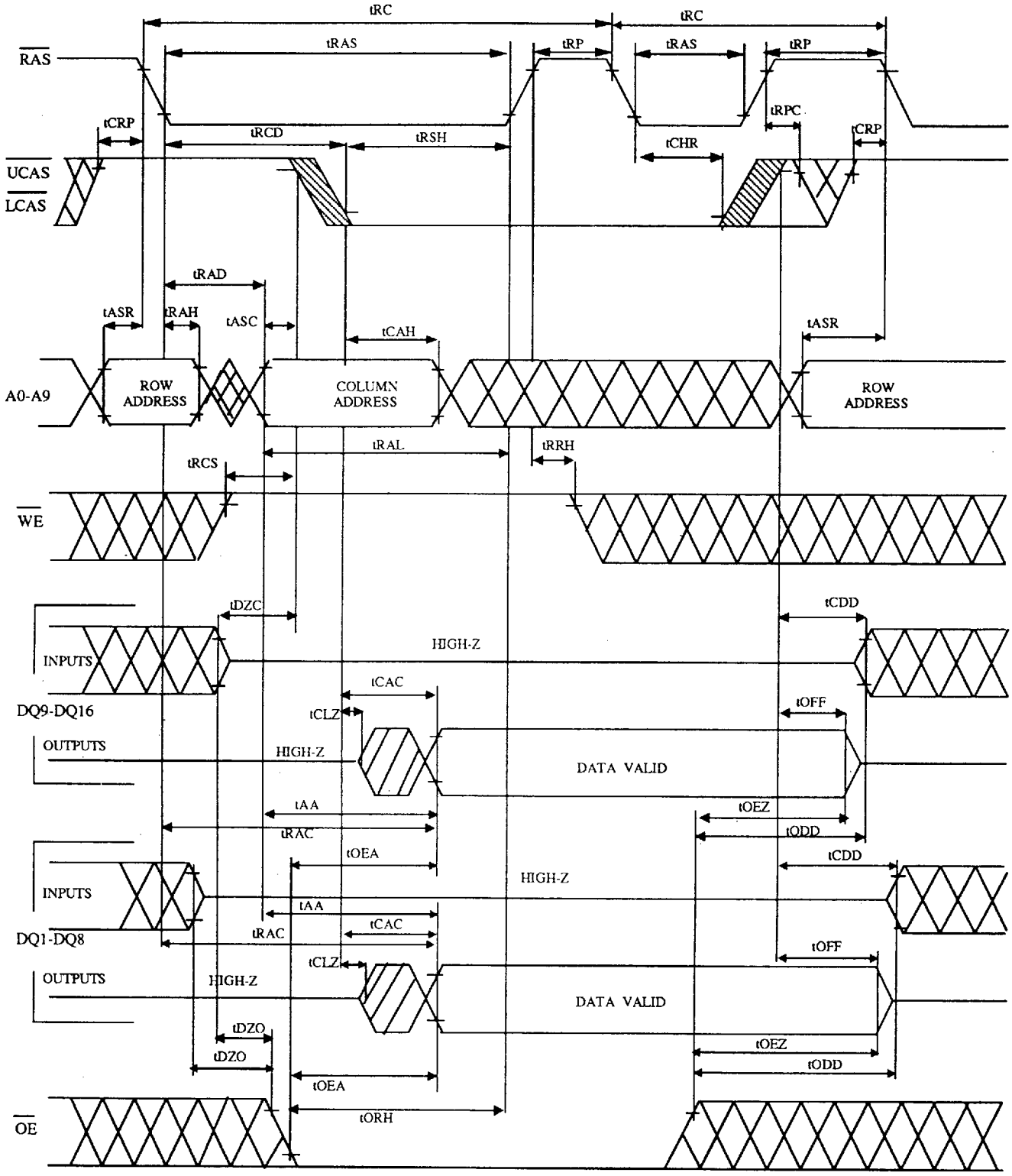
Self Refresh Cycle (Note 28)



Upper / (Lower) Self Refresh Cycle* (Note 28)

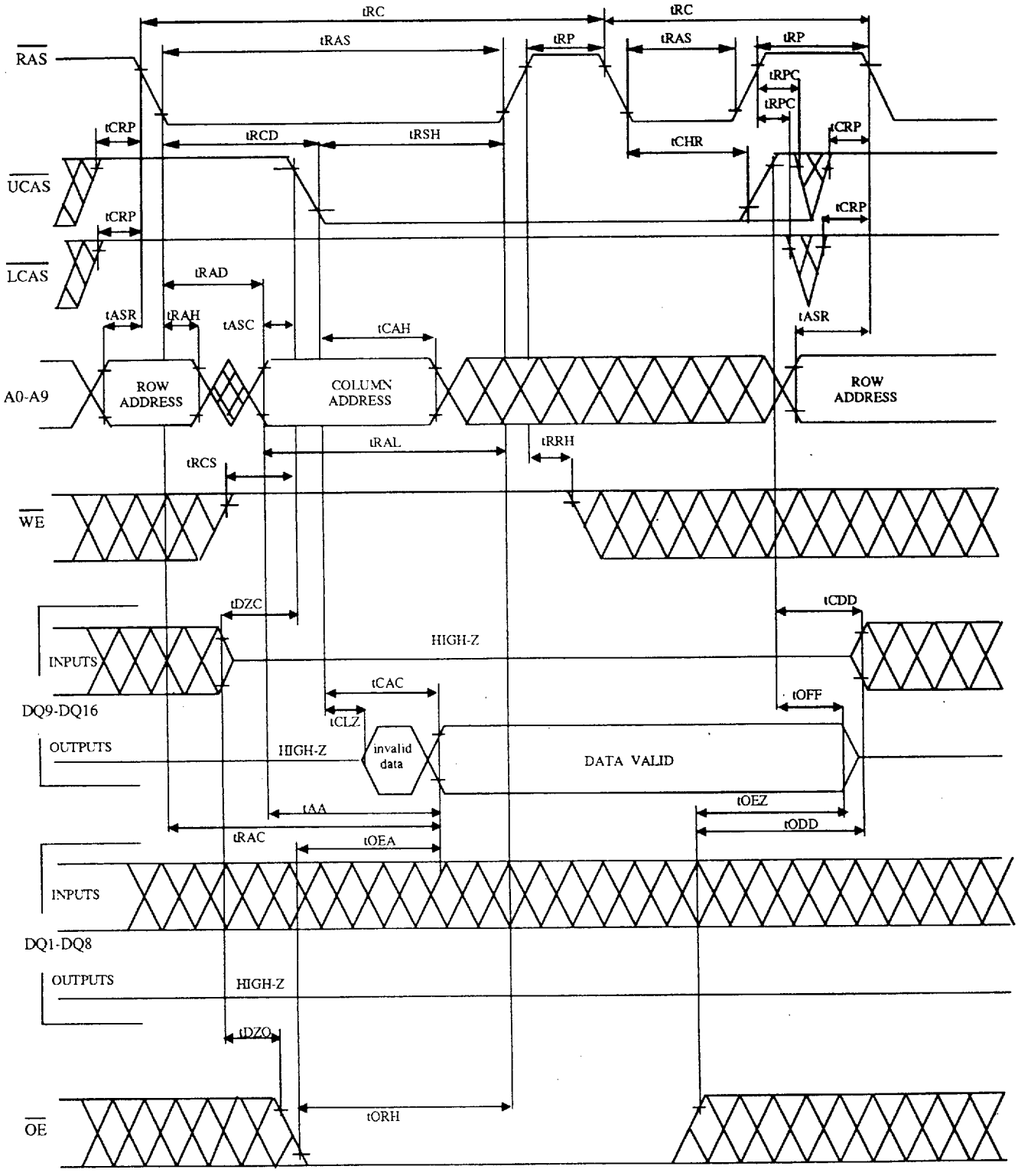


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

Upper/(Lower) Hidden Refresh Cycle (Byte Read) (Note 30)

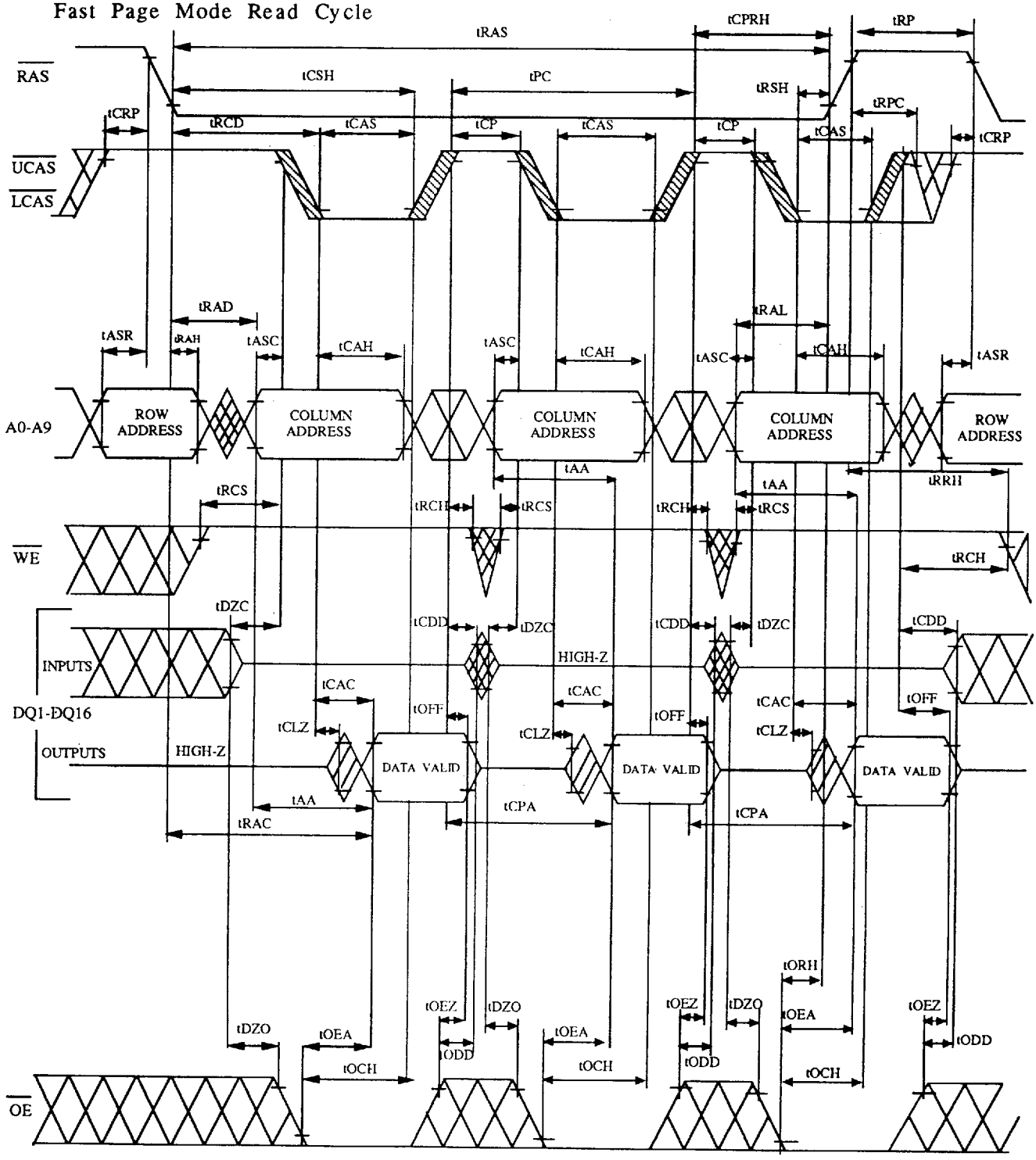


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

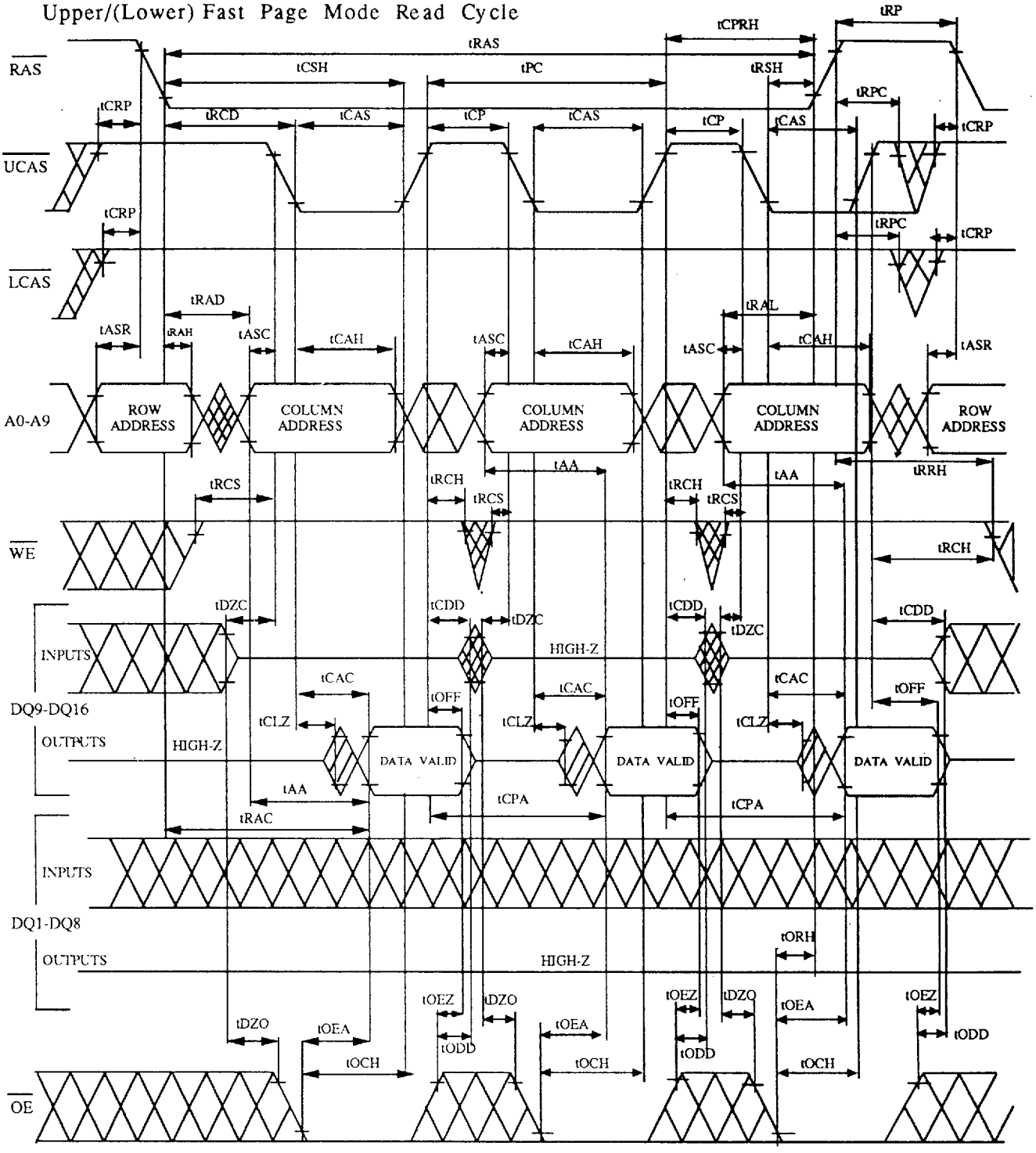
Fast Page Mode Read Cycle



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

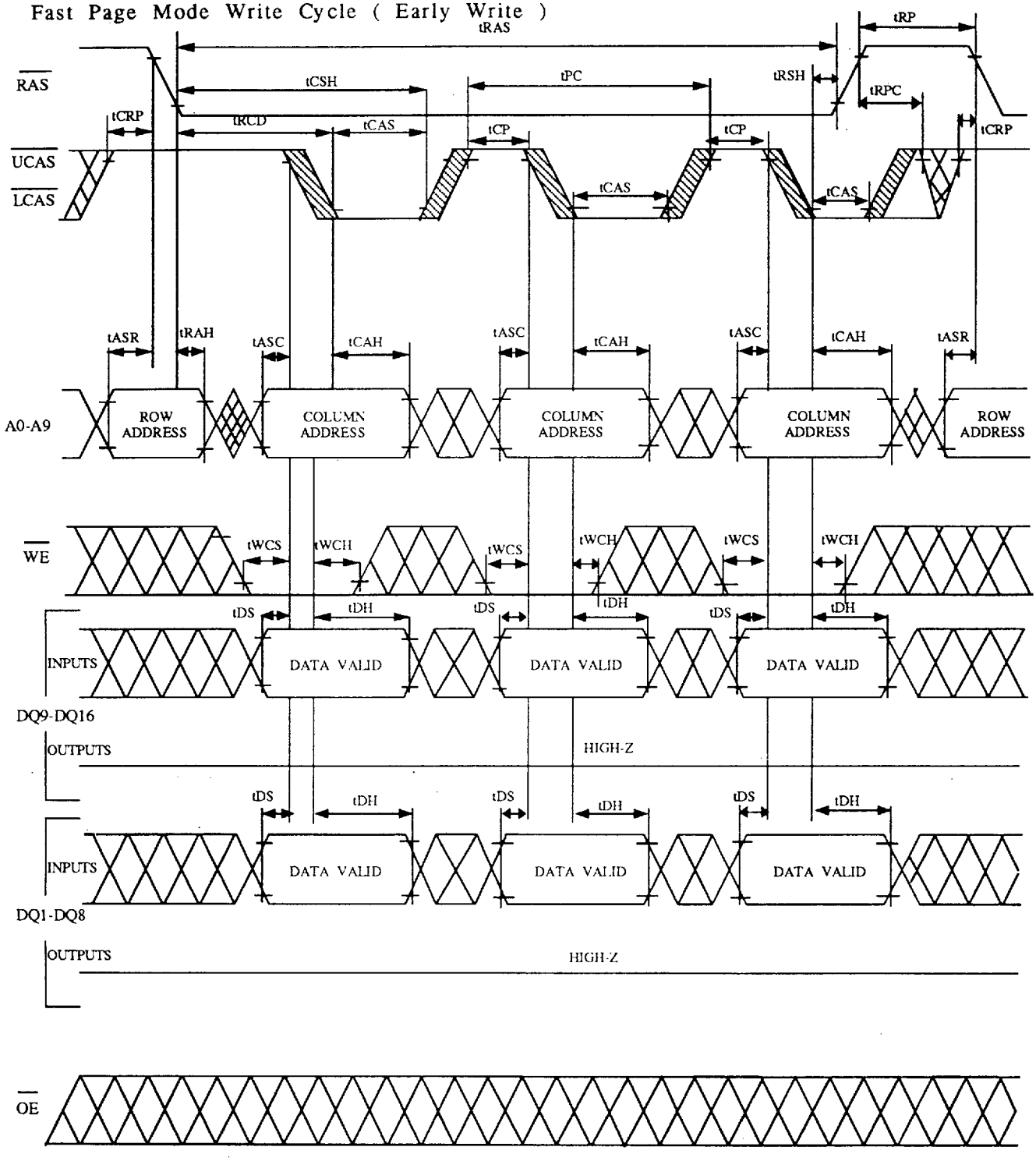
Upper/(Lower) Fast Page Mode Read Cycle



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

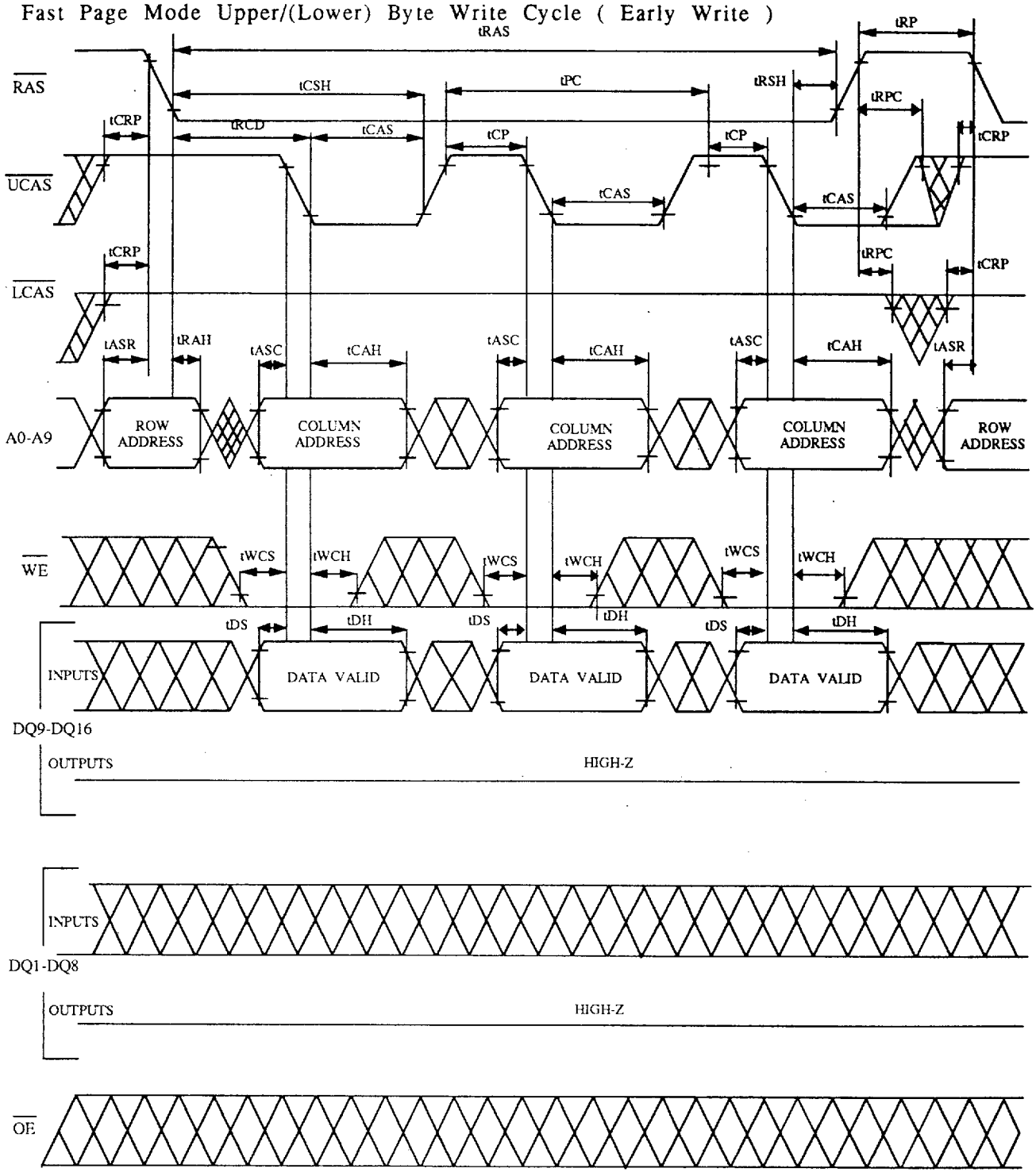
Fast Page Mode Write Cycle (Early Write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

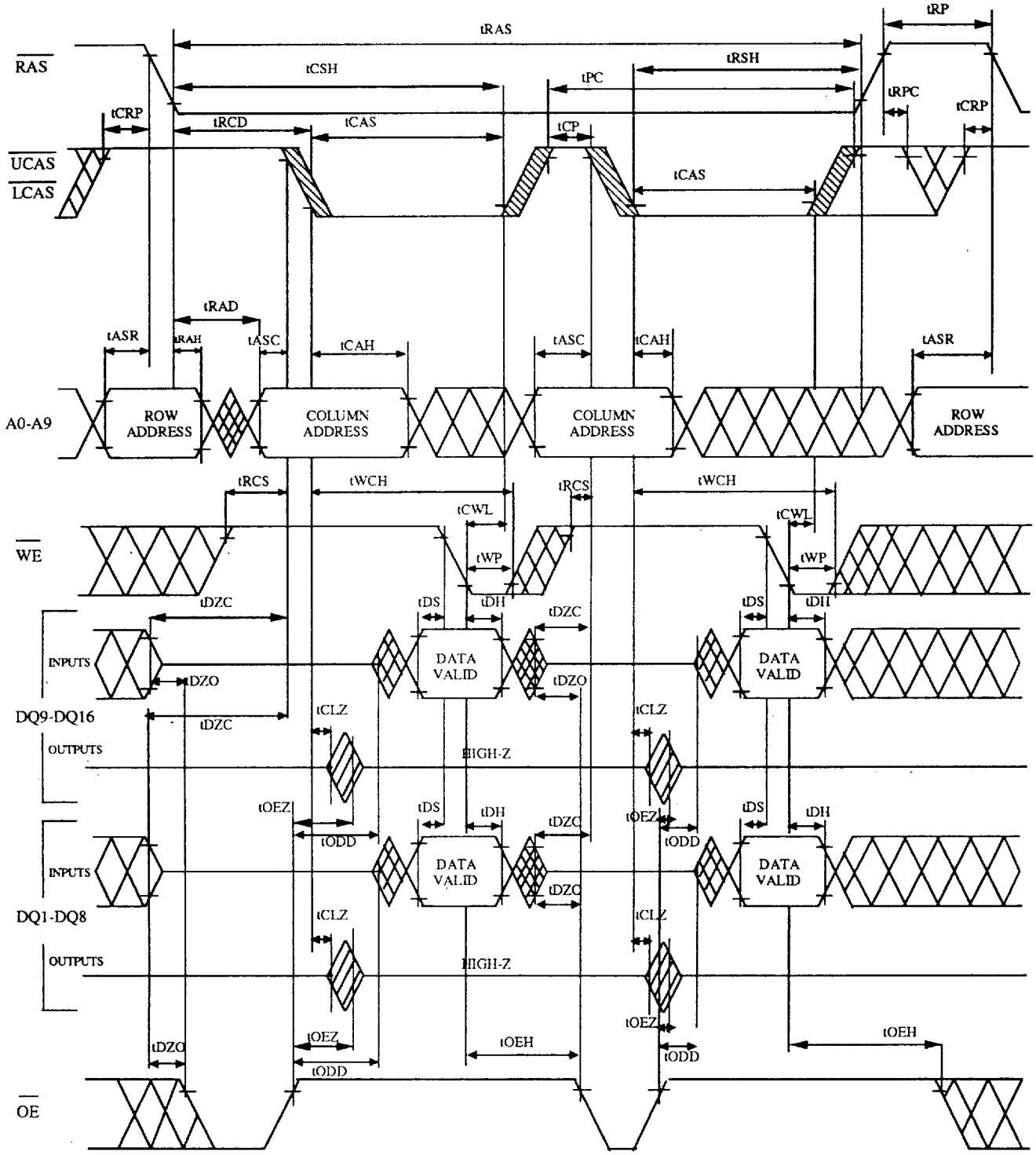
Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

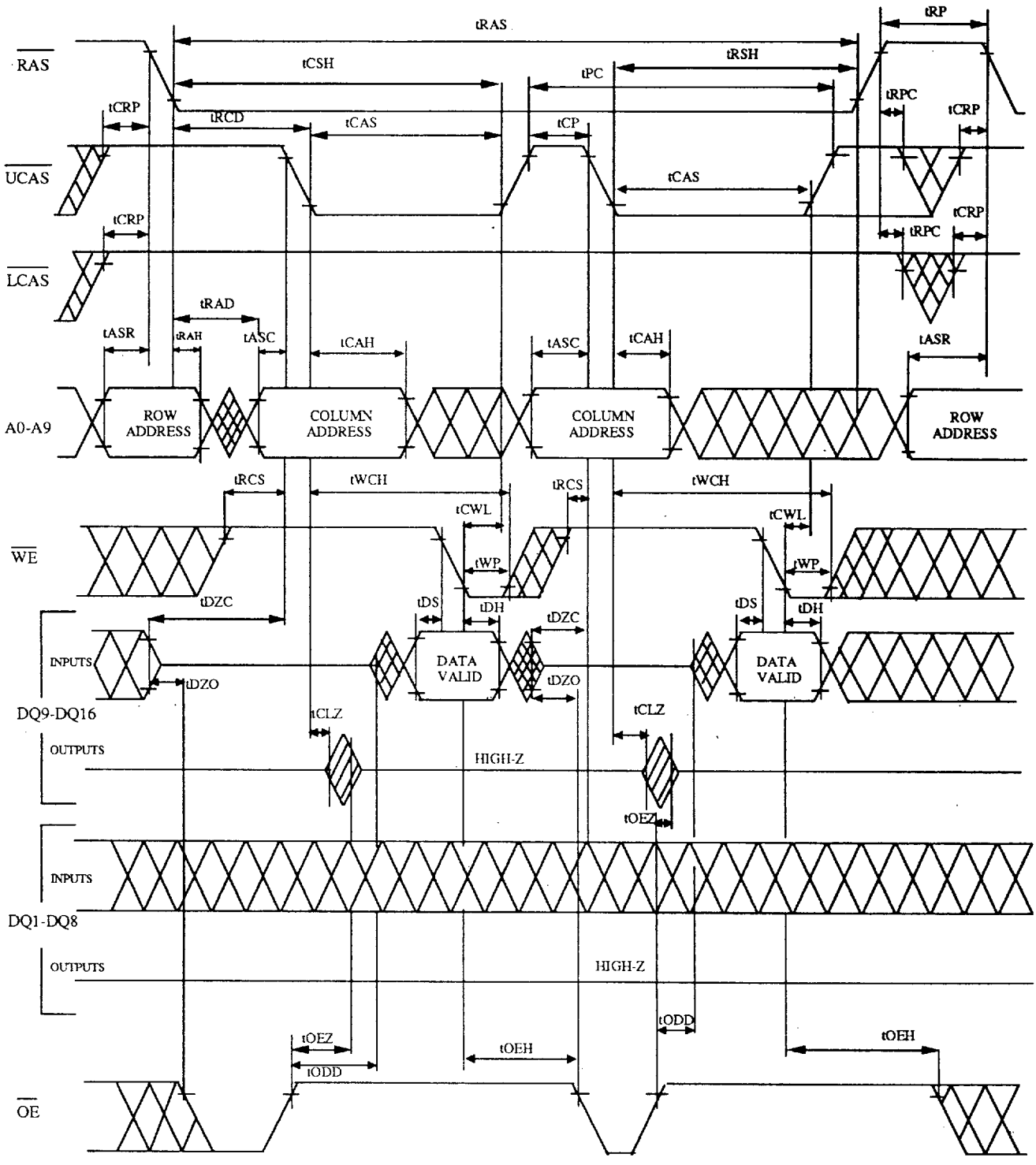
Fast Page Mode Write Cycle (Delayed Write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

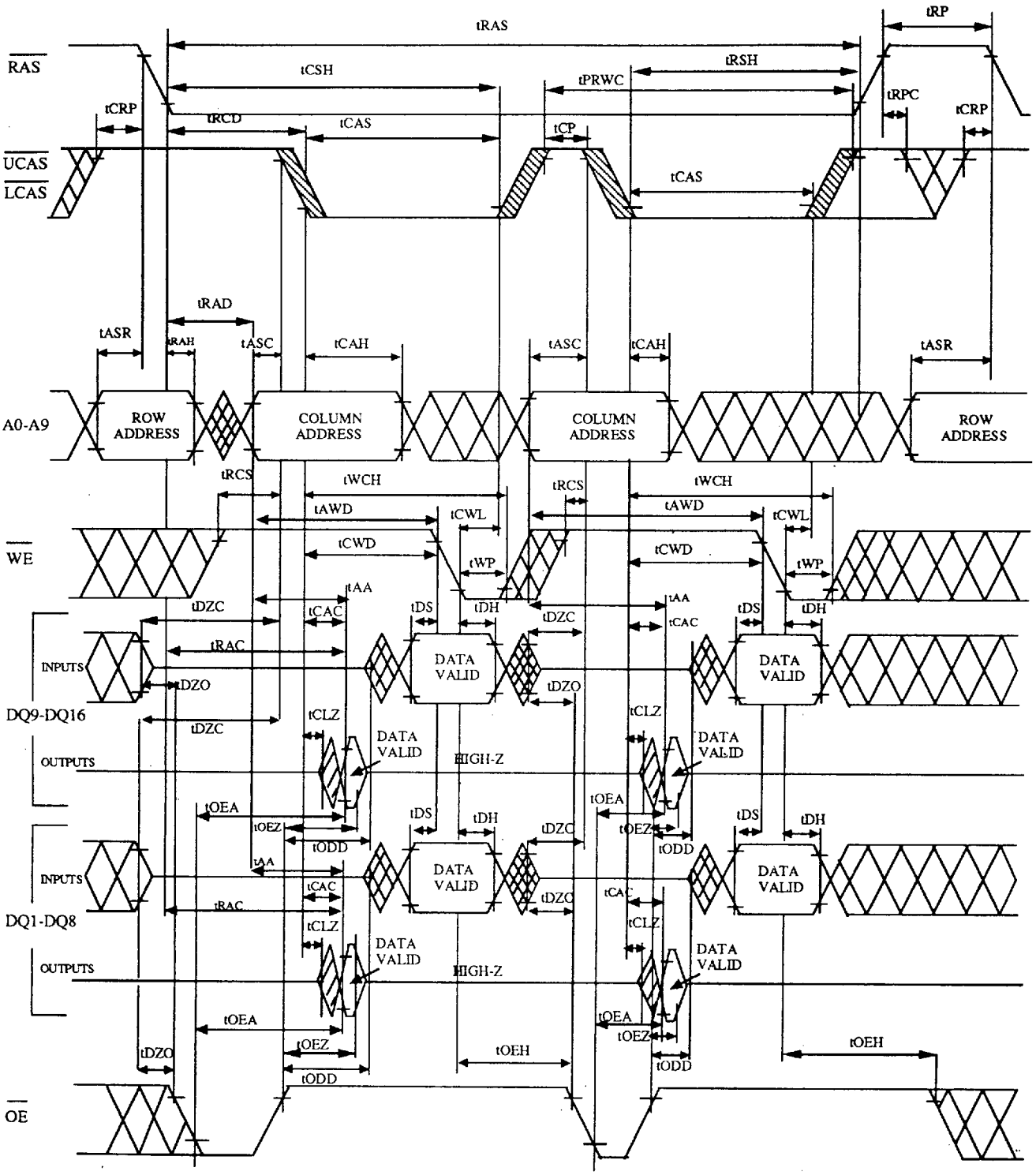
Fast Page Mode Upper/(Lower) Byte Write (Delayed Write)



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M4V181600AJ,TP,RT-5,-6,-7

FAST PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle