SPEED/PACKAGE AVAILABILITY

54LS	F,W	74LS	B
54S	F,W	74S	B

DESCRIPTION

This Schottky-clamped high-performance multiplexer features three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

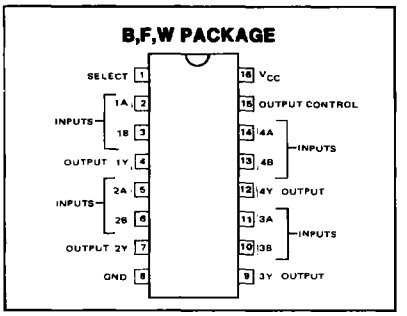
This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

FUNCTION TABLE

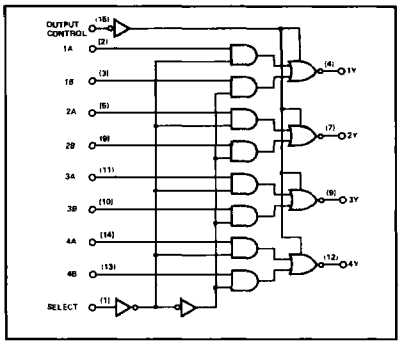
INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

PIN CONFIGURATION



BLOCK DIAGRAM



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74LS C_L=15pF			54/74S C_L=15pF R_L=280Ω			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	Data	Any		12	18		4	6	ns
t_{PHL} High-to-low				12	18		4	6	
t_{PLH} Low-to-high	Select	Any		14	21		8	12	
t_{PHL} High-to-low				14	21		7.5	12	
Output enable time									
t_{ZH} To high level	Output control	Any		20	30		13	19.5	
t_{ZL} To low level				20	30		14	21	
Output disable time			C_L=5pF			C_L=5pF			
t_{HZ} From high level	Output	Any		14	30		5.5	8.5	
t_{LZ} From low level	control			14	25		9	14	

Load circuit and waveforms shown at front of section (totem pole outputs).