MOTOROLA

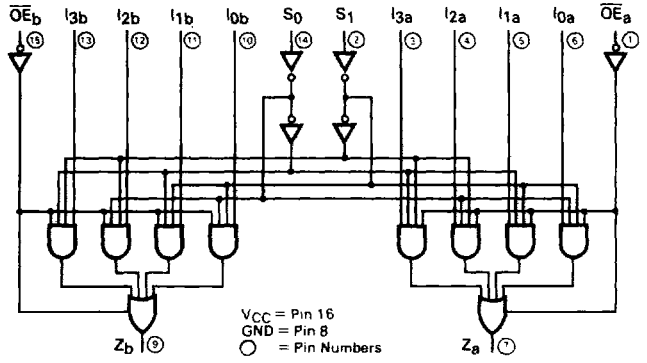
MC54F/74F253

DUAL 4-INPUT MULTIPLEXER
(with 3-State Outputs)

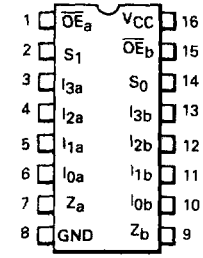
DESCRIPTION — The MC54F/74F253 is a Dual 4-Input Multiplexer with 3-State Outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable $\overline{OE}$ inputs, allowing the outputs to interface directly with bus oriented systems.

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS
FAST™ SCHOTTKY TTL

LOGIC DIAGRAM



CONNECTION DIAGRAM DIP
(TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)
D Suffix — Case 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74	—	—	-3.0	mA
I_{OL}	Output Current — Low	54, 74	—	—	24	mA

FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-Input Multiplexers with 3-State Outputs. They select two bits from four sources selected by common Select Inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Level
L = LOW Level
X = Immaterial
(Z) = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

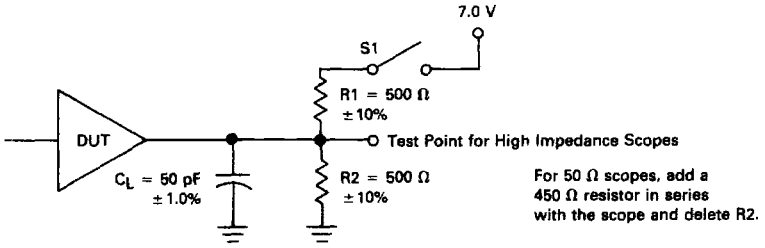
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				-1.2	V	I_{IN} = 18 mA	V_{CC} = MIN
V_{OH}	Output HIGH Voltage	54, 74	2.4			V	I_{OH} = −3.0 mA	V_{CC} = 4.50 V
		74	2.7			V	I_{OH} = −3.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 24 mA	V_{CC} = MIN
I_{OZH}	Output Off Current—HIGH				50	μA	V_{OUT} = 2.7 V	V_{CC} = MAX
I_{OZL}	Output Off Current—LOW				-50	μA	V_{OUT} = 0.5 V	V_{CC} = MAX
I_{IH}	Input HIGH Current				20	μA	V_{IN} = 2.7 V	V_{CC} = MAX
					0.1	μA	V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.6	mA	V_{IN} = 0.5 V	V_{CC} = MAX
I_{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V_{OUT} = 0 V	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH				16	mA	OE_n = GND I_O = 4.5 V; S_n, I_1 - I_3 = GND	
	Total, Output LOW				23		I_n, S_n, OE_n = GND V_{CC} = MAX	
	Total at HIGH-Z				23		OE_n = 4.5 V, V_{CC} = MAX I_n, S_n = GND	

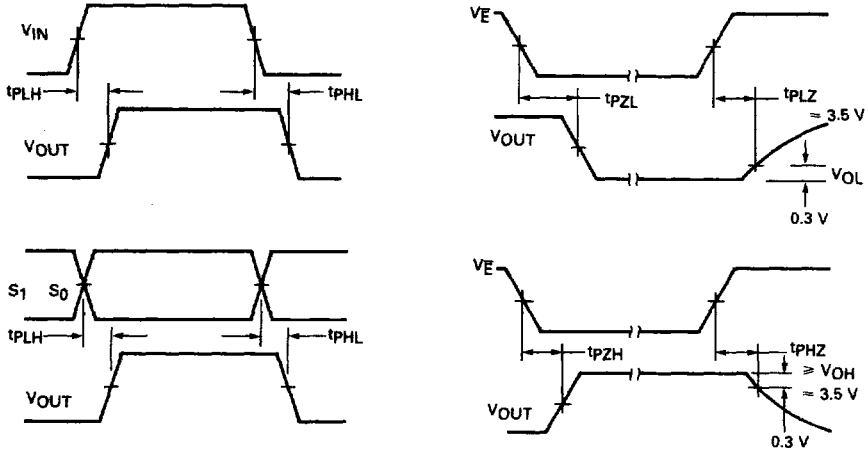
AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF		54F T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% C_L = 50 pF		74F T_A = 0°C to +70°C V_{CC} = 5.0 V ±10% C_L = 50 pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.5 3.0	11.5 9.0	3.5 2.5	15 11	4.5 3.0	13.5 10	ns
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	3.0 2.5	7.0 6.0	2.5 2.5	9.0 8.0	3.0 2.5	8.0 7.0	ns
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	8.0 8.0	2.5 2.5	10 10	3.0 3.0	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	5.0 6.0	2.0 2.0	6.5 8.0	2.0 2.0	6.0 7.0	ns

AC TEST CIRCUIT



PROPAGATION DELAY MEASUREMENTS



NOTES:
1. All input waveforms have the following characteristics:
   Low Level = 0V
   High Level = 3.0 V
   Rise and Fall Times (10% to 90%) = 2.5 ns
2. All timing is measured at 1.5 V unless otherwise indicated.