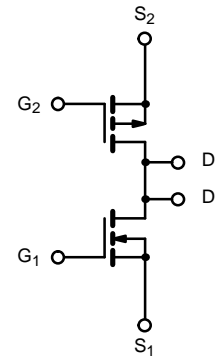
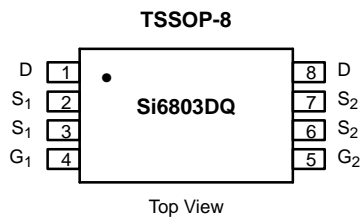




N- and P-Channel Half-Bridge, Reduced Q_g , Fast Switching

High-Efficiency
PWM Optimized

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.095 @ $V_{GS} = 4.5$ V	± 2.5
		0.145 @ $V_{GS} = 3.0$ V	± 2.0
P-Channel	-20	0.110 @ $V_{GS} = -4.5$ V	± 2.3
		0.165 @ $V_{GS} = -3.0$ V	± 1.9



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 2.5	± 2.3
		$T_A = 70^\circ\text{C}$	± 2.0	± 1.9
Pulsed Drain Current	I_{DM}	± 10		A
Continuous Source Current (Diode Conduction) ^a	I_S	1.0	-1.0	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.0	
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V	N-Ch		±100	nA	
			P-Ch		±100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = -20 V, V _{GS} = 0 V	P-Ch		-1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 70 °C	N-Ch		25		
		V _{DS} = -20 V, V _{GS} = 0 V, T _J = 70 °C	P-Ch		-25		
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N-Ch	10		A	
		V _{DS} = -5 V, V _{GS} = -4.5 V	P-Ch	-10			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 2.5 A	N-Ch		0.076	0.095	Ω
		V _{GS} = -4.5 V, I _D = -2.3 A	P-Ch		0.086	0.110	
		V _{GS} = 3.0 V, I _D = 2.0 A	N-Ch		0.105	0.145	
		V _{GS} = -3.0 V, I _D = -1.9 A	P-Ch		0.122	0.165	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 2.5 A	N-Ch		5.5	S	
		V _{DS} = -15 V, I _D = -2.3 A	P-Ch		6.0		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.0 A, V _{GS} = 0 V	N-Ch		0.75	1.1	V
		I _S = -1.0 A, V _{GS} = 0 V	P-Ch		0.75	1.1	
Dynamic^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 3.5 V, V _{GS} = 4.5 V, I _D = 0.3 A P-Channel V _{DS} = -3.5 V, V _{GS} = -4.5 V I _D = -0.3 A	N-Ch		3.8	7.5	nC
Gate-Source Charge	Q _{gs}		P-Ch		5.2	10	
Gate-Drain Charge	Q _{gd}		N-Ch		0.8		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 3.5 V, R _L = 11.5 Ω I _D ≅ 0.3 A, V _{GEN} = 4.5 V, R _G = 6 Ω P-Channel V _{DD} = -3.5 V, R _L = 11.5 Ω I _D ≅ -0.3 A, V _{GEN} = -4.5 V, R _G = 6 Ω	N-Ch		14	30	ns
Rise Time	t _r		P-Ch		12	30	
Turn-Off Delay Time	t _{d(off)}		N-Ch		34	70	
			P-Ch		32	70	
Fall Time	t _f		N-Ch		25	50	
			P-Ch		22	50	
Source-Drain Reverse Recovery Time	t _{rr}		N-Channel—I _F = 1.0 A, di/dt = 100 A/μs	N-Ch		50	
		P-Channel—I _F = -1.0 A, di/dt = 100 A/μs	P-Ch		50	80	

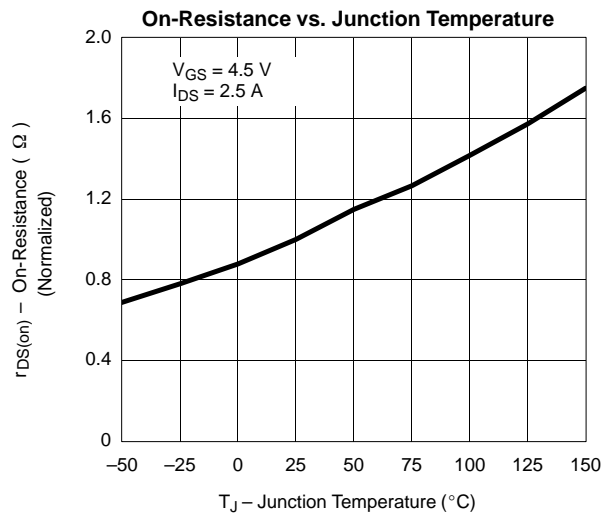
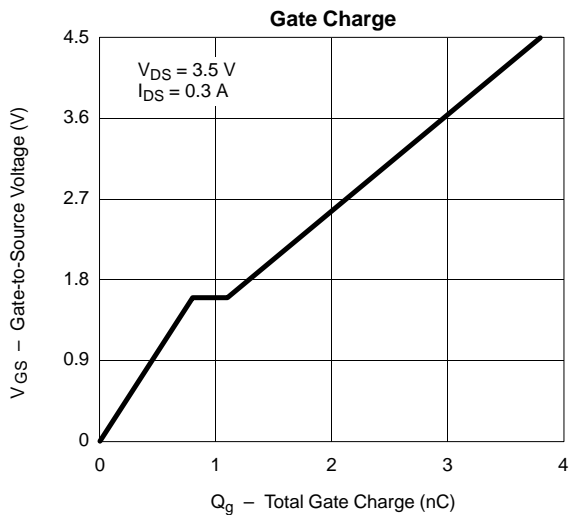
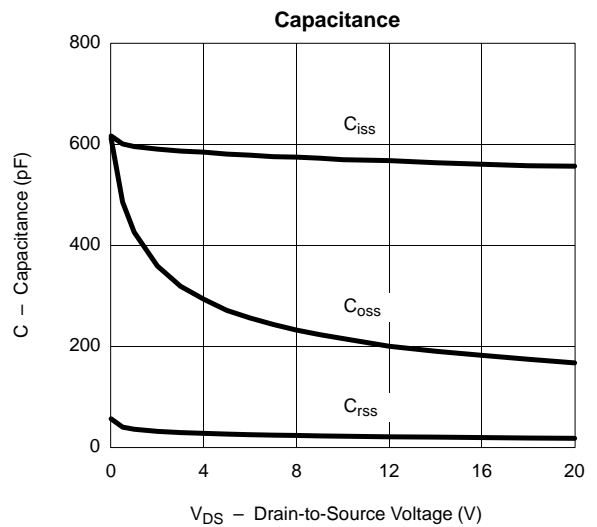
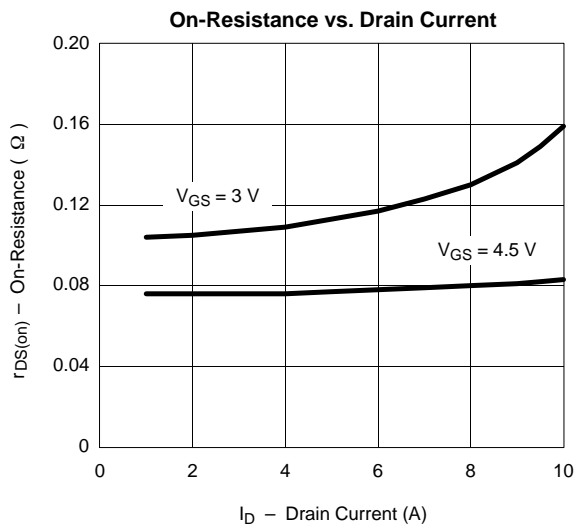
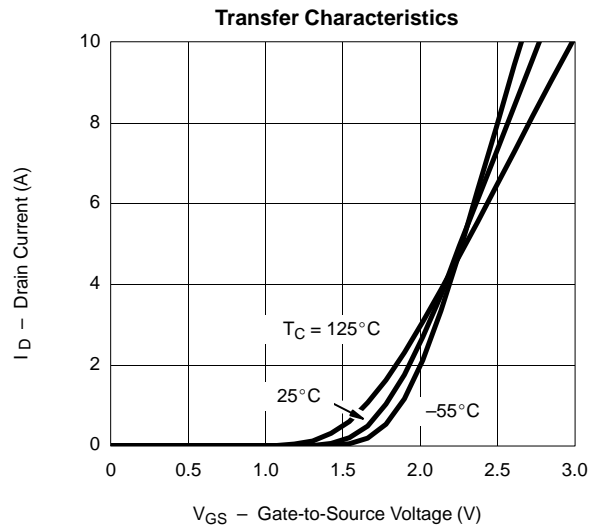
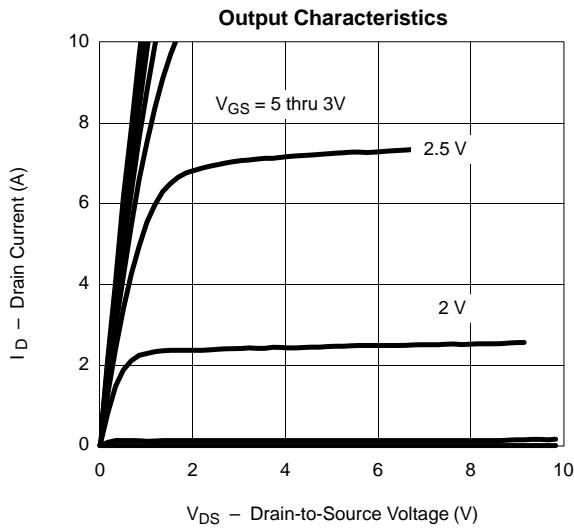
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

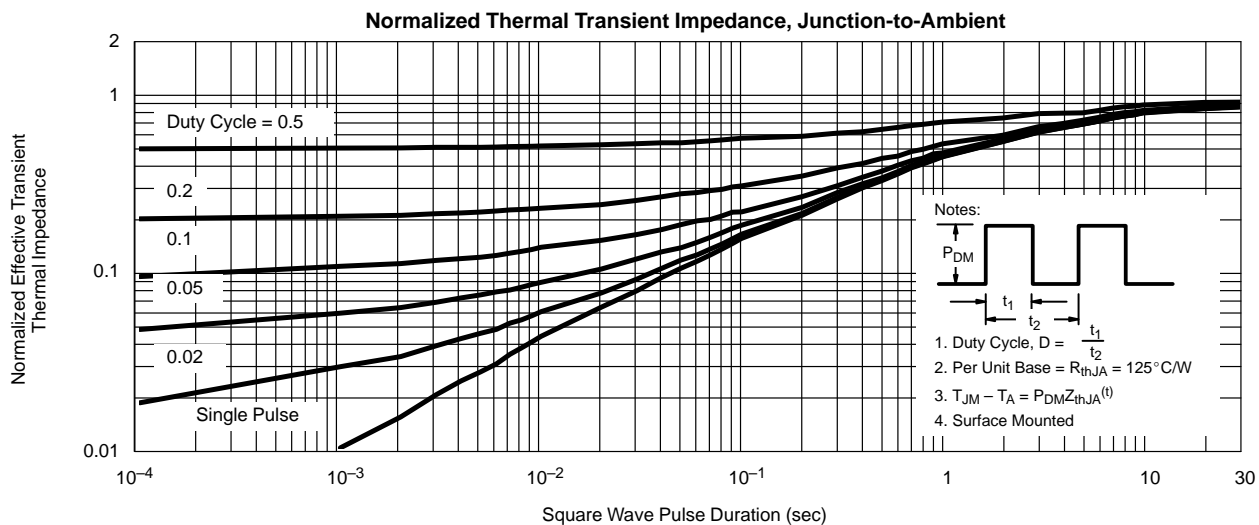
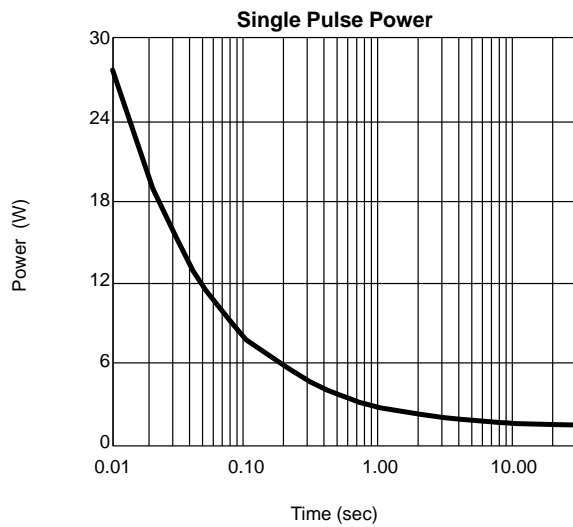
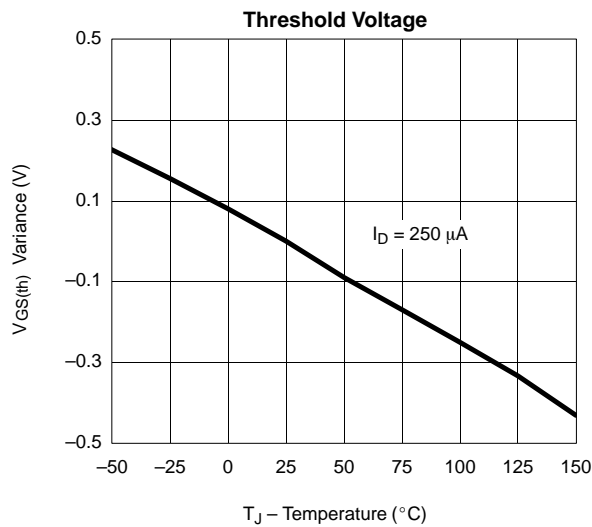
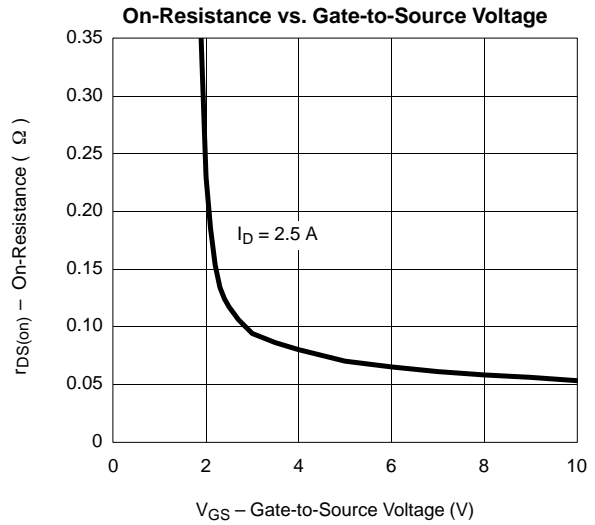
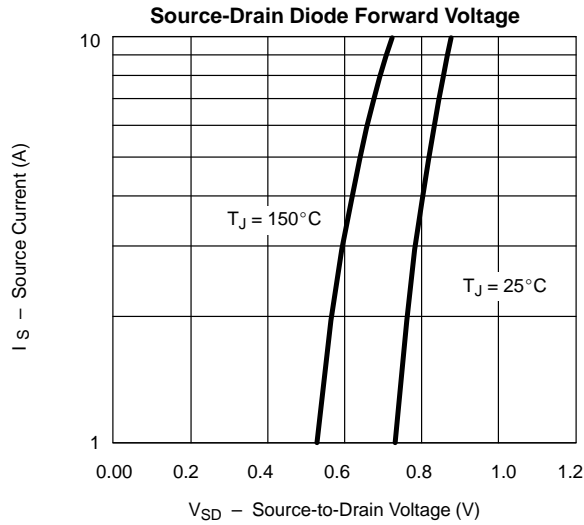


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL



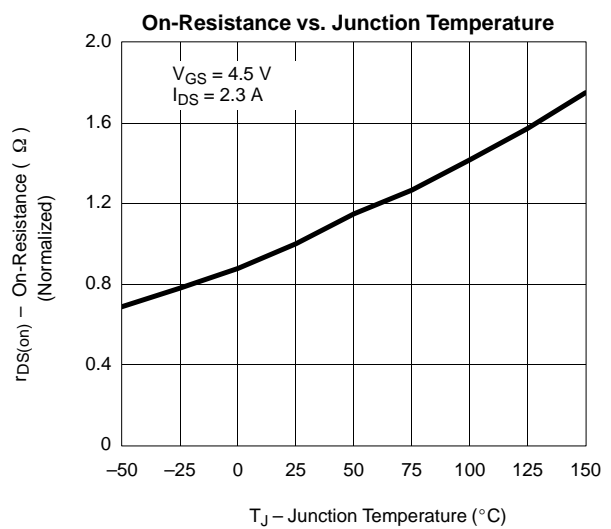
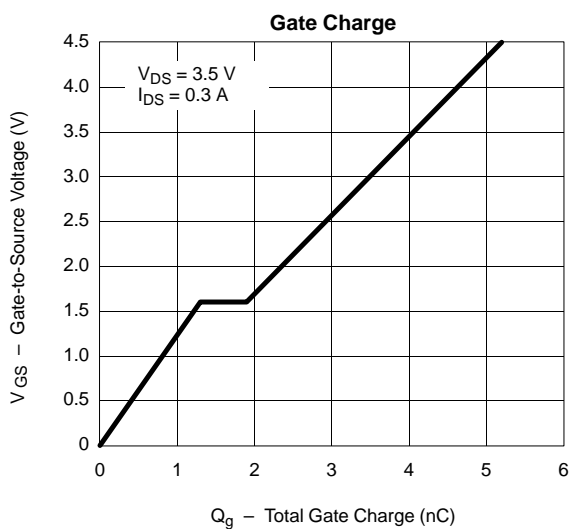
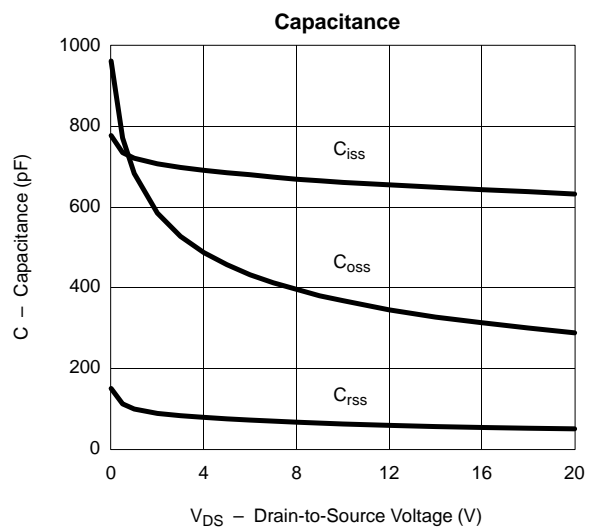
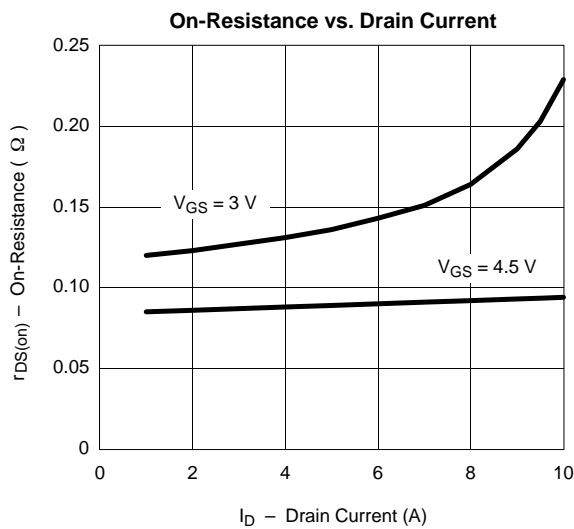
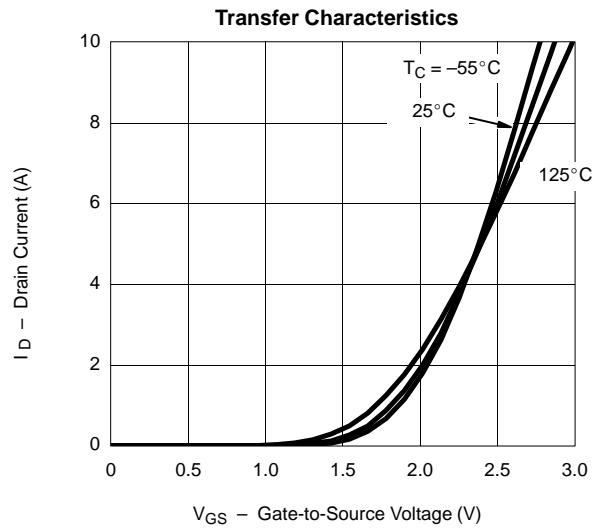
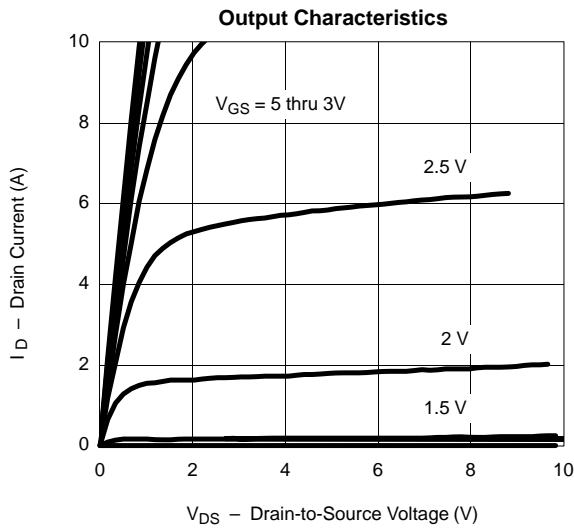
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL

