NEC

MOS INTEGRATED CIRCUIT

μPD42S16160L, 4216160L, 42S18160L, 4218160L

3.3 V OPERATION 16M-BIT DYNAMIC RAM
1M-WORD BY 16-BIT, FAST PAGE MODE, BYTE READ/WRITE MODE

DESCRIPTION

The μPD42S16160L, 4216160L, 42S18160L, 4218160L are 1 048 576 words by 16 bits dynamic CMOS RAMs.

These differ in refresh cycle and the μPD42S16160L, 42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh (see the table below).

These are packed in 50-pin plastic TSOP(II) and 42-pin plastic SOJ.

FEATURES

- 1 048 576 words by 16 bits organization
- Single +3.3 V ± 0.3 V power supply
- Fast page mode
- Byte read/write mode
- The μPD42S16160L, 42S18160L can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh.

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Part number	Refresh cycle	Refresh	Power consumption at standby (MAX.)
μPD42S16160L	4 096 cycles/128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	0.54 mW (CMOS level input)
μPD42S18160L	1 024 cycles/128 ms		
μPD4216160L	4 096 cycles/64 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh	1.8 mW (CMOS level input)
μPD4218160L	1 024 cycles/16 ms		

★ ★

- Fast access and cycle time

Part number	Power consumption Active (MAX.)	Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
μPD42S16160L-A60, 4216160L-A60	324 mW	60 ns	110 ns	40 ns
μPD42S18160L-A60, 4218160L-A60	540 mW			
μPD42S16160L-A70, 4216160L-A70	288 mW	70 ns	130 ns	45 ns
μPD42S18160L-A70, 4218160L-A70	504 mW			
μPD42S16160L-A80, 4216160L-A80	252 mW	80 ns	150 ns	50 ns
μPD42S18160L-A80, 4218160L-A80	468 mW			

The information in this document is subject to change without notice.

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The mark ★ shows revised points.

ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Refresh
μPD42S16160LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil) Normal pinout	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S18160LG5-A60			
μPD42S16160LG5-A70	70 ns		
μPD42S18160LG5-A70			
μPD42S16160LG5-A80	80 ns		
μPD42S18160LG5-A80			
μPD42S16160LG5M-A60	60 ns	50-pin plastic TSOP (II) (400 mil) Reverse pinout	
μPD42S18160LG5M-A60			
μPD42S16160LG5M-A70	70 ns		
μPD42S18160LG5M-A70			
μPD42S16160LG5M-A80	80 ns		
μPD42S18160LG5M-A80			
μPD42S16160LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD42S18160LLE-A60			
μPD42S16160LLE-A70	70 ns		
μPD42S18160LLE-A70			
μPD42S16160LLE-A80	80 ns		
μPD42S18160LLE-A80			
μPD4216160LG5-A60	60 ns	50-pin plastic TSOP (II) (400 mil) Normal pinout	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4218160LG5-A60			
μPD4216160LG5-A70	70 ns		
μPD4218160LG5-A70			
μPD4216160LG5-A80	80 ns		
μPD4218160LG5-A80			
μPD4216160LG5M-A60	60 ns	50-pin plastic TSOP (II) (400 mil) Reverse pinout	
μPD4218160LG5M-A60			
μPD4216160LG5M-A70	70 ns		
μPD4218160LG5M-A70			
μPD4216160LG5M-A80	80 ns		
μPD4218160LG5M-A80			
μPD4216160LLE-A60	60 ns	42-pin plastic SOJ (400 mil)	
μPD4218160LLE-A60			
μPD4216160LLE-A70	70 ns		
μPD4218160LLE-A70			
μPD4216160LLE-A80	80 ns		
μPD4218160LLE-A80			

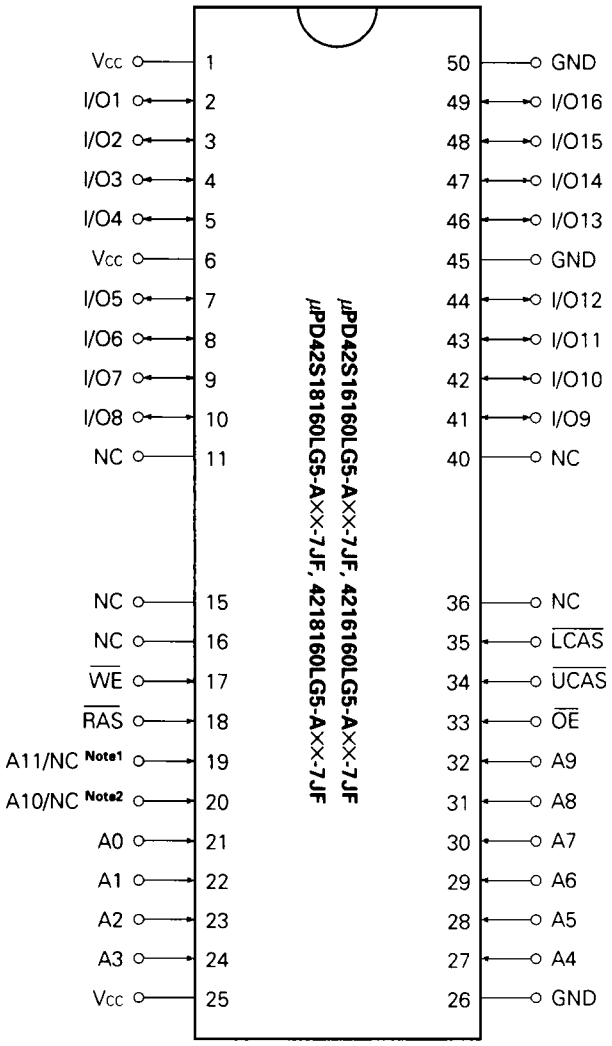
QUALITY GRADE

STANDARD

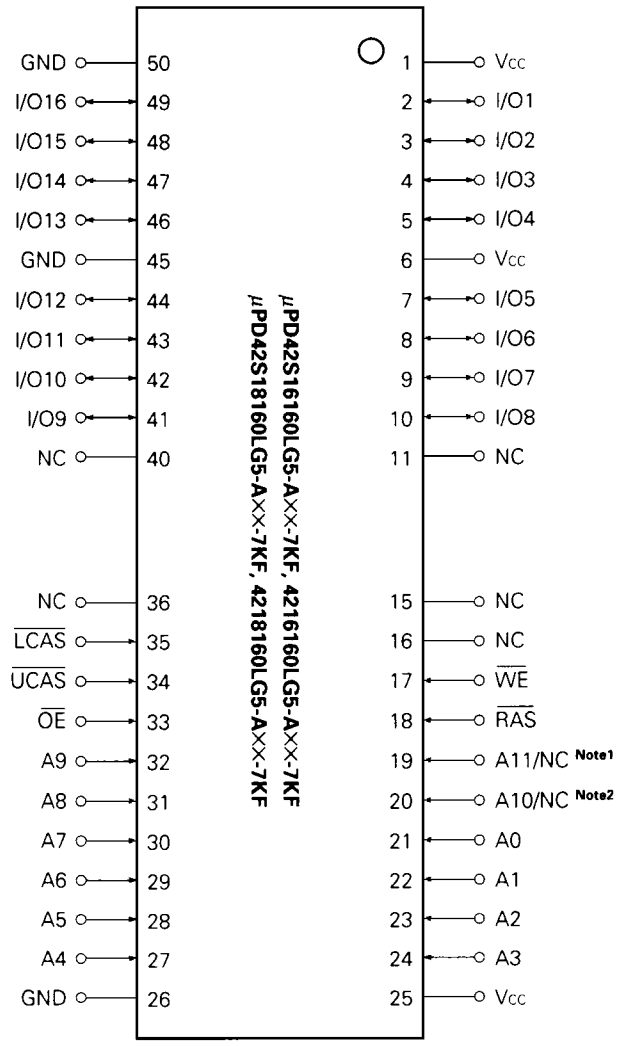
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking side)

50-pin Plastic TSOP (II)



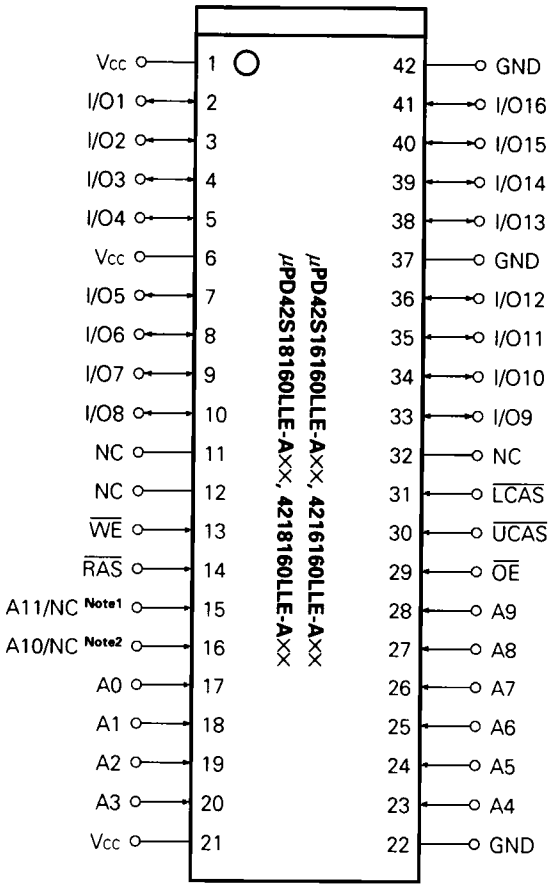
Reverse bent



Notes 1. A11 . . . μPD42S16160L, 4216160L NC . . . μPD42S18160L, 4218160L
2. A10 . . . μPD42S16160L, 4216160L NC . . . μPD42S18160L, 4218160L

A0 to A11	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Supply Voltage
GND	:	Ground
NC	:	No Connection

42-pin Plastic SOJ



Notes 1. A11 . . . μPD42S16160L, 4216160L NC . . . μPD42S18160L, 4218160L
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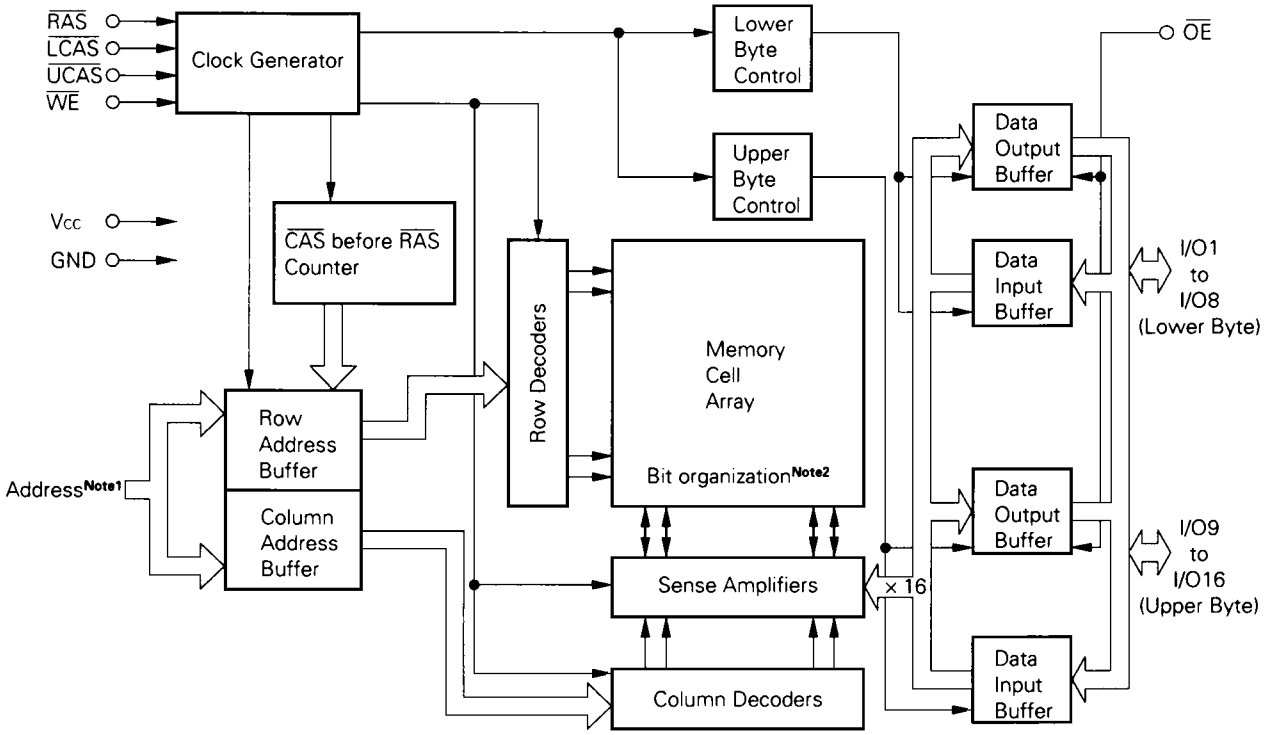
A0 to A11	:	Address Inputs
I/O1 to I/O16	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{UCAS}$	:	Column Address Strobe (upper)
$\overline{LCAS}$	:	Column Address Strobe (lower)
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Supply Voltage
GND	:	Ground
NC	:	No Connection

BLOCK DIAGRAM



Notes 1.

Part number	Row address	Column address
μPD42S16160L, 4216160L	A0 to A11	A0 to A7
μPD42S18160L, 4218160L	A0 to A9	A0 to A9

2. μPD42S16160L, 4216160L · · · 4 096× 256 × 16 μPD42S18160L, 4218160L · · · 1 024× 1 024 × 16

INPUT/OUTPUT PIN FUNCTIONS

The μPD42S16160L, 4216160L, 42S18160L, 4218160L have input pins $\overline{RAS}$, $\overline{CAS}$ Note1, $\overline{WE}$, $\overline{OE}$, A0 to A11/A9 Note2 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh.
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A11/A9 Note2 (Address input)		Address bus. Input total 20-bit of address signal, upper 12/10 Note3-bit and lower 8/10 Note4-bit in sequence (address multiplex method). Therefore, one word is selected from 1 048 576-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data input/output)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Notes 1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

2. A11 ··· μPD42S16160L, 4216160L A9 ··· μPD42S18160L, 4218160L

3. 12 ··· μPD42S16160L, 4216160L 10 ··· μPD42S18160L, 4218160L

4. 8 ··· μPD42S16160L, 4216160L 10 ··· μPD42S18160L, 4218160L

ELECTRICAL SPECIFICATIONS Notes 1, 2, 3

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Ambient Temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	A0 to A11			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O1 to I/O16			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

[μPD42S16160L, 4216160L]

Parameter		Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	4, 5, 8
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
★ Standby current	μPD42S16160L	I_{CC2}	$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5	mA	
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.15		
	μPD4216160L		$V_{IH(MIN.)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN.)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	4,5,6,8
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	4, 5, 7
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	4, 5
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
★ $\overline{CAS}$ before $\overline{RAS}$ long refresh current (4 096 cycles/128 ms, only for μPD42S16160L)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 4 096 cycles/128 ms $\overline{RAS}, \overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ $\overline{WE}, \overline{OE}$: V_{IH} Address input : Don't care Output : Open	$t_{RAS} \leqq 1\ \mu s$		220	μA	4, 5
★ Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S16160L)		I_{CC7}	I_O = 0 mA $\overline{RAS}, \overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$			150	μA	
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 3.6 V		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.0 mA			0.4	V	

[μPD42S18160L, 4218160L]

Parameter		Symbol	Test Condition		MIN.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	4, 5, 8
				t_{RAC} = 70 ns		140		
				t_{RAC} = 80 ns		130		
Standby current	μPD42S18160L	I_{CC2}	$V_{IH(MIN.)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5	mA	★
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.15		
	μPD4218160L		$V_{IH(MIN.)} \leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		2		
			V_{CC}–0.2 V $\leqq \overline{RAS}$, $\overline{CAS}$	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $V_{IH(MIN.)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	4,5,6,8
				t_{RAC} = 70 ns		140		
				t_{RAC} = 80 ns		130		
Operating current (Fast page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$ $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		90	mA	4, 5, 7
				t_{RAC} = 70 ns		80		
				t_{RAC} = 80 ns		70		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling, $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 60 ns		150	mA	4, 5
				t_{RAC} = 70 ns		140		
				t_{RAC} = 80 ns		130		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (1 024 cycles/128 ms, only for μPD42S18160L)		I_{CC6}	Standby : V_{CC}–0.2 V $\leqq \overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 1 024 cycles/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ $\overline{WE}$, $\overline{OE}$: V_{IH} Address input : Don't care Output : Open	$t_{RAS} \leqq 1$ μs		180	μA	4, 5 ★
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for μPD42S18160L)		I_{CC7}	I_O = 0 mA $\overline{RAS}$, $\overline{CAS}$: 0 V $\leqq V_{IL} \leqq$ 0.2 V V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$			150	μA	★
Input leakage current		$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current		$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 3.6 V		–5	+5	μA	
High level output voltage		V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage		V_{OL}	I_O = 2.0 mA			0.4	V	

AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted) Notes 9, 10 (1/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read or Write Cycle Time	t_{RC}	110		130		150		ns	
Read Modify Write Cycle Time	t_{RWC}	160		180		200		ns	
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		ns	
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	85		90		105		ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	11, 12
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		20		20	ns	11, 12
Access Time from Column Address	t_{AA}		30		35		40	ns	11, 12
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45	ns	12
Access Time from $\overline{OE}$	t_{OEA}		15		20		20	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	ns	11
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		ns	12
$\overline{OE}$ to Data Setup Time	t_{OLZ}	0		0		0		ns	12
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	13	0	15	0	15	ns	13
$\overline{OE}$ to Data Delay Time	t_{OED}	13		15		15		ns	
Output Buffer Turn-off Delay Time ($\overline{OE}$)	t_{OEZ}	0	13	0	15	0	15	ns	13
$\overline{OE}$ Command Hold Time	t_{OEH}	0		0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive Setup Time	t_{OES}	0		0		0		ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	15		18		20		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	20	10 000	20	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	25	60	ns	11
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	14
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5		5		5		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		ns	
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		ns	

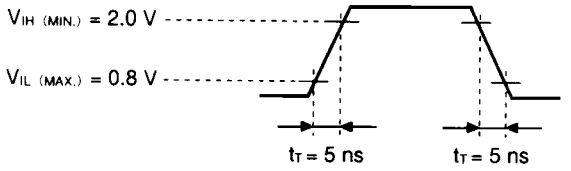
(2/2)

Parameter		Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Column Address Setup Time		t_{ASC}	0		0		0		ns	
Column Address Hold Time		t_{CAH}	15		15		15		ns	
Column Address Lead Time Referenced to $\overline{RAS}$		t_{RAL}	30		35		40		ns	
Read Command Setup Time		t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	0		0		0		ns	15
Read Command Hold Time Referenced to $\overline{CAS}$		t_{RCH}	0		0		0		ns	15
Write Command Hold Time Referenced to $\overline{CAS}$		t_{WCH}	10		10		15		ns	16
Write Command Pulse Width		t_{WP}	10		10		15		ns	16
Data-in Setup Time		t_{DS}	0		0		0		ns	17
Data-in Hold Time		t_{DH}	10		15		15		ns	17
$\overline{WE}$ Command Setup Time		t_{WCS}	0		0		0		ns	18
$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	38		40		45		ns	18
$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	83		95		105		ns	18
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)		t_{CPWD}	60		65		70		ns	18
Column Address Delay Time Referenced to $\overline{WE}$		t_{AWD}	53		60		65		ns	18
Write Command Lead Time Referenced to $\overline{RAS}$		t_{RWL}	20		20		20		ns	
Write Command Lead Time Referenced to $\overline{CAS}$		t_{CWL}	15		15		15		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CSR}	5		5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh		t_{CHR}	10		10		10		ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RASS}	100		100		100		μs	19
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{RPS}	110		130		150		ns	19
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)		t_{CHS}	−50		−50		−50		ns	19
$\overline{WE}$ Hold Time		t_{WHR}	15		15		15		ns	★
Masked Byte Write Hold Time Referenced to $\overline{RAS}$		t_{MRH}	0		0		0		ns	
Refresh Time	μPD42S16160L, 42S18160L	t_{REF}		128		128		128	ms	19 ★
	μPD4216160L			64		64		64		
	μPD4218160L			16		16		16		

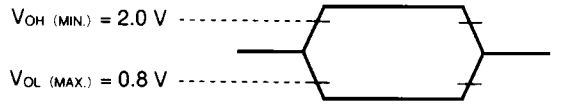
Notes

1. $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
2. All voltages are referenced to GND.
3. After power up, wait more than 100 μs ($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.
4. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
5. Specified values are obtained with outputs unloaded.
6. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
7. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.
8. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.
9. AC measurements assume t_T = 5 ns.
10. AC Characteristics test condition

    (1) Input timing specification



    (2) Output timing specification

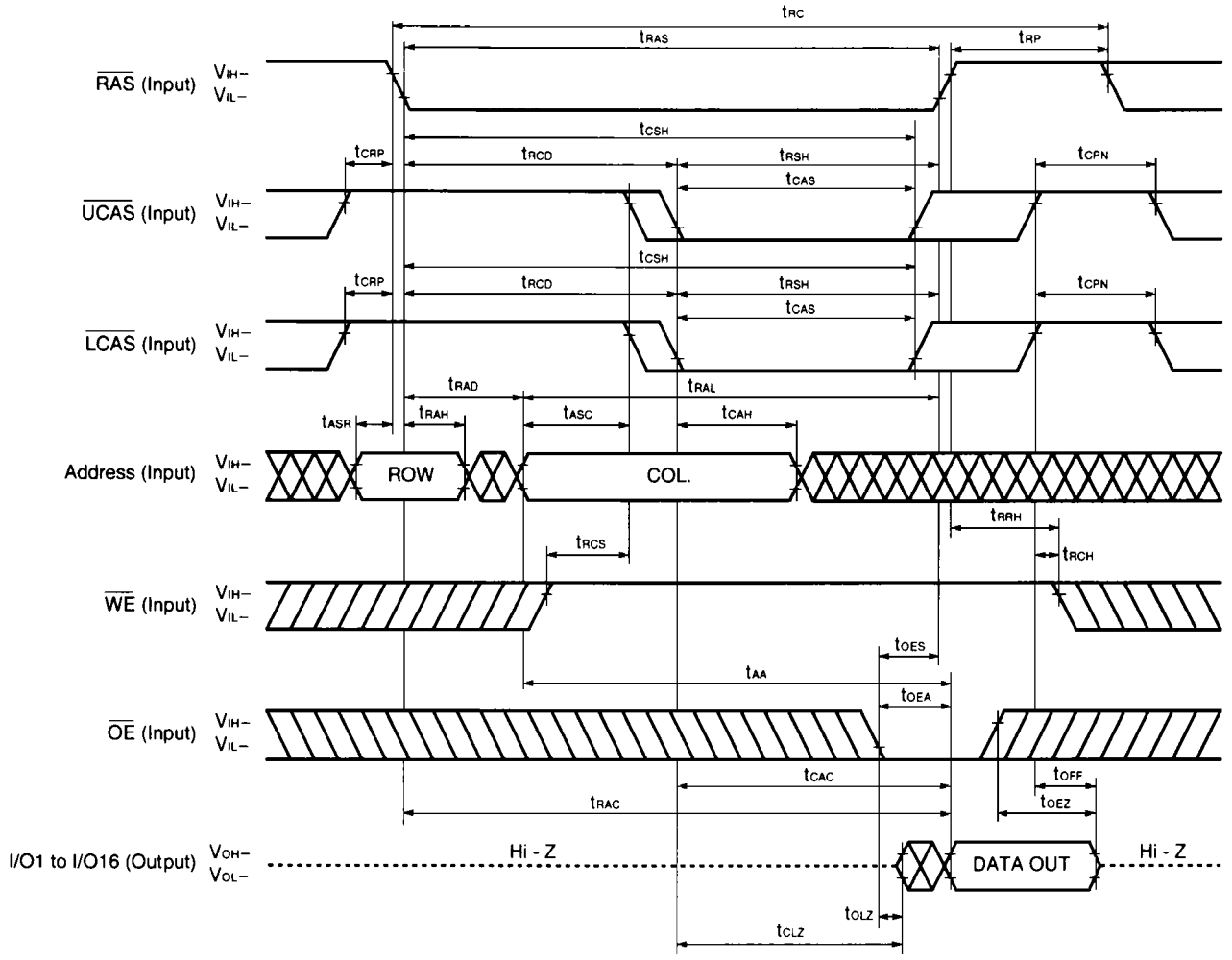


11. For read cycles, access time is defined as follows :

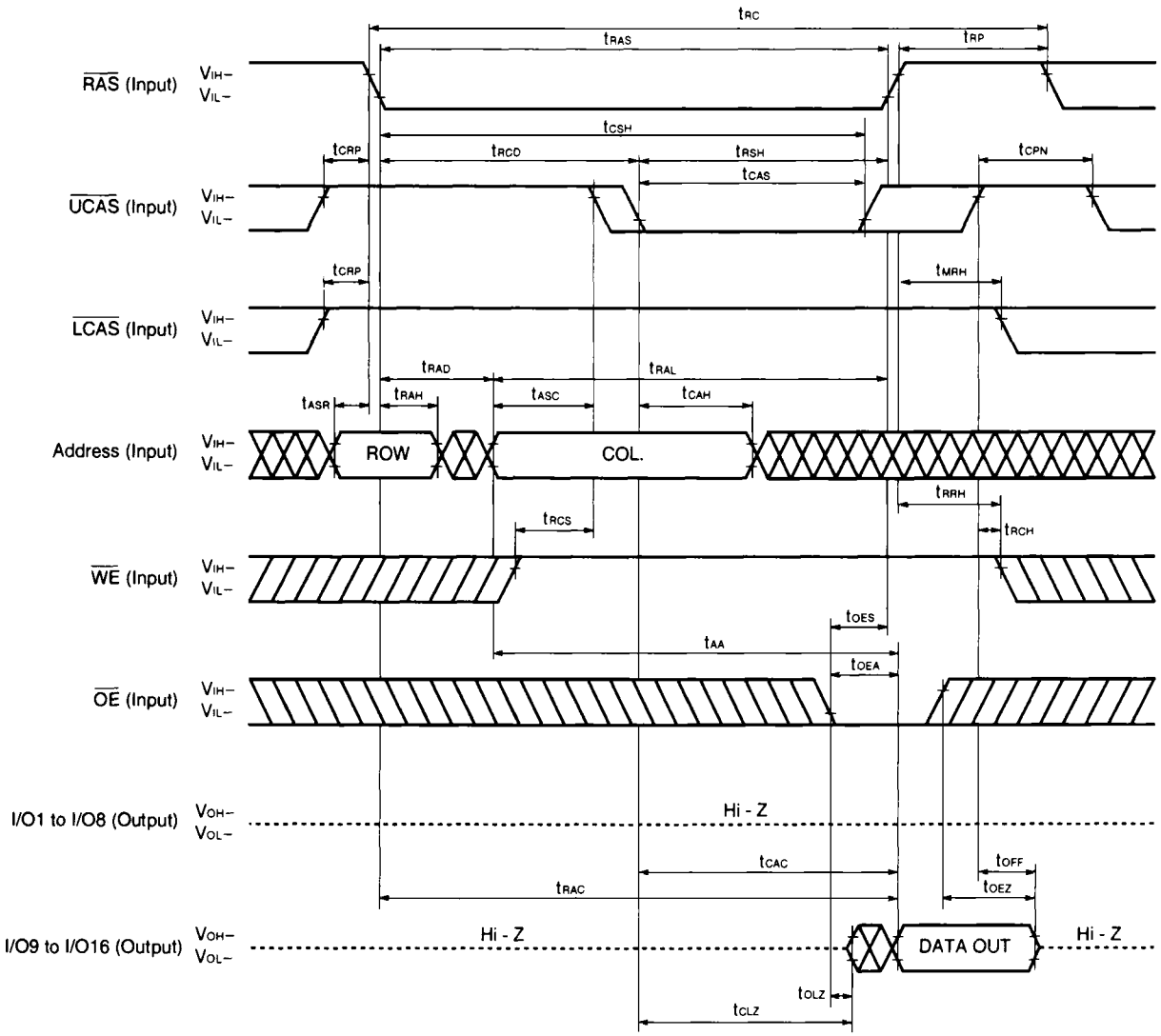
Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD(MAX.)}$, $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD} > t_{RAD(MAX.)}$, $t_{RCD} \leqq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$	$t_{RAD} + t_{AA(MAX.)}$
$t_{RCD} > t_{RCD(MAX.)}$	$t_{CAC(MAX.)}$	$t_{RCD} + t_{CAC(MAX.)}$

    $t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.
12. Loading conditions are 1TTL and 100 pF.
13. $t_{OFF(MAX.)}$ and $t_{OEZ(MAX.)}$ define the time at which the output achieves the condition of Hi-Z and are not referenced to V_{OH} or V_{OL}.
14. $t_{CRP(MIN.)}$ requirement should be applied for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.
15. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
16. $t_{WP(MIN.)}$ is applied for late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.
17. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.
18. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$ and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.
19. This specification is applied only for the μPD42S16160L, 42S18160L.

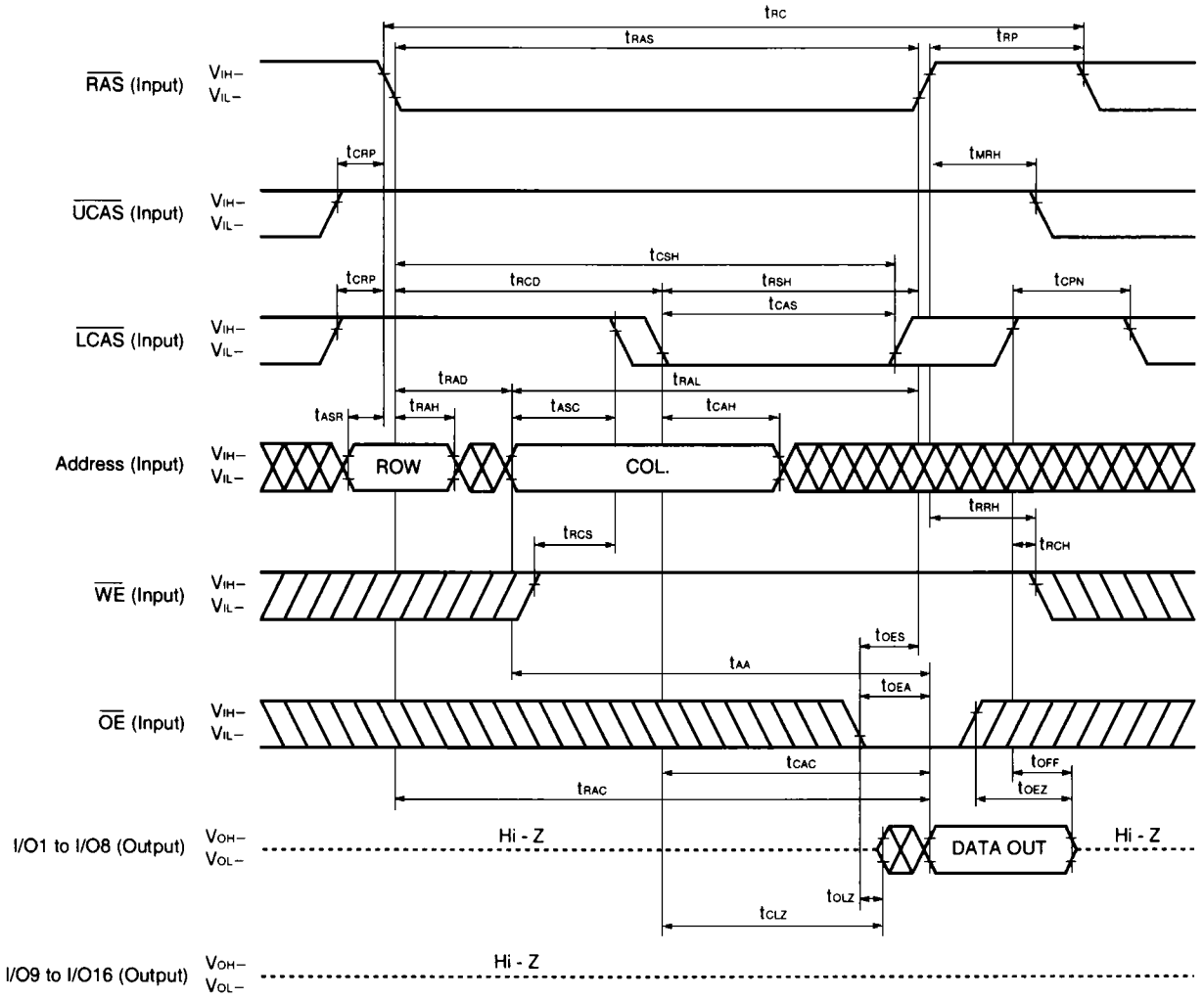
READ CYCLE


tRC
tRAS
tRP
RAS (Input)
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
UCAS (Input)
LCAS (Input)
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address (Input)
ROW
COL.
tRRH
tRCS
tRCH
WE (Input)
tOES
tAA
tOEA
OE (Input)
tCAC
tOFF
tRAC
tOEZ
I/O1 to I/O16 (Output)
VOH–
VOL–
Hi - Z
DATA OUT
tOLZ
tCLZ

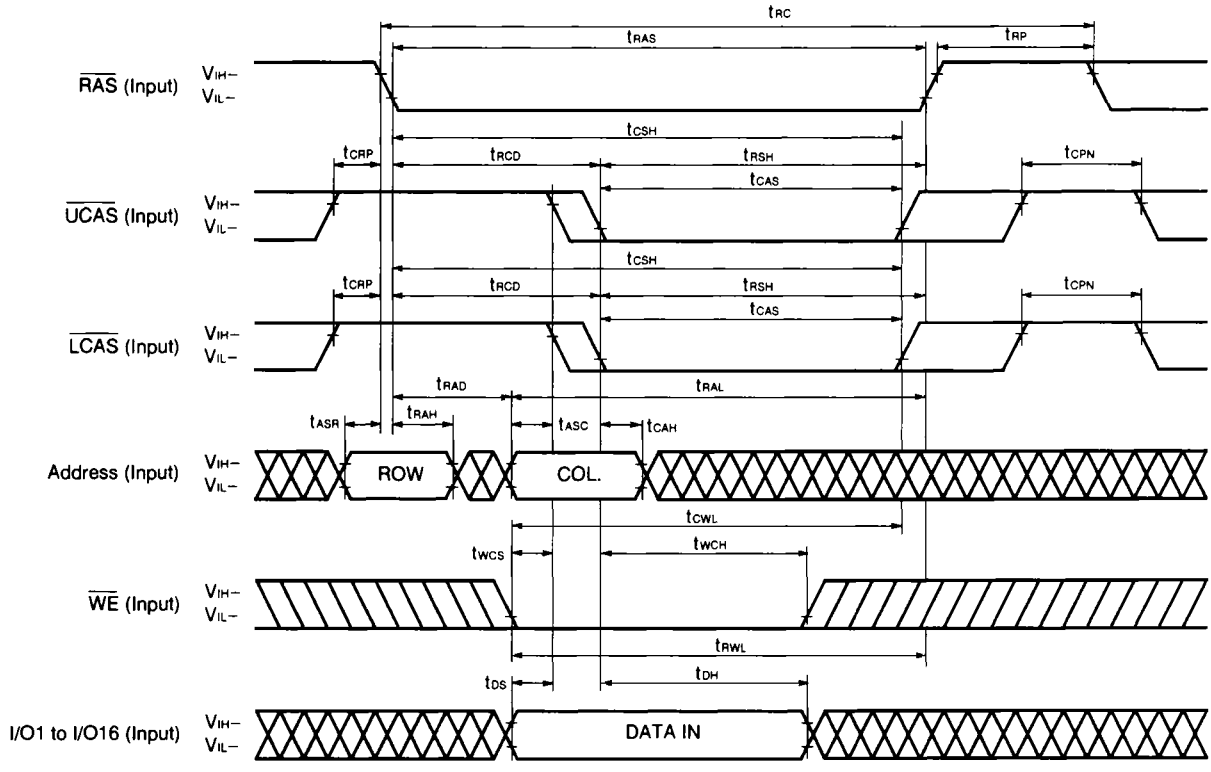
UPPER BYTE READ CYCLE



LOWER BYTE READ CYCLE

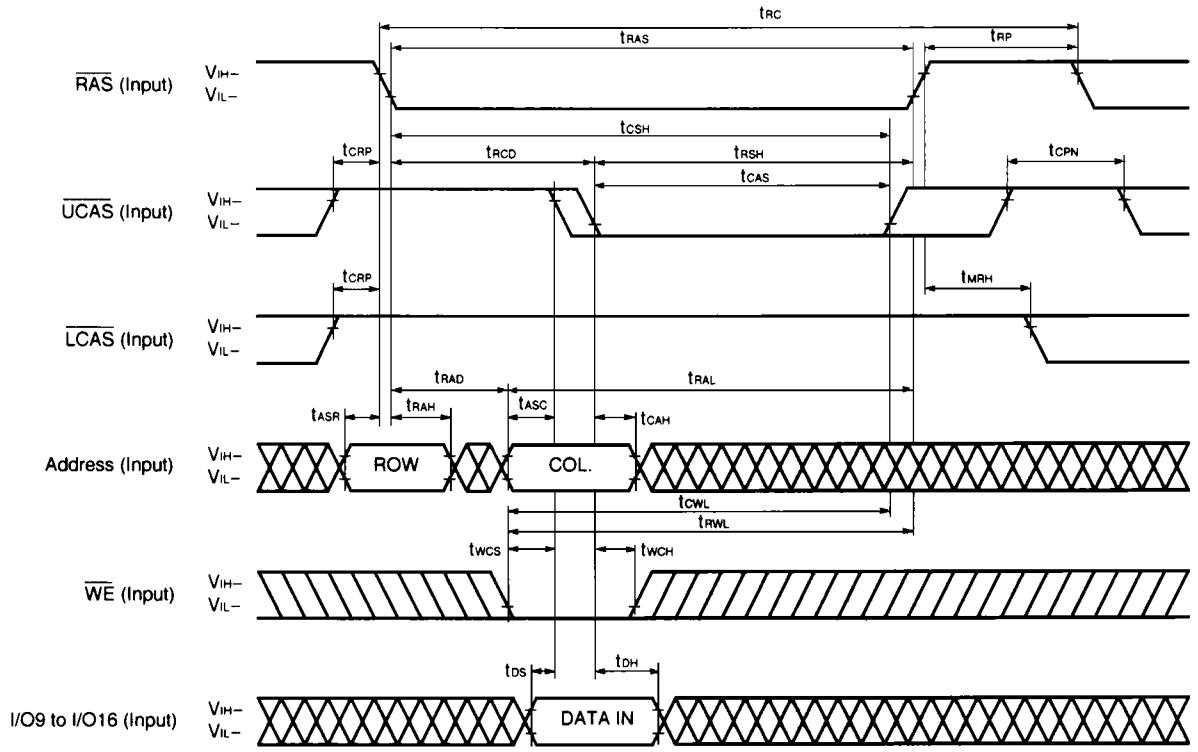


EARLY WRITE CYCLE



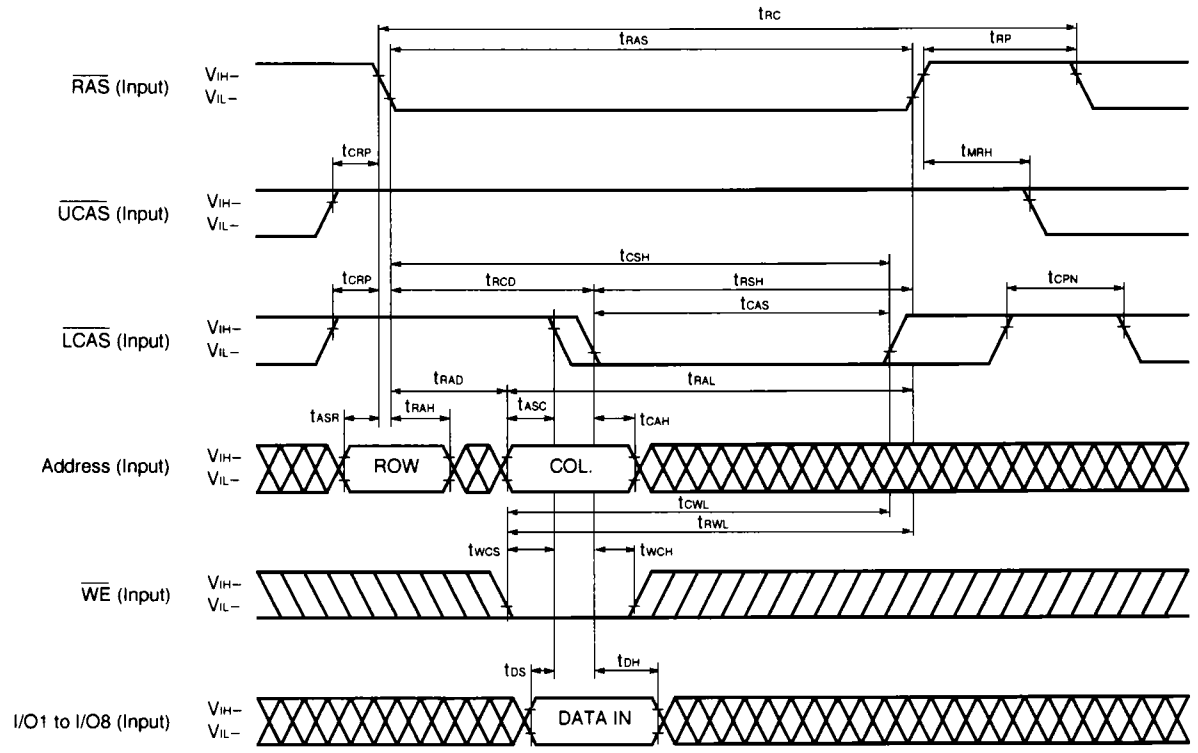
Remark $\overline{OE}$ = Don't care

UPPER BYTE EARLY WRITE CYCLE



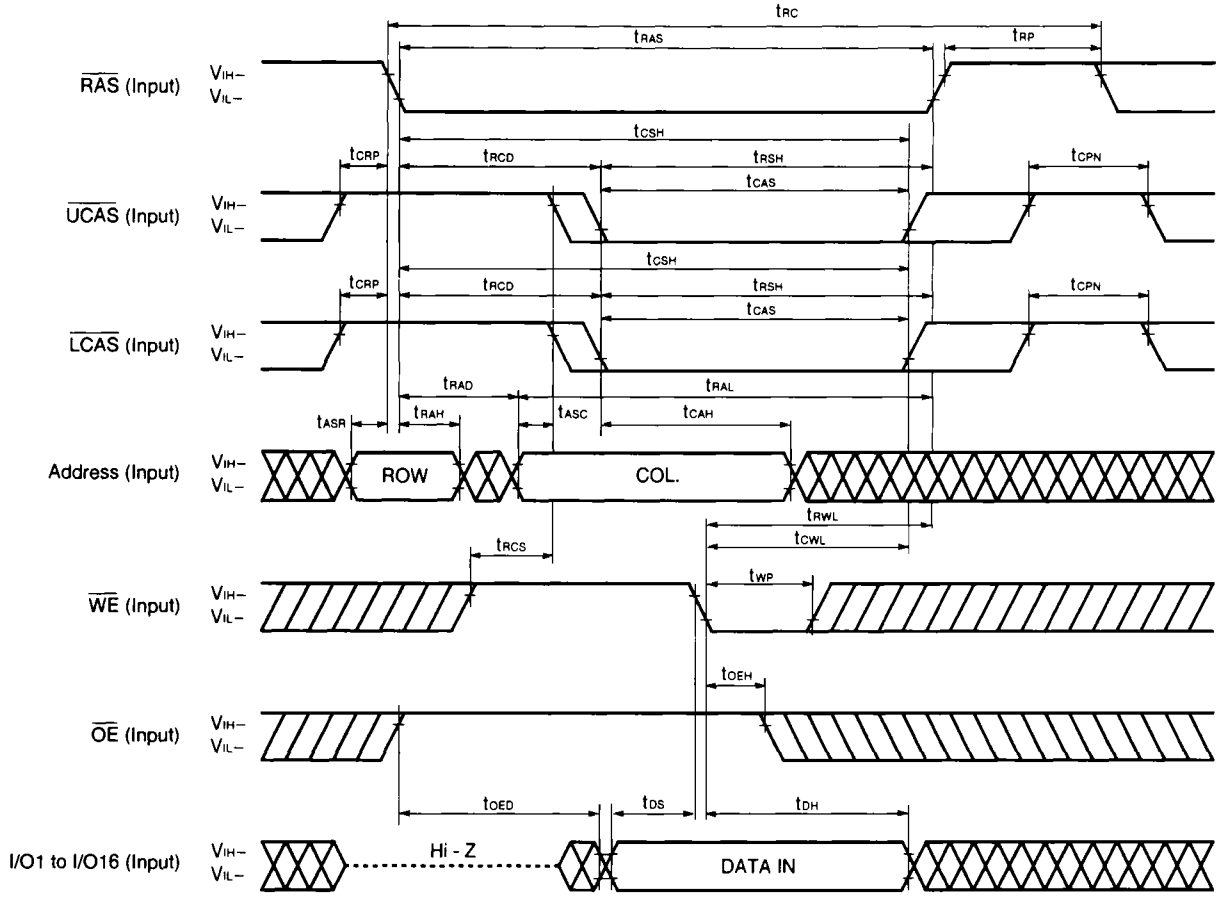
Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

LOWER BYTE EARLY WRITE CYCLE

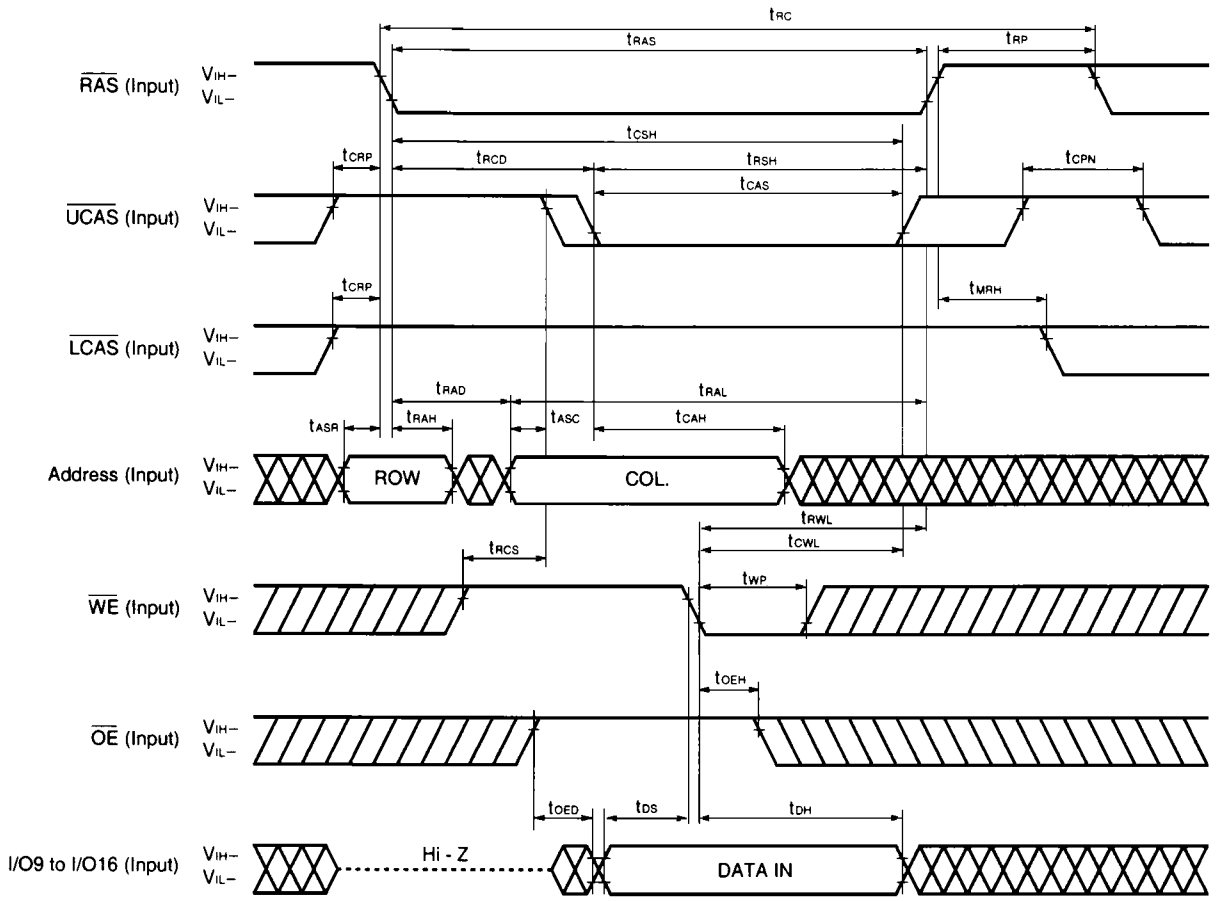


Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

LATE WRITE CYCLE

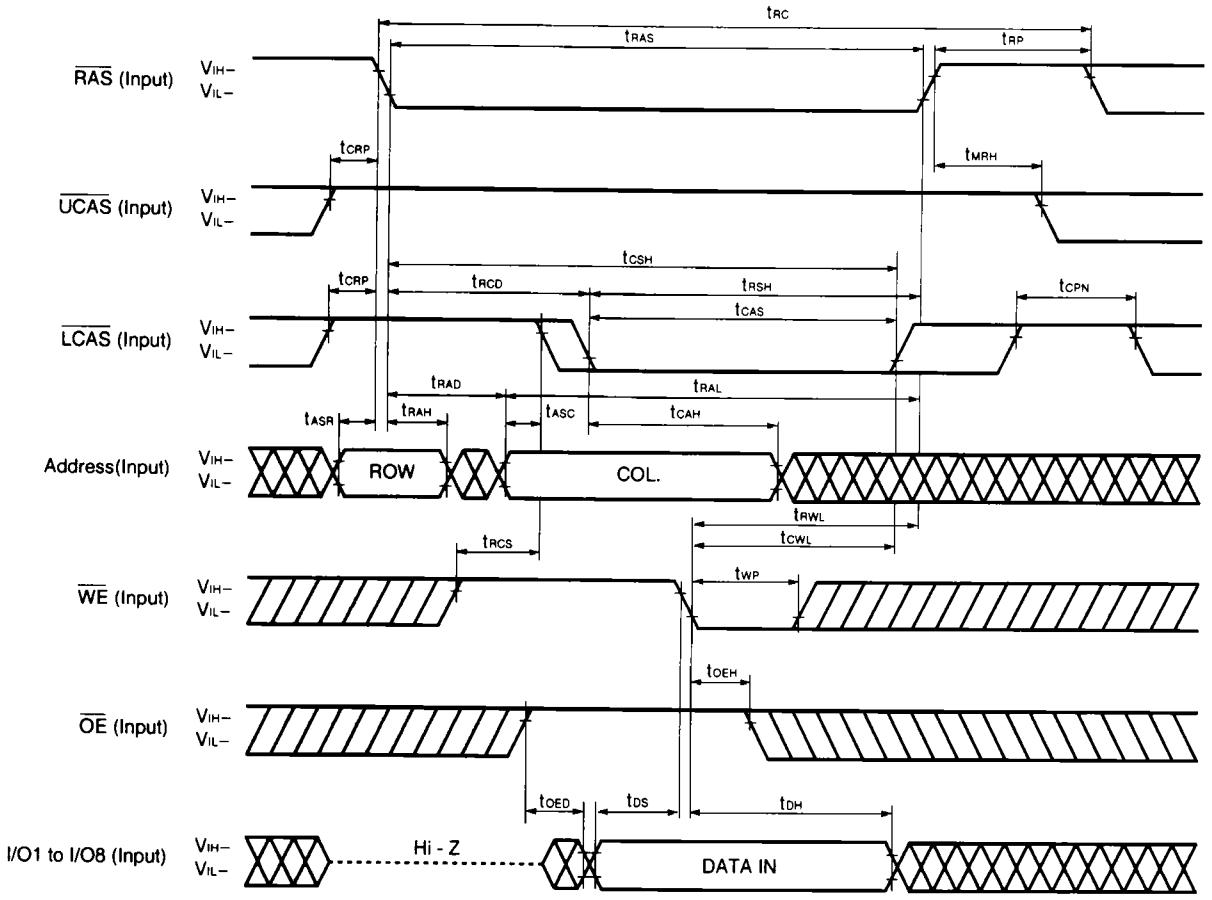


UPPER BYTE LATE WRITE CYCLE



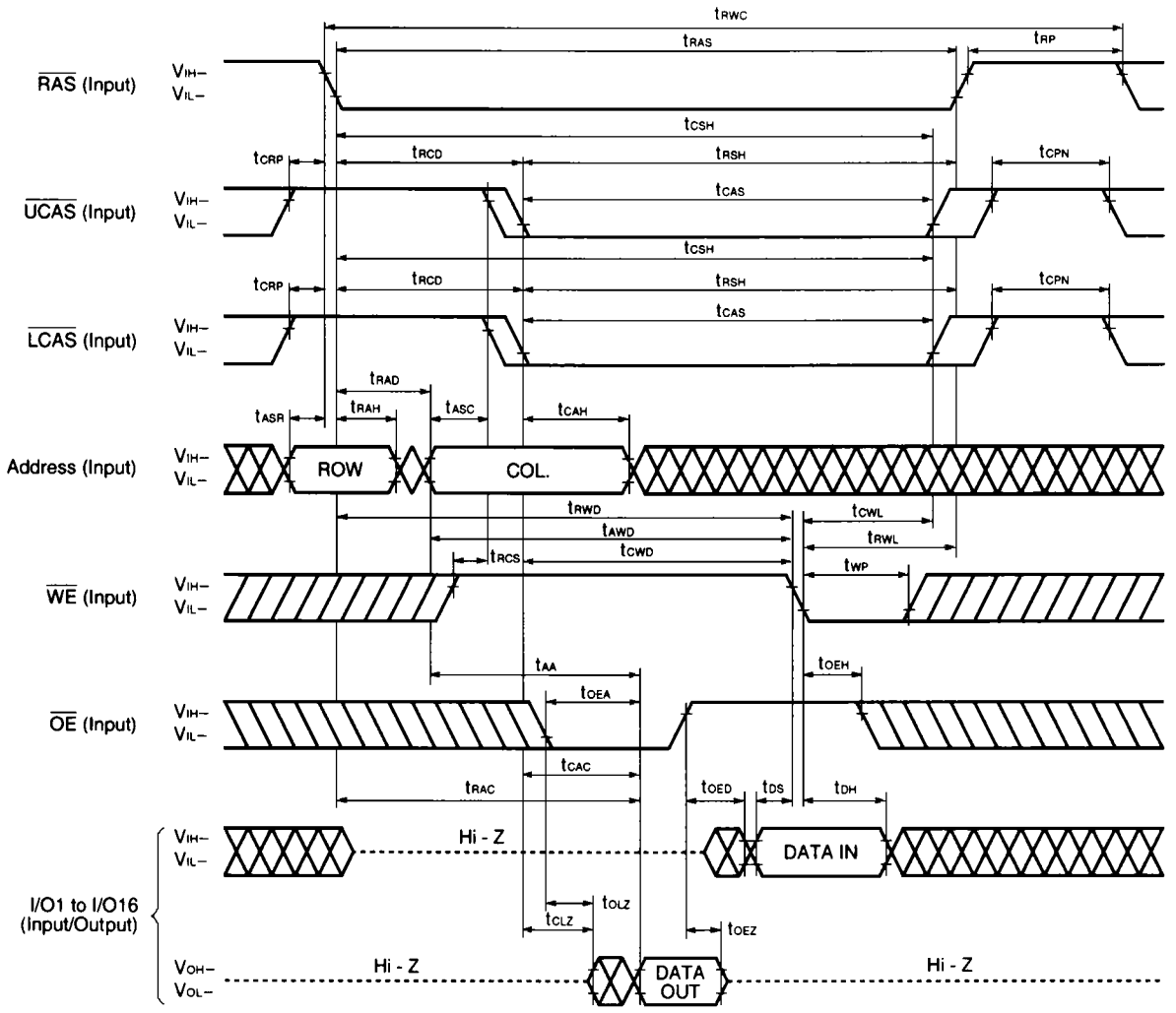
Remark I/O1 to I/O8 = Don't care

LOWER BYTE LATE WRITE CYCLE

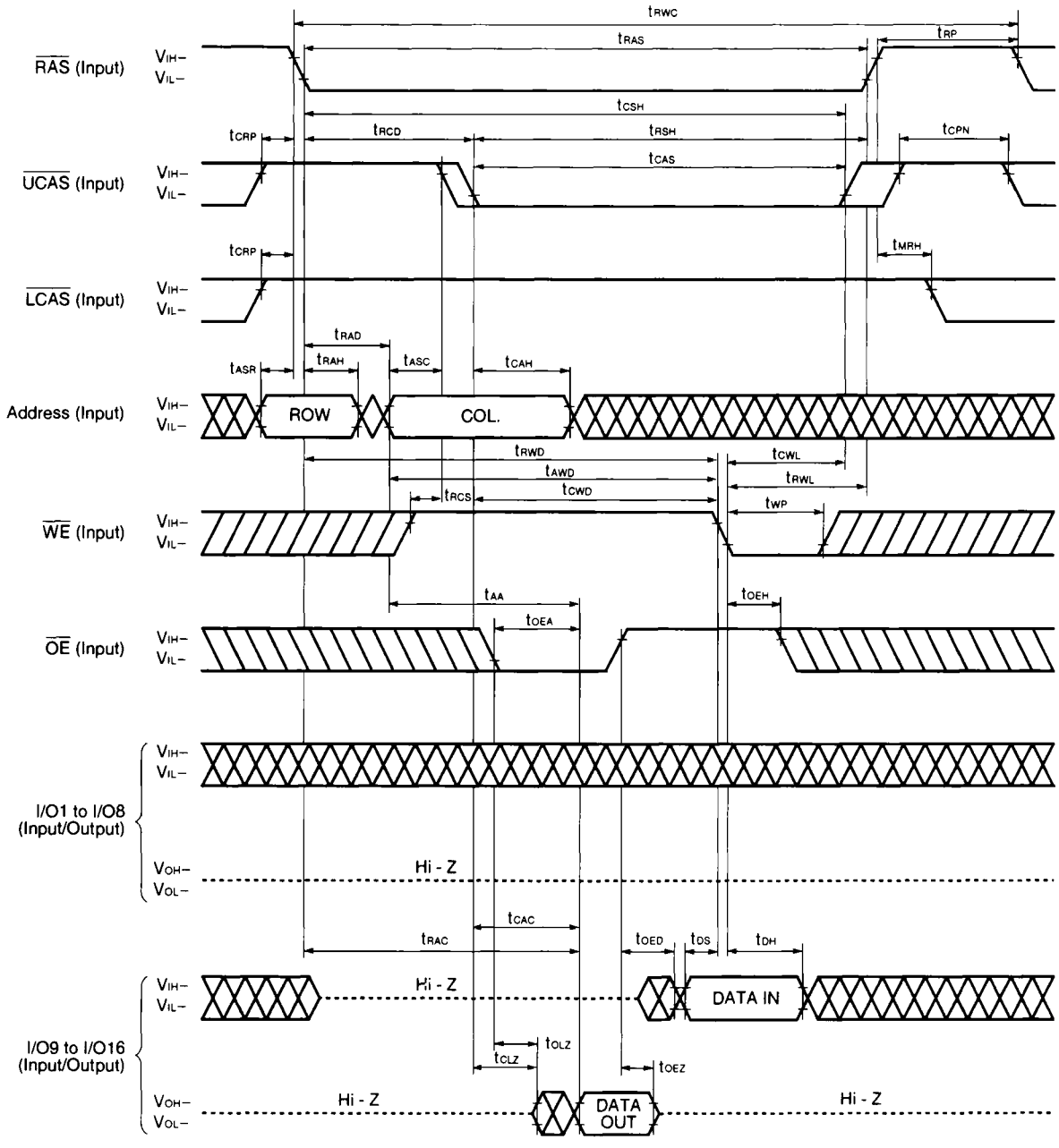


Remark I/O9 to I/O16 = Don't care

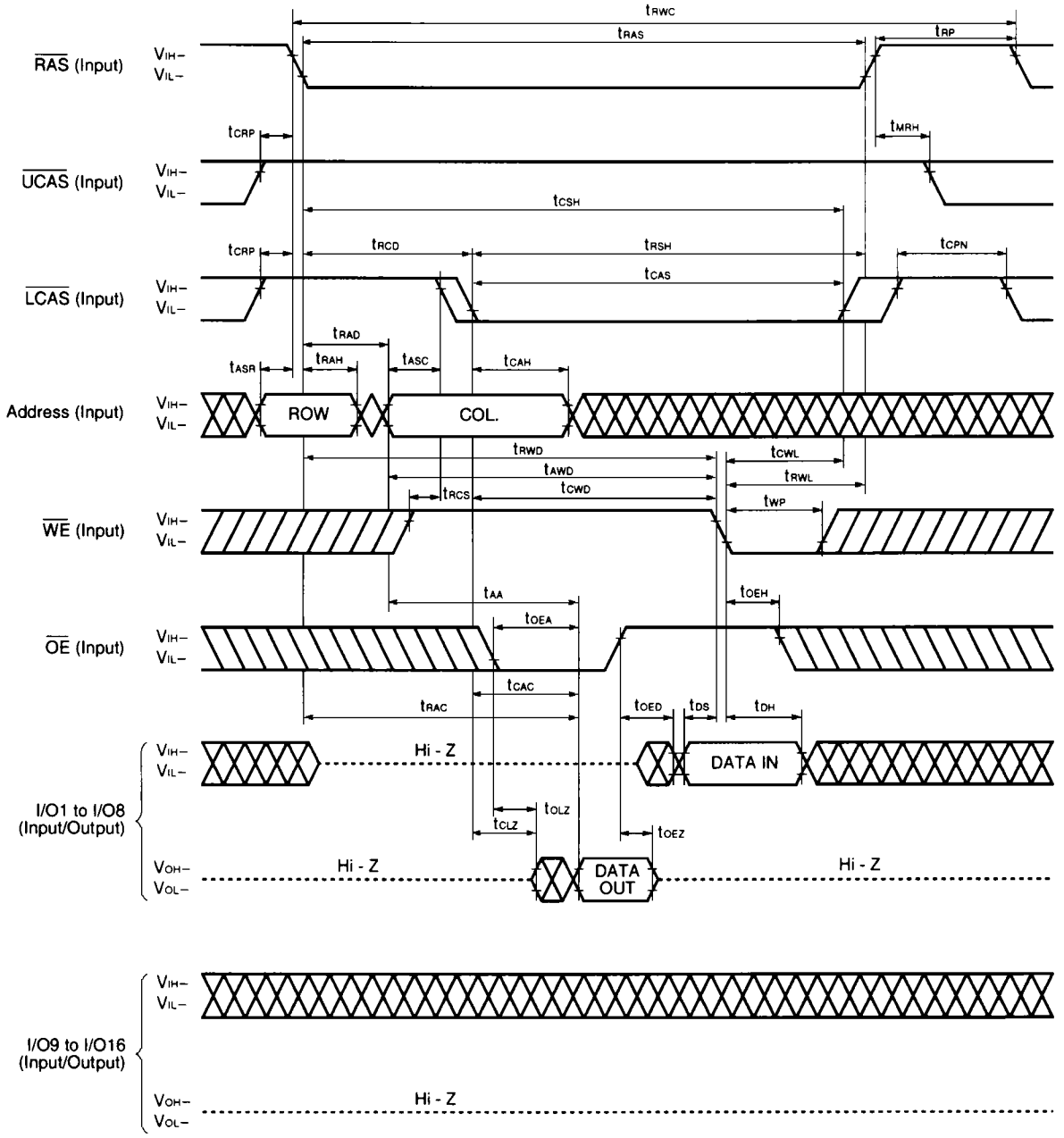
READ MODIFY WRITE CYCLE ★



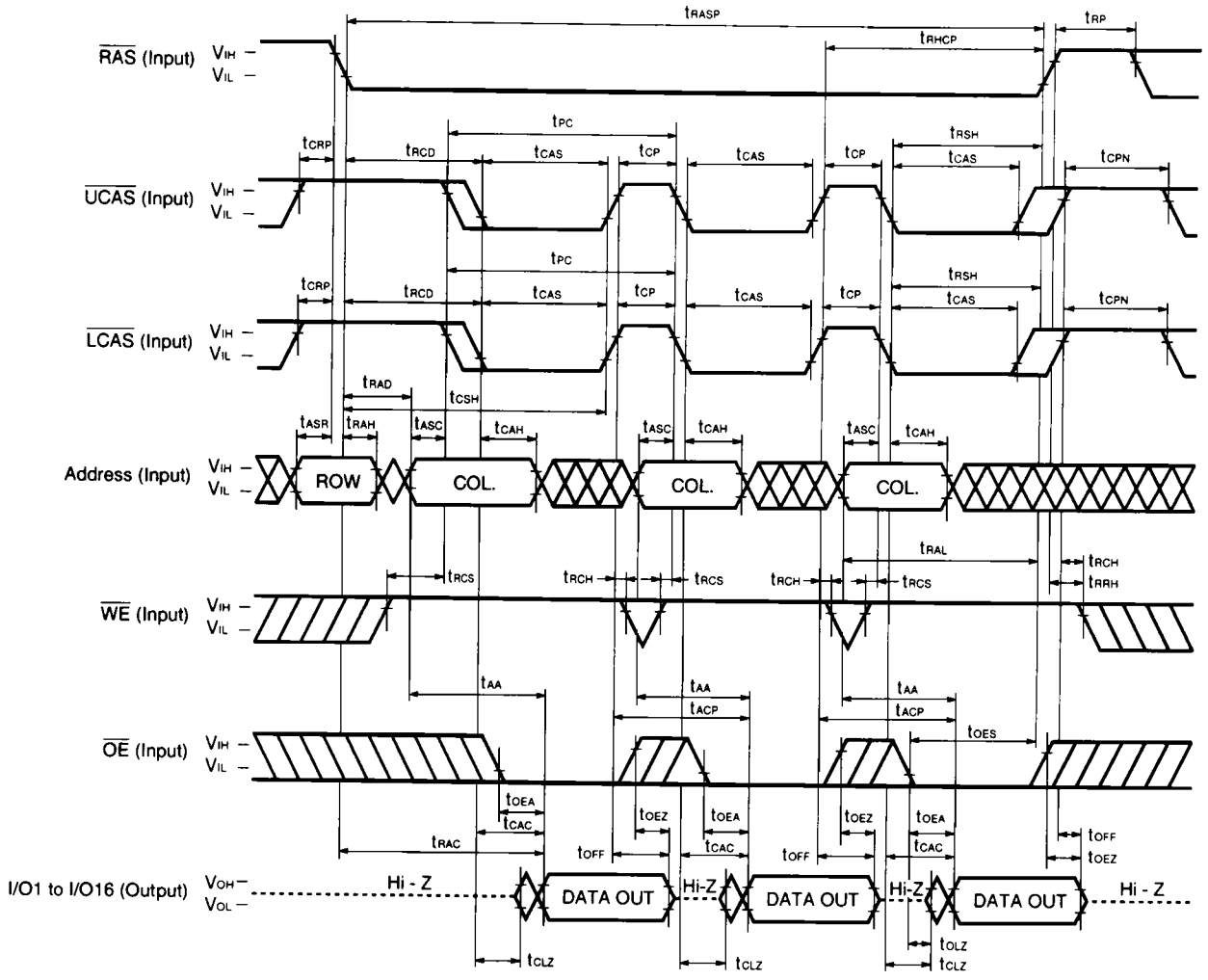
★ UPPER BYTE READ MODIFY WRITE CYCLE



LOWER BYTE READ MODIFY WRITE CYCLE ★

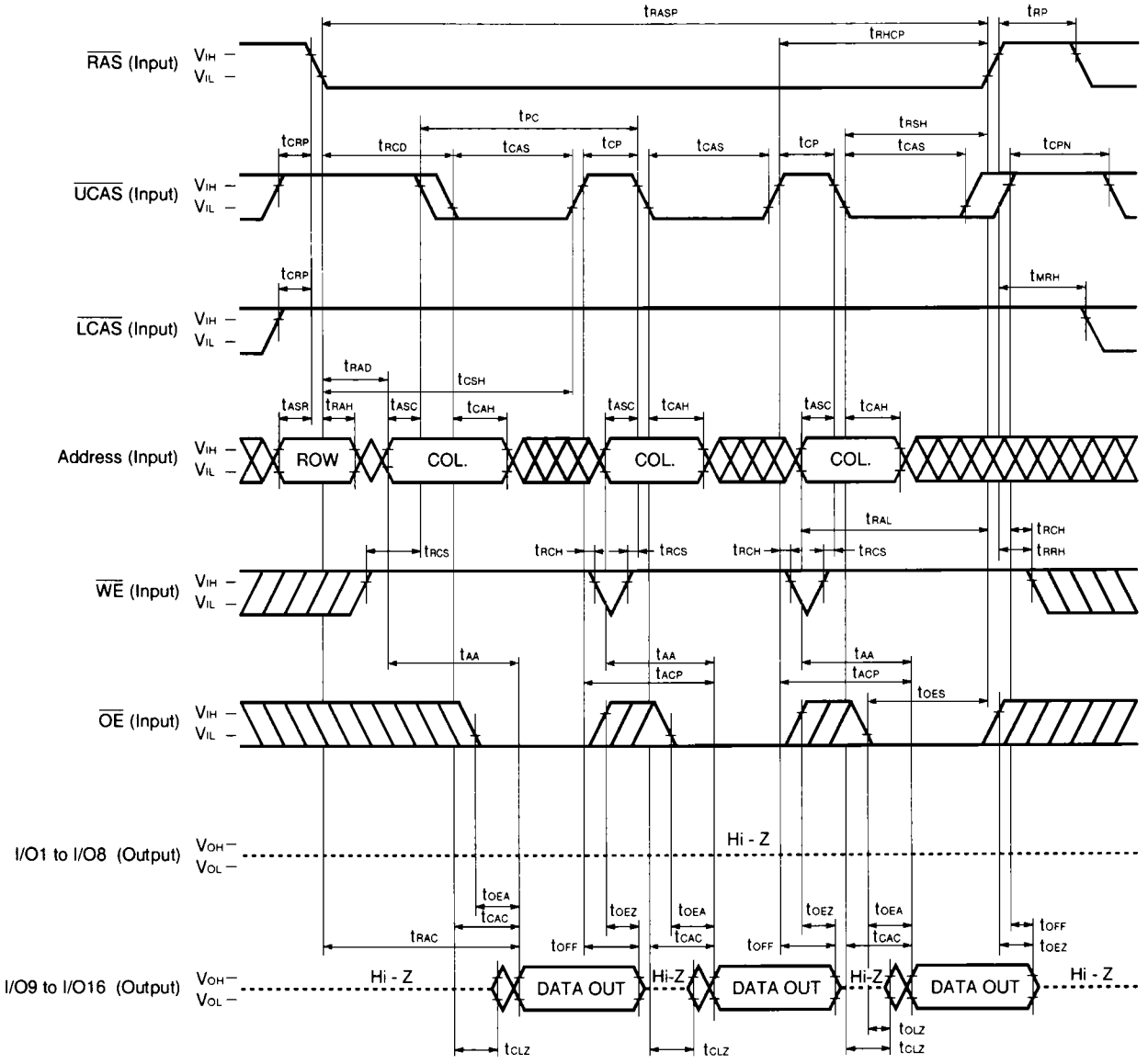


FAST PAGE MODE READ CYCLE



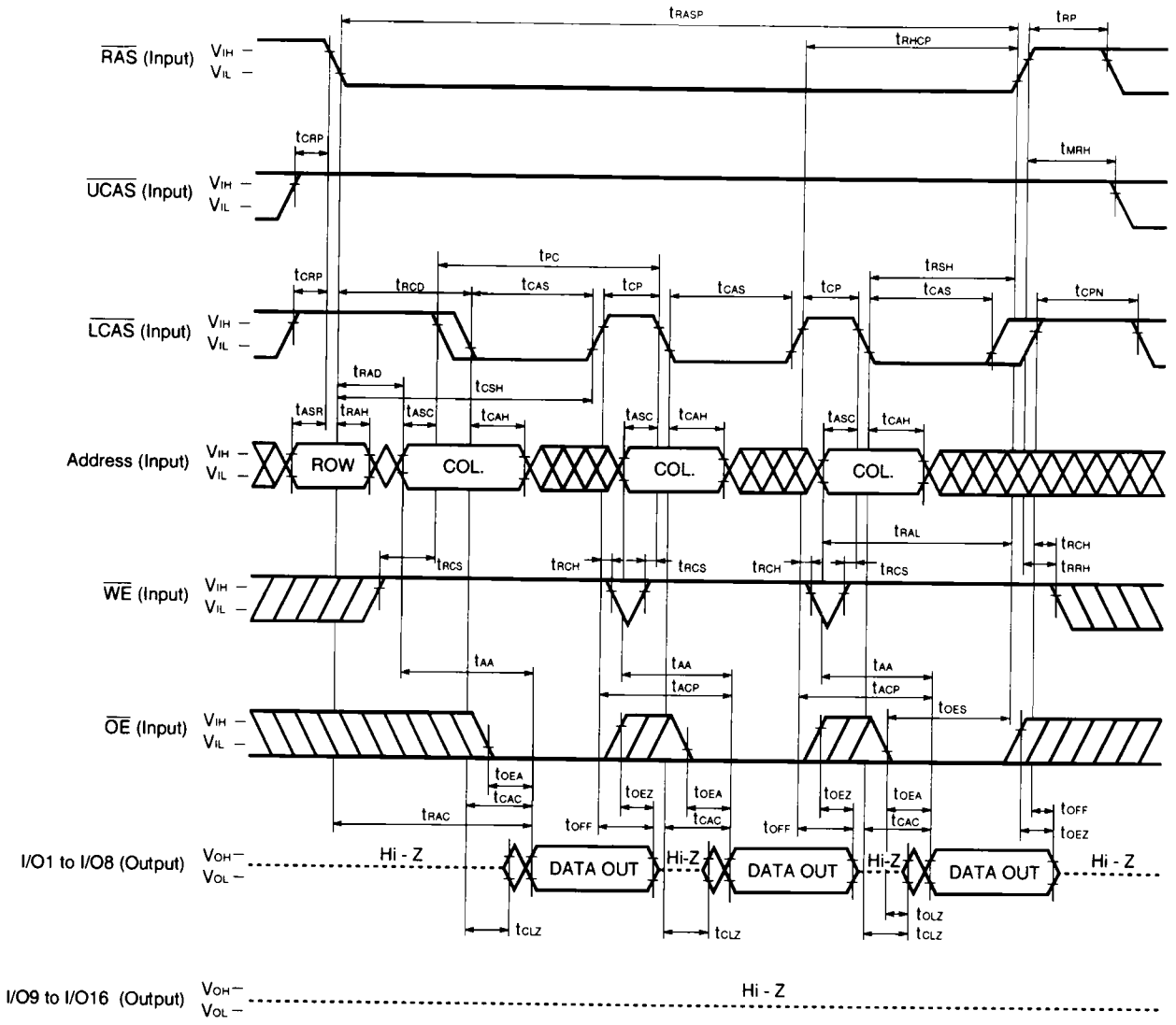
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ CYCLE



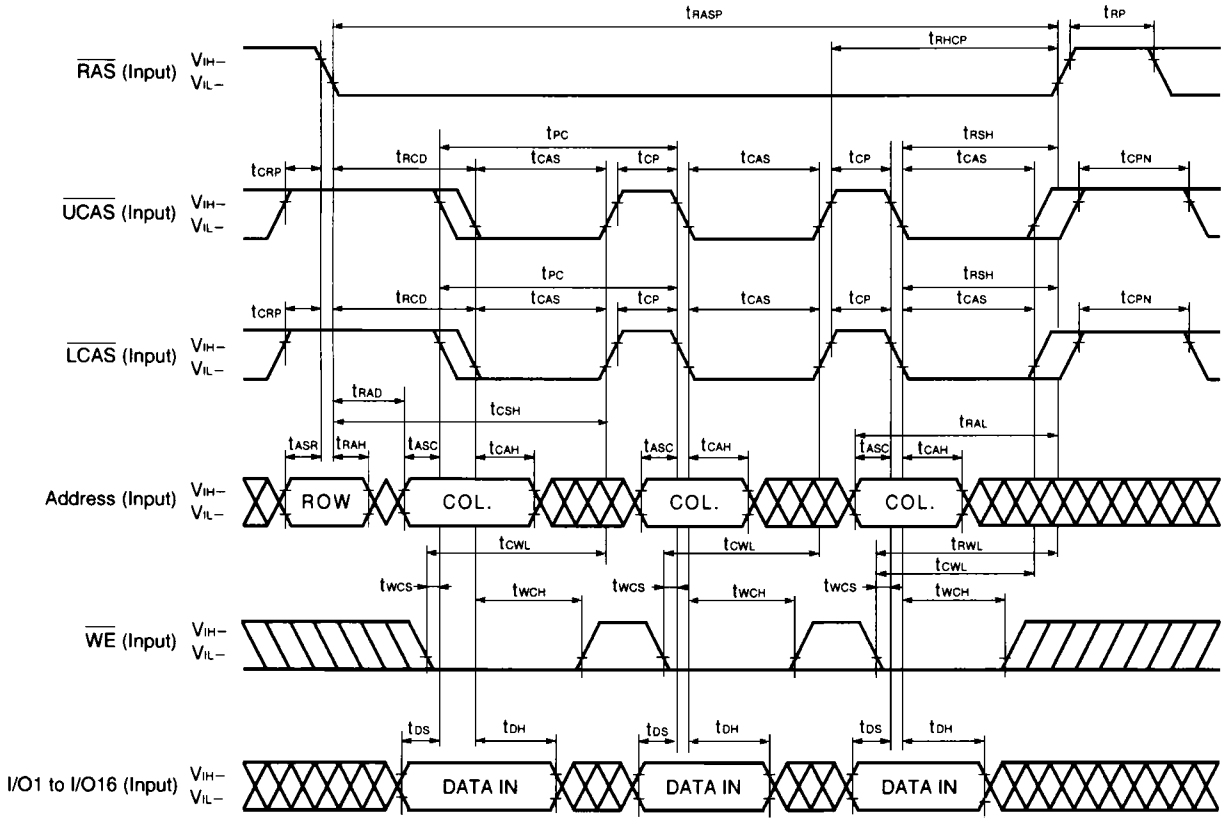
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LOWER BYTE READ CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

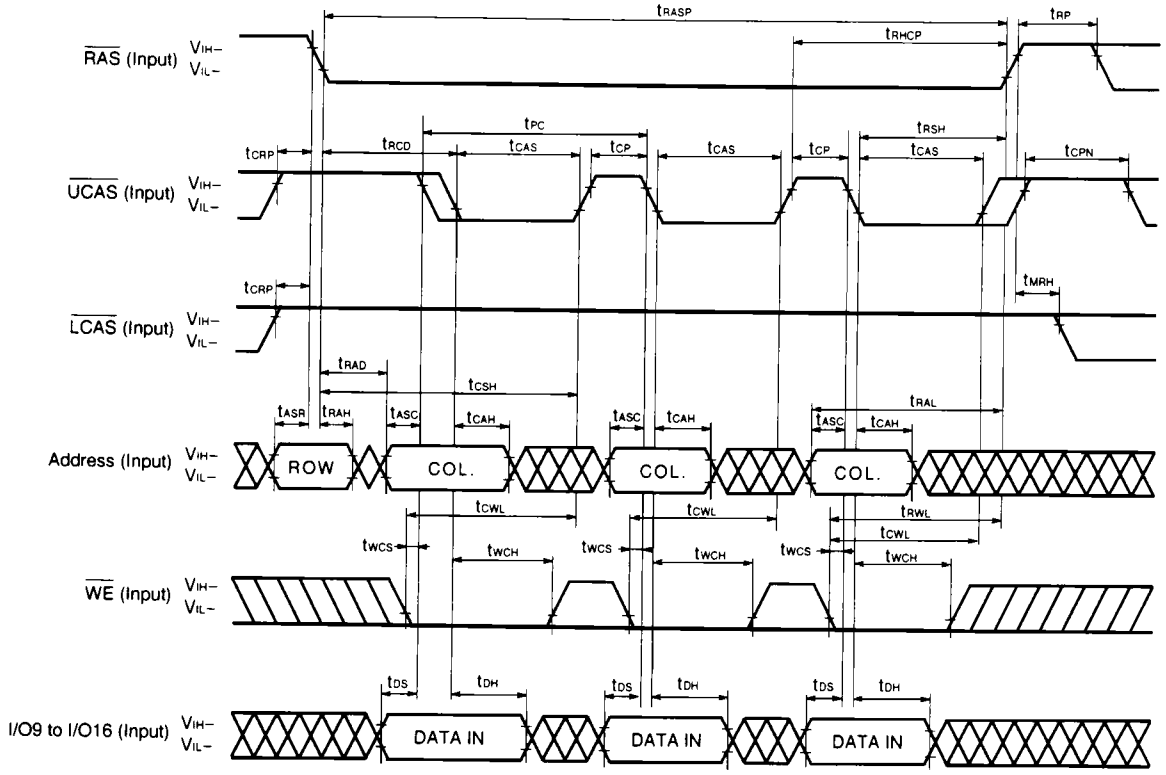
FAST PAGE MODE EARLY WRITE CYCLE



Remark $\overline{OE}$ = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

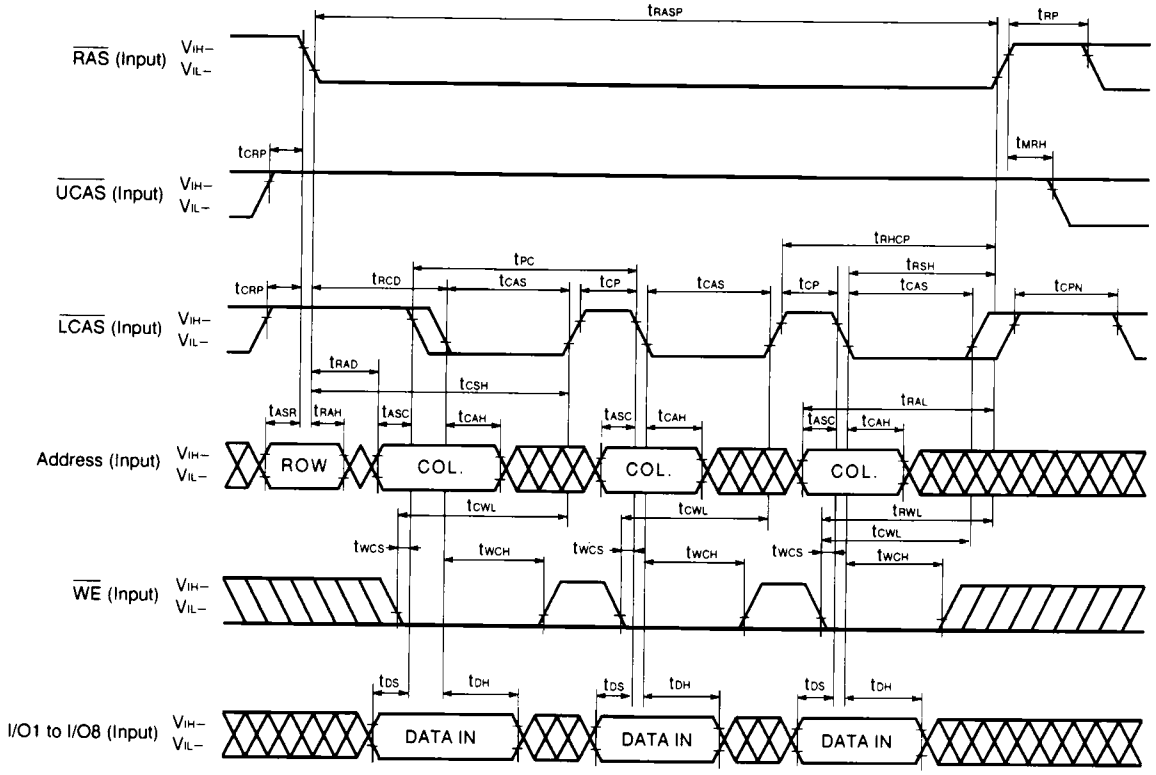
FAST PAGE MODE UPPER BYTE EARLY WRITE CYCLE



Remark I/O1 to I/O8, $\overline{OE}$ = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

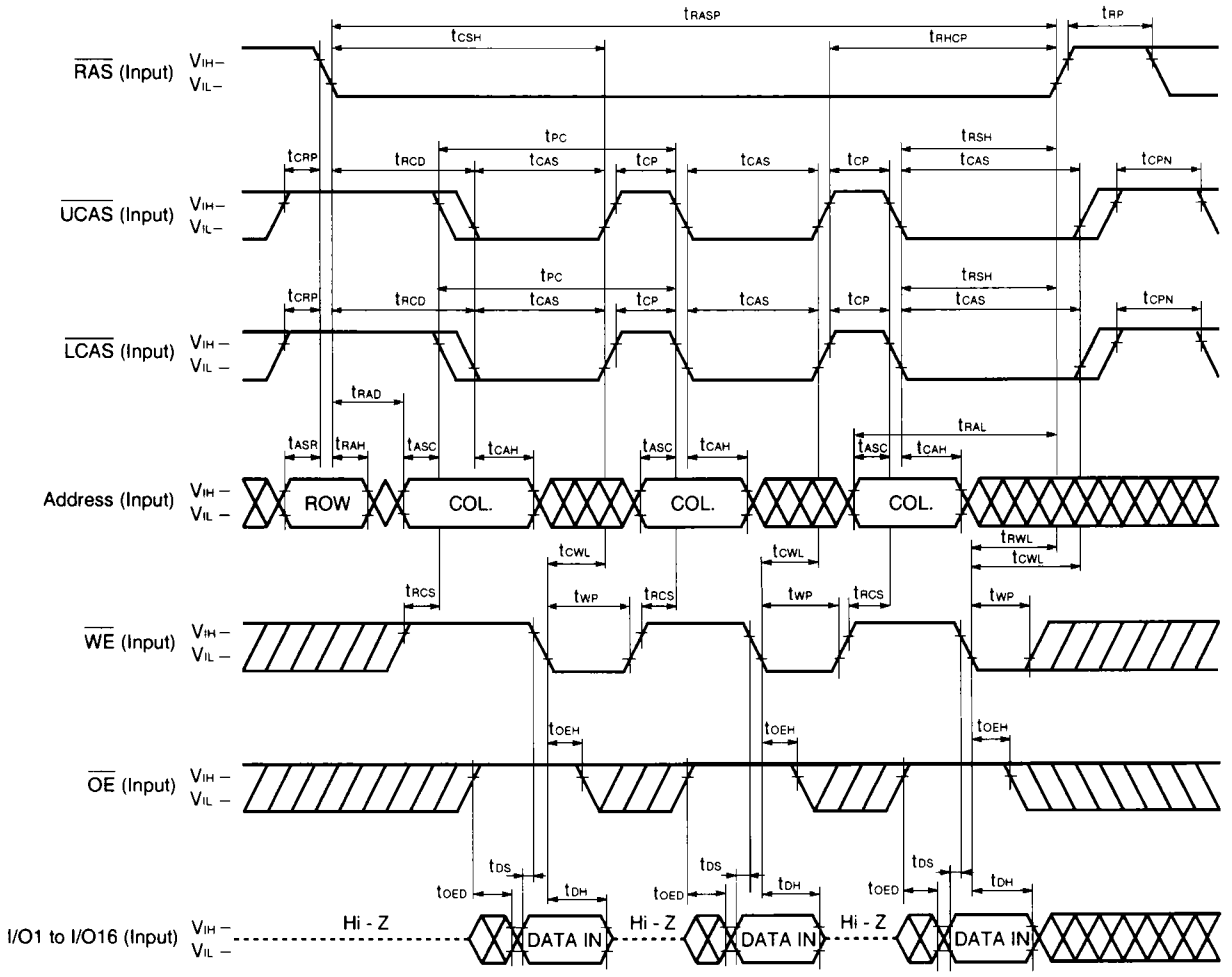
FAST PAGE MODE LOWER BYTE EARLY WRITE CYCLE



Remark I/O9 to I/O16, $\overline{OE}$ = Don't care

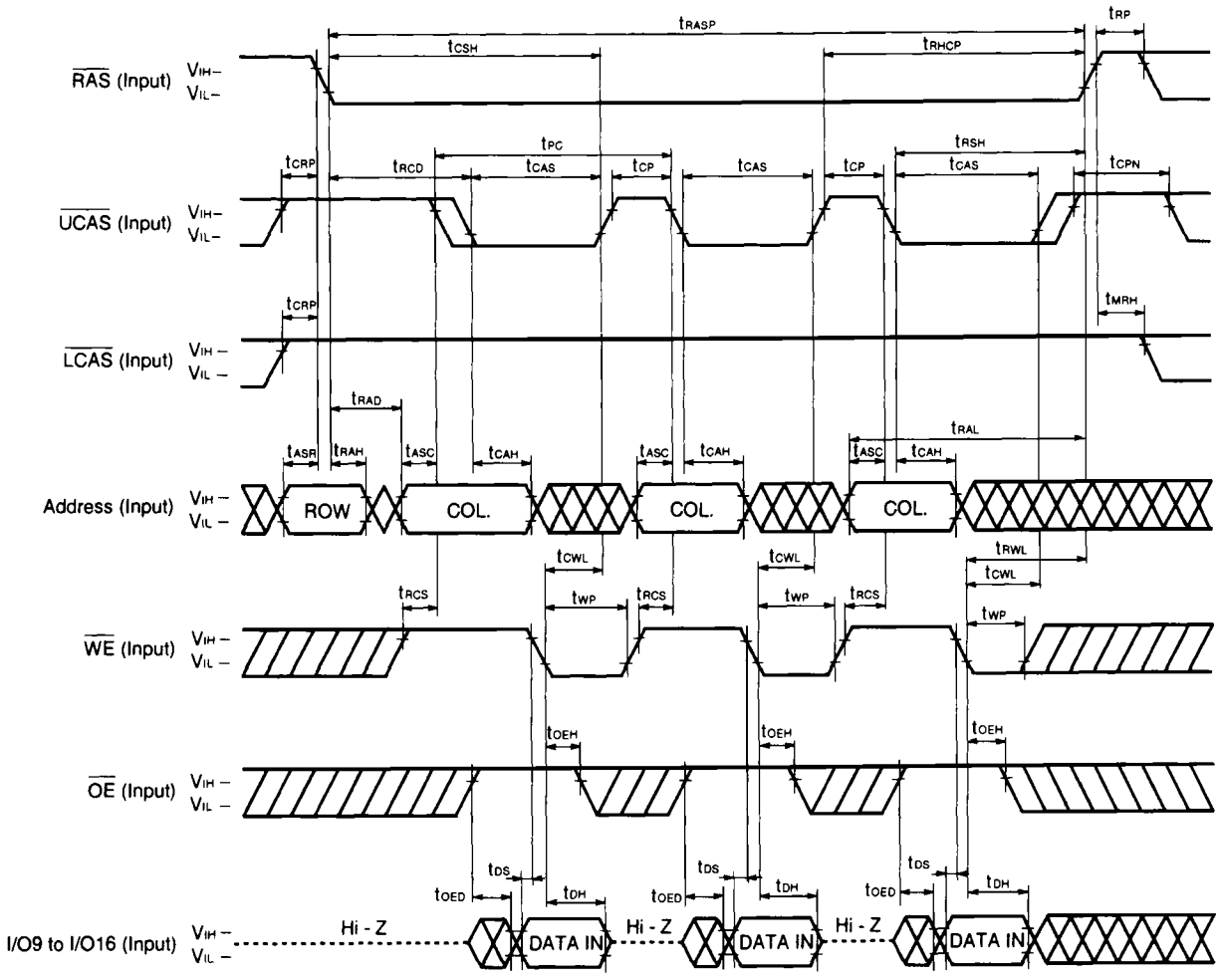
In the fast page mode, read. write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE LATE WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

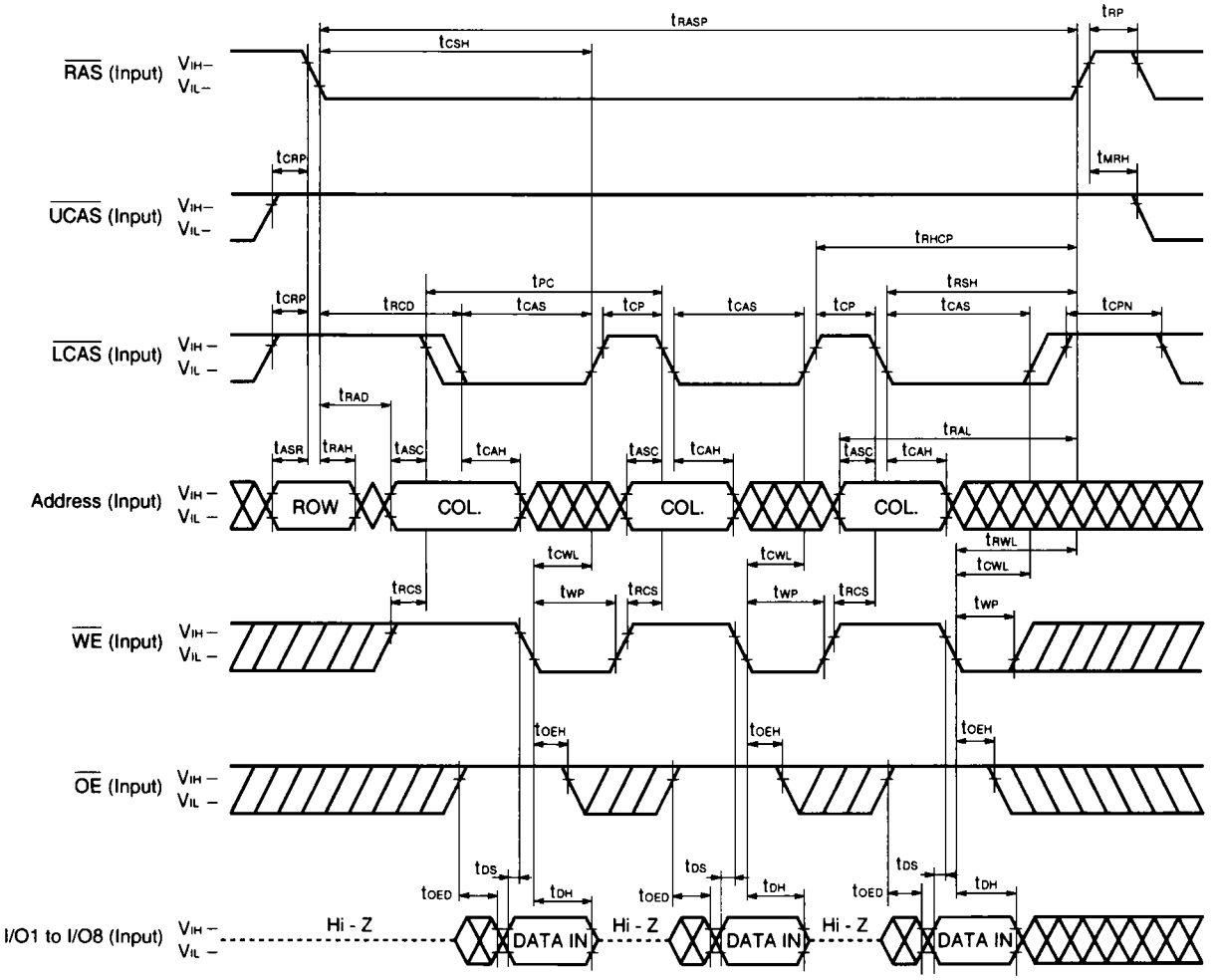
FAST PAGE MODE UPPER BYTE LATE WRITE CYCLE



Remark I/O1 to I/O8 = Don't care

In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

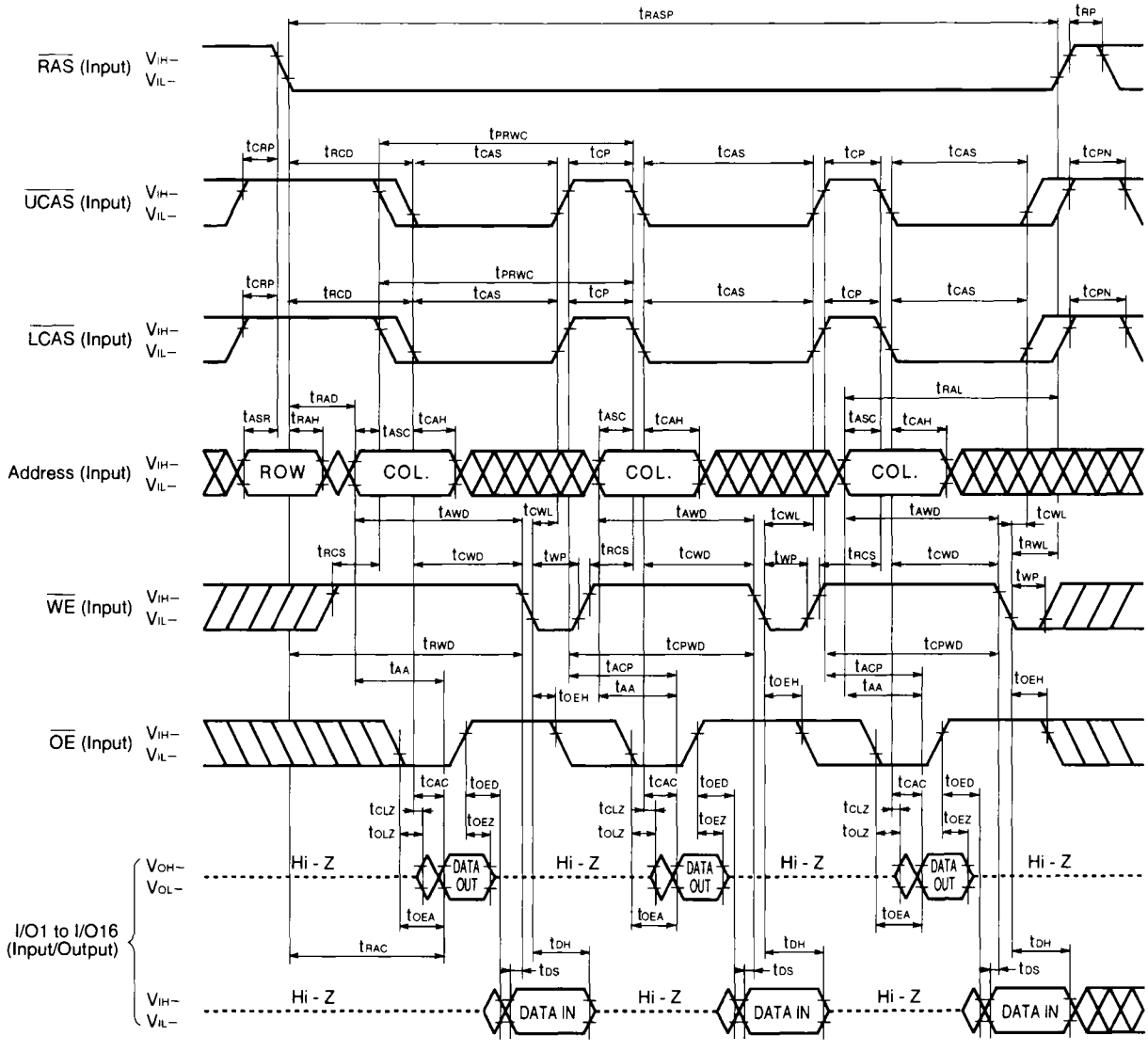
FAST PAGE MODE LOWER BYTE LATE WRITE CYCLE



Remark I/O9 to I/O16 = Don't care

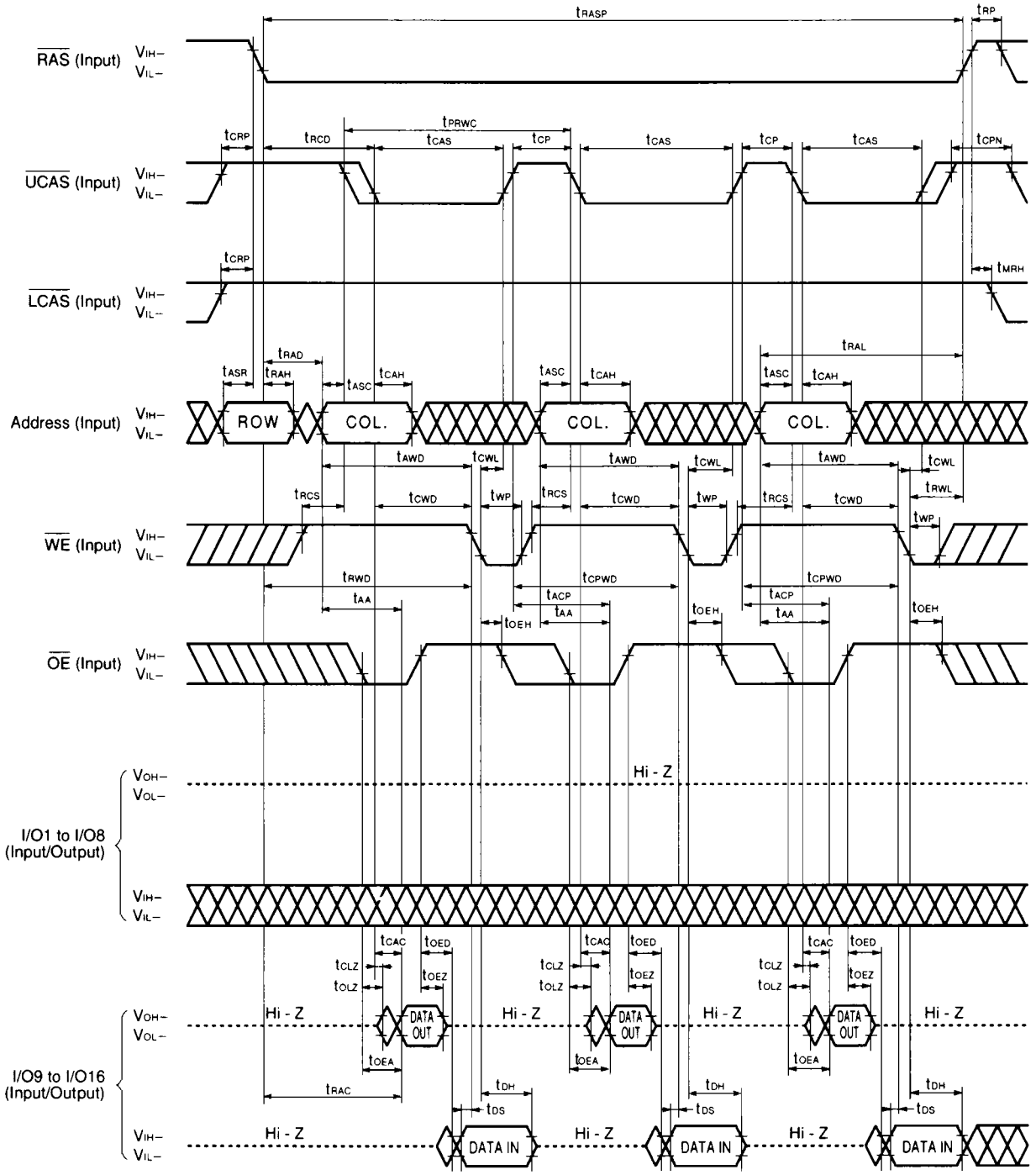
In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★ FAST PAGE MODE READ MODIFY WRITE CYCLE



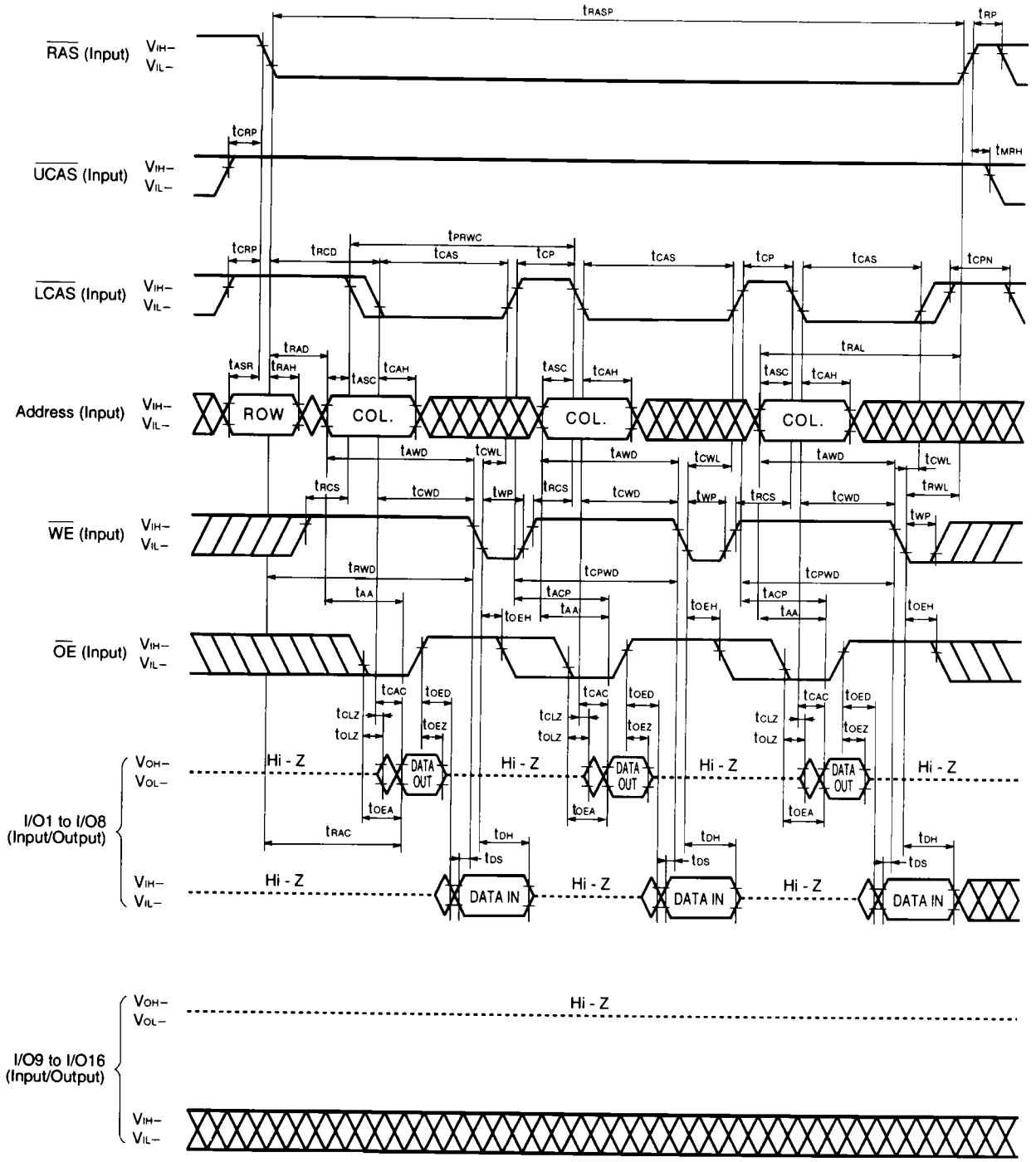
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE UPPER BYTE READ MODIFY WRITE CYCLE ★



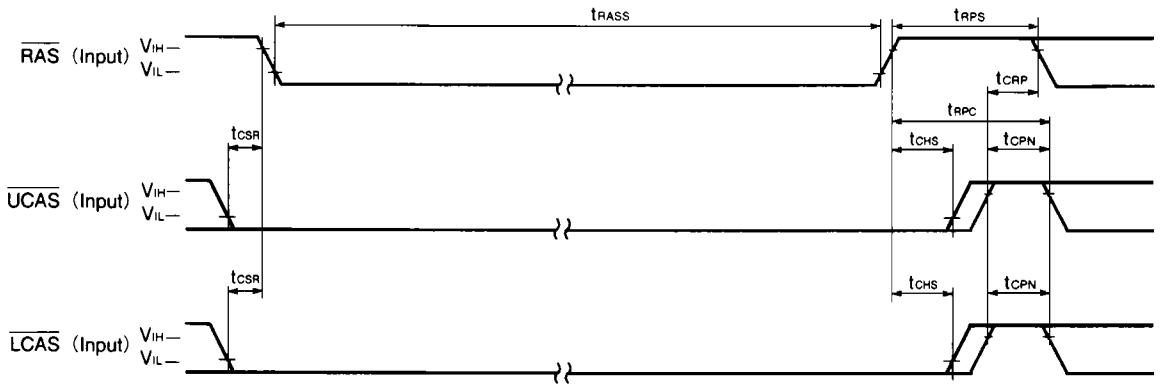
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★ FAST PAGE MODE LOWER BYTE READ MODIFY WRITE CYCLE



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ BEFORE $\overline{RAS}$ SELF REFRESH CYCLE (Only for the μPD42S16160L, 42S18160L)



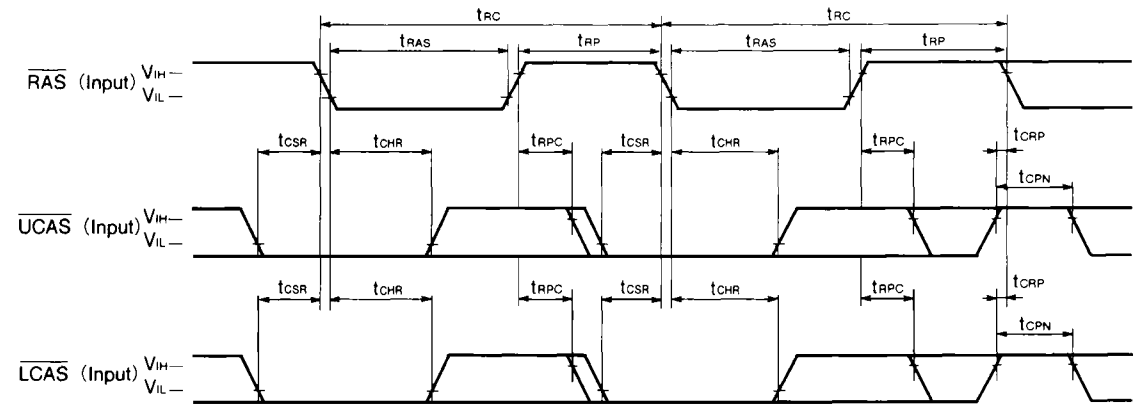
Remark Address, $\overline{WE}$, $\overline{OE}$ = Don't care I/O1 to I/O16 = Hi - Z

How to use $\overline{CAS}$ before $\overline{RAS}$ self refresh mode

$\overline{CAS}$ before $\overline{RAS}$ self refresh mode can't be used by itself. It must be used with performing one of 3 refreshes below.

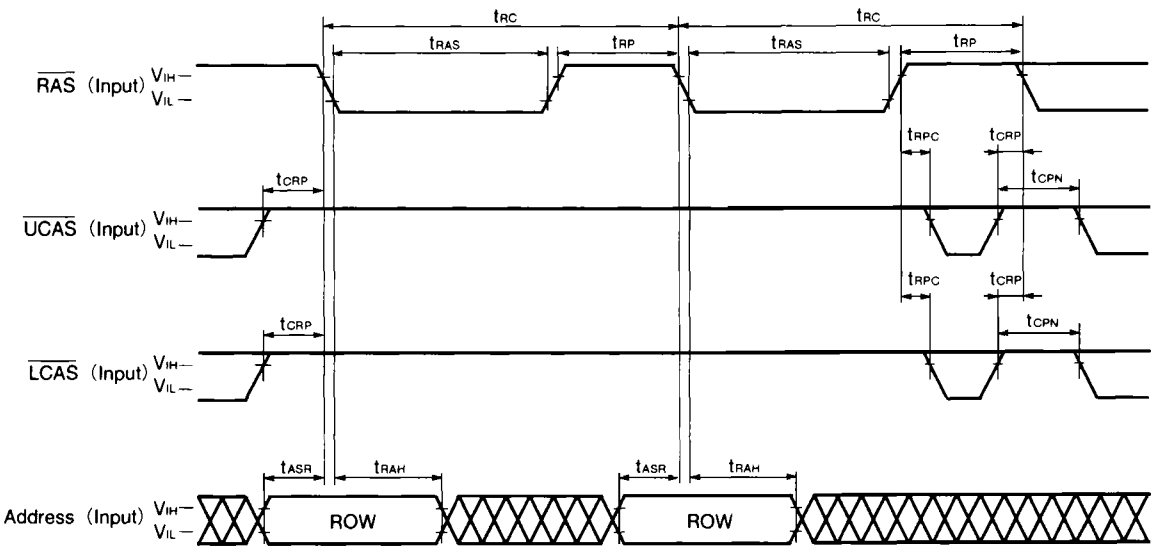
- **When using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh** ★
  Refresh 4 096 times (μPD42S16160L) or 1 024 times (μPD42S18160L) during 128 ms before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.
- **When using burst $\overline{CAS}$ before $\overline{RAS}$ refresh**
  Refresh 4 096 times during 64 ms (μPD42S16160L) or 1 024 times during 16 ms (μPD42S18160L) before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.
- **When using $\overline{RAS}$ only refresh**
  Refresh all refresh addresses during 64 ms (μPD42S16160L) or 16 ms (μPD42S18160L) before set into the $\overline{CAS}$ before $\overline{RAS}$ self refresh mode and after reset.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



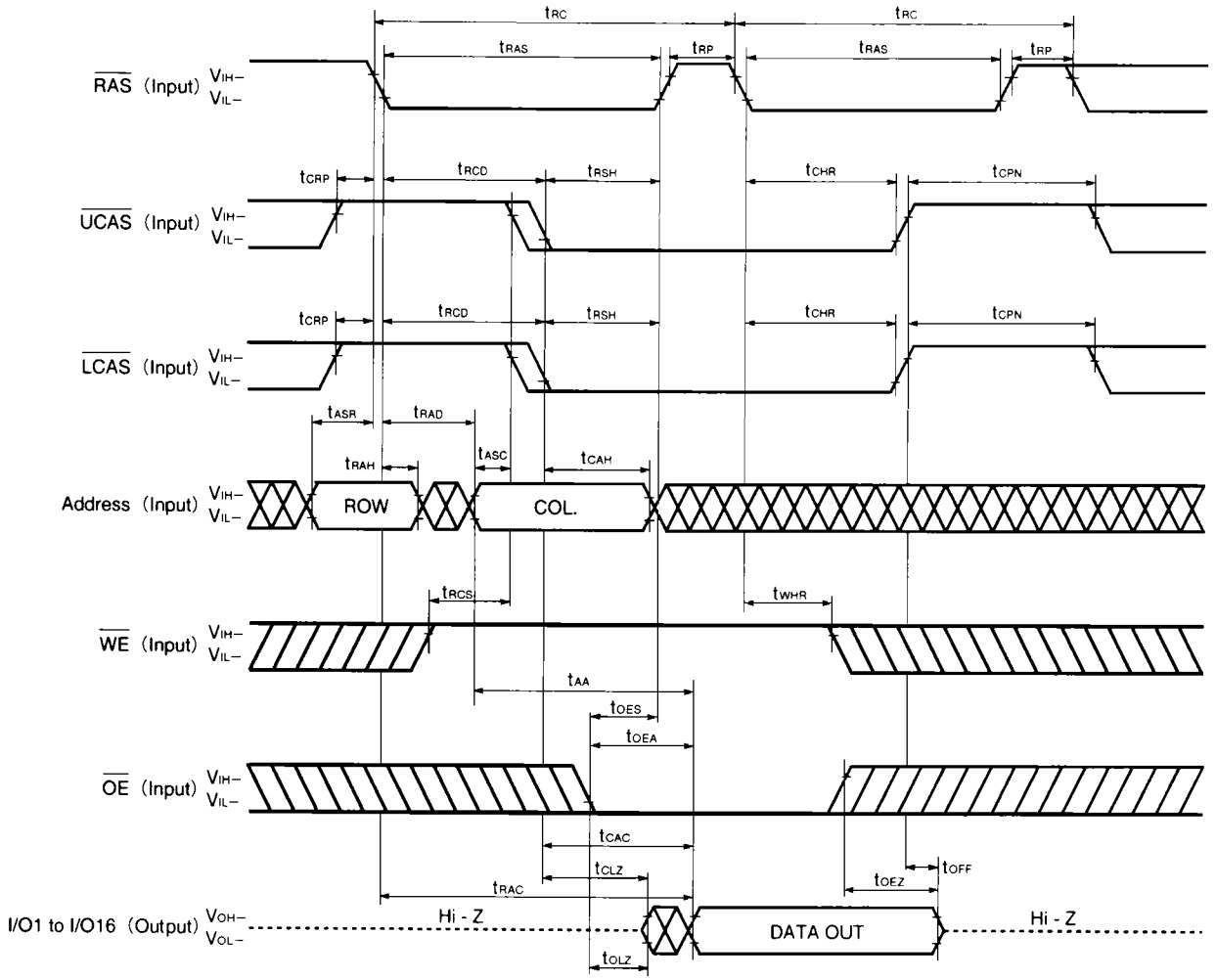
Remark Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O1 to I/O16 = Hi - Z

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

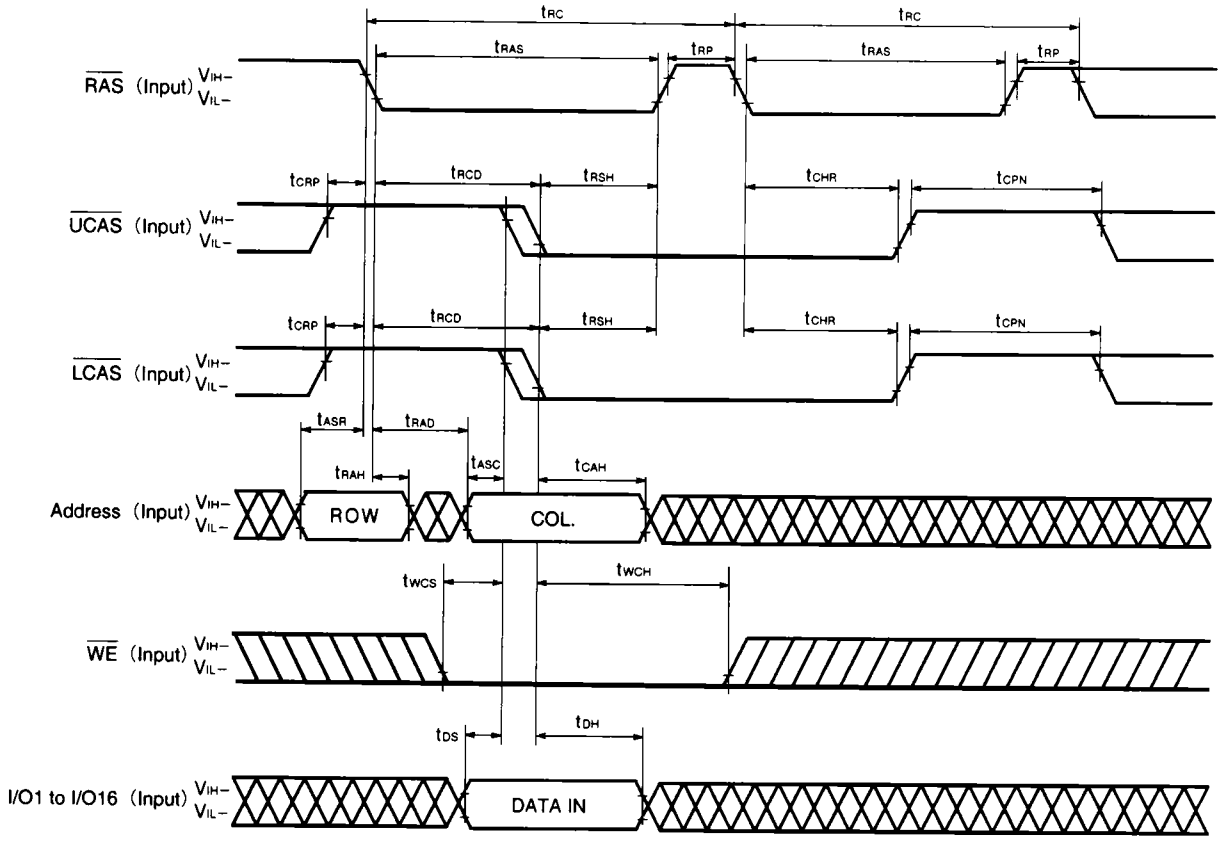


Remark $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care I/O1 to I/O16 = Hi - Z

HIDDEN REFRESH CYCLE (READ) ★

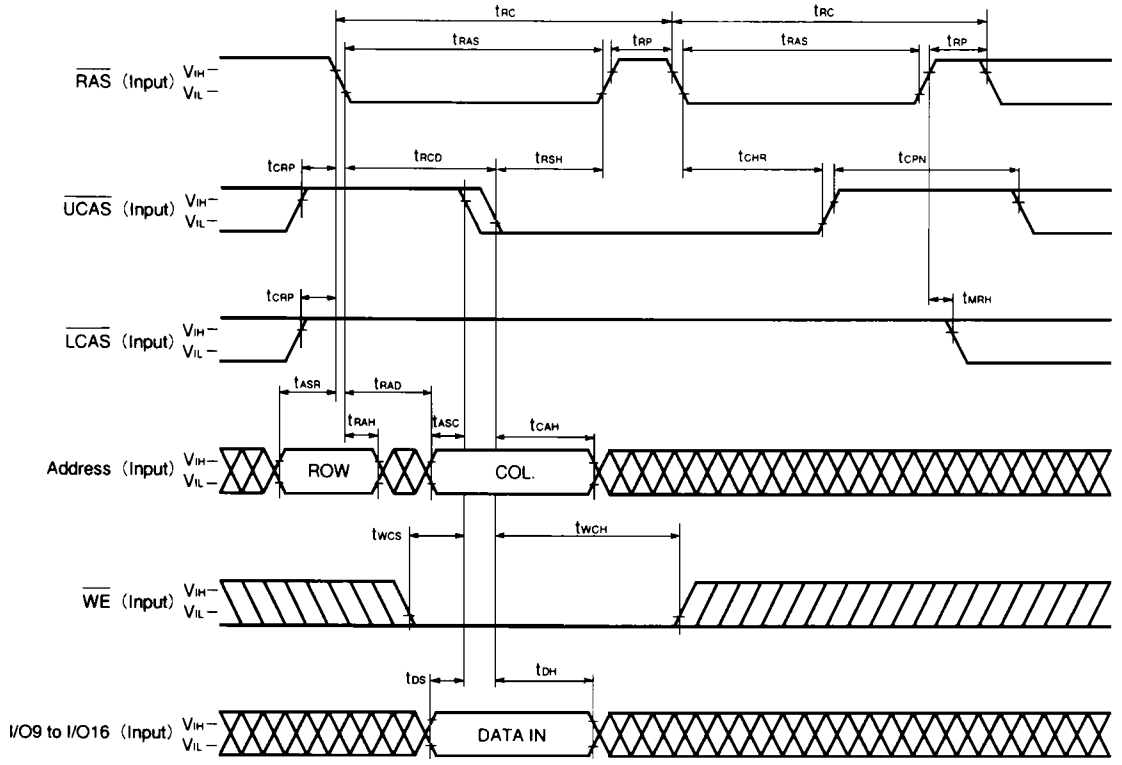


HIDDEN REFRESH CYCLE (WRITE)



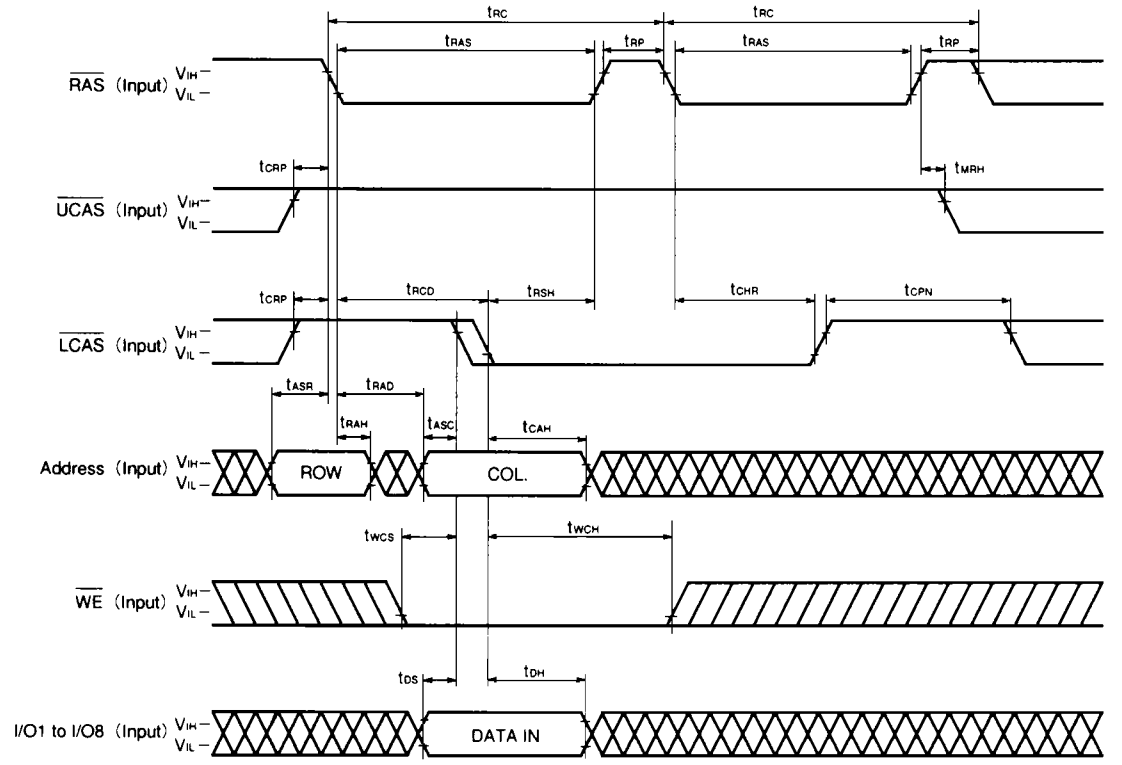
Remark $\overline{OE}$ = Don't care

HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Remark $\overline{OE}$, I/O1 to I/O8 = Don't care

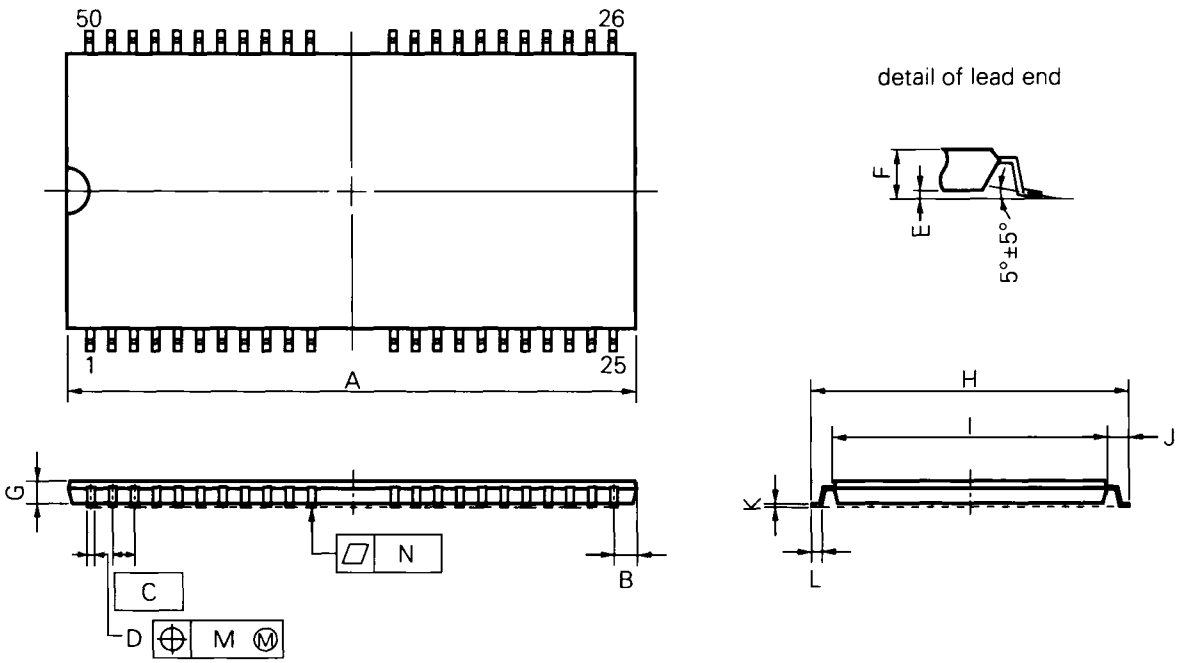
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



Remark $\overline{OE}$, I/O9 to I/O16 = Don't care

PACKAGE DRAWINGS

★ 50 PIN PLASTIC TSOP(III) (400 mil)



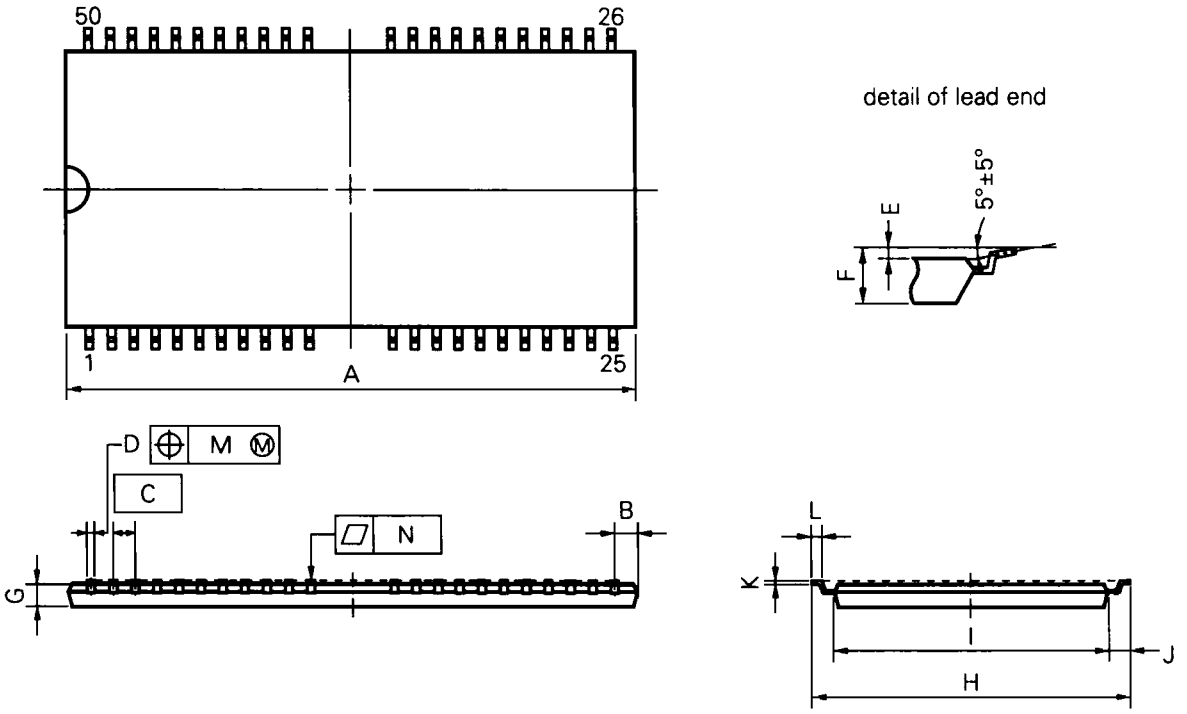
S50G5-80-7JF-1

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004

50 PIN PLASTIC TSOP(III) (400 mil) ★



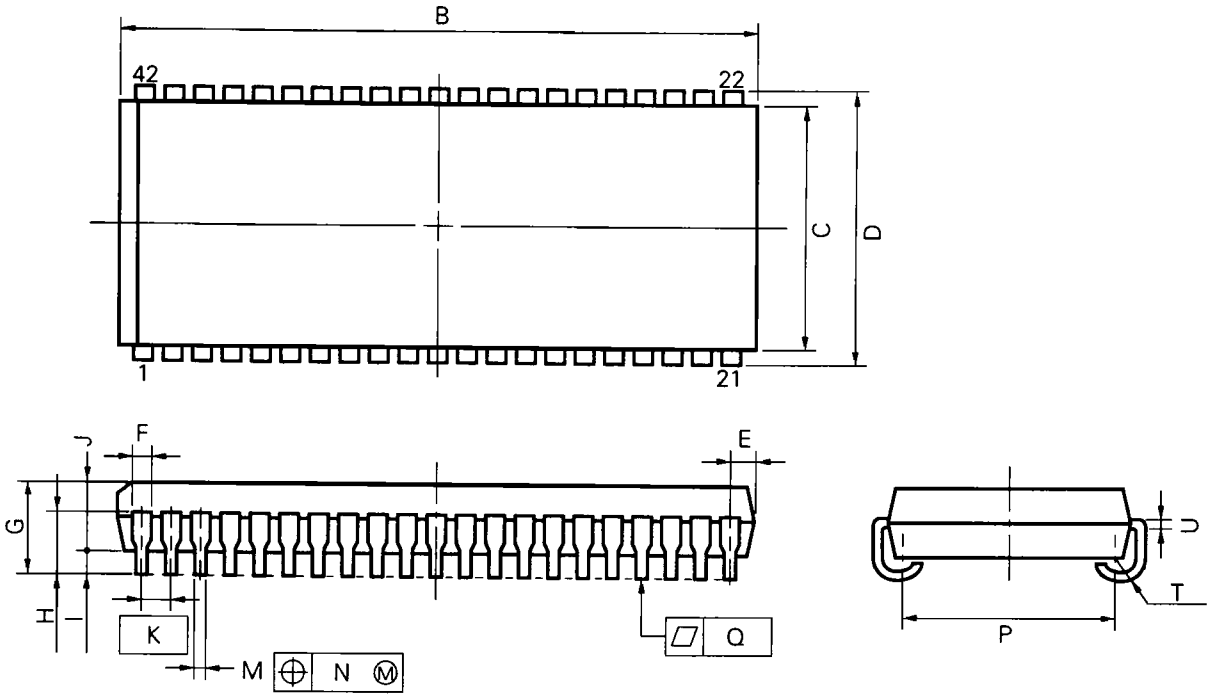
S50G5-80-7KF-1

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.45 MAX.	0.845 MAX.
B	1.13 MAX.	0.045 MAX.
C	0.8 (T.P.)	0.031 (T.P.)
D	0.30 ± 0.10	$0.012^{+0.004}_{-0.005}$
E	0.05 ± 0.05	0.002 ± 0.002
F	1.1 MAX.	0.044 MAX.
G	0.97	0.038
H	11.76 ± 0.2	0.463 ± 0.008
I	10.16 ± 0.1	0.400 ± 0.004
J	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	0.5 ± 0.1	$0.020^{+0.004}_{-0.005}$
M	0.13	0.005
N	0.10	0.004

42 PIN PLASTIC SOJ (400 mil)



P42LE-400A

ITEM	MILLIMETERS	INCHES
B	$27.56^{+0.2}_{-0.35}$	$1.085^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.08±0.15	$0.043^{+0.006}_{-0.007}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.10	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

RECOMMENDED SOLDERING CONDITIONS

Please consult with our sales offices for soldering conditions of the μPD42S16160L, 4216160L, 42S18160L, 4218160L.

TYPE OF SURFACE MOUNT DEVICE

μPD42S16160LG5, 4216160LG5, 42S18160LG5, 4218160LG5 : 50-pin Plastic TSOP (II) (400 mil)
μPD42S16160LLE, 4216160LLE, 42S18160LLE, 4218160LLE : 42-pin Plastic SOJ (400 mil)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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