Revision Date: May 5, 1997

AP9A403A

2048 x 9 Asynchronous CMOS FIFO

Features

- Fast access times: 15, 20, 25, 35 ns
- Fast-fall-through time architecture based on CMOS dual-port SRAM technology
- Independent timing on input and output port
- Expandable-in width and depth
- Full, half-full and empty status flags
- Data retransmit capability
- TTL-compatible I/O
- Control signals assertive-LOW for noise immunity
- 28-pin, 300-Mil DIP and 32-pin PLCC package
- Functionally compatible with the IDT7203

Functional Description

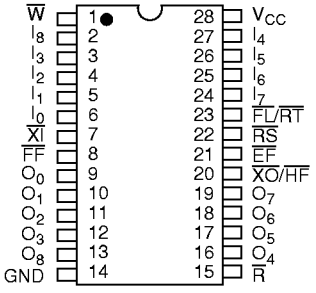
The AP9A403A is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 2048 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit AP9A403A word may consist of a standard eight-bit byte with a parity bit or block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the AP9A403A becomes either totally full (or totally empty). Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-full and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full AP9A403A or by attempting to read additional words from an already-empty AP9A403A. When an AP9A403A is operating in a depth-expansion configuration, the Half-Full flag is not available.

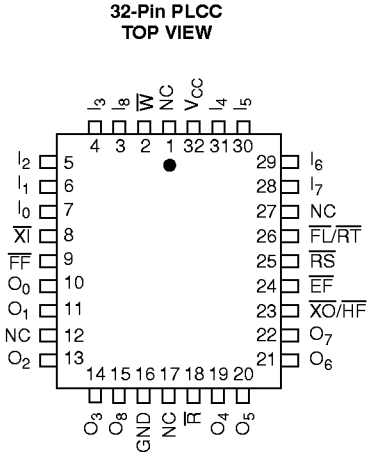
Pin Configurations

28-Pin DIP
TOP VIEW



9A403A-1

32-Pin PLCC
TOP VIEW



9A403A-2

Selection Guide

	AP9A403A-15	AP9A403A-20	AP9A403A-25	AP9A403A-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)	100	100	100	100
Maximum Standby Current (mA)	15	15	15	15

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Functional Description (continued)

Data words are read out from the AP9A403A's output port in precisely the same order that they were written in at its input port; that is, according to a First-in, First-out queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the AP9A403A device.

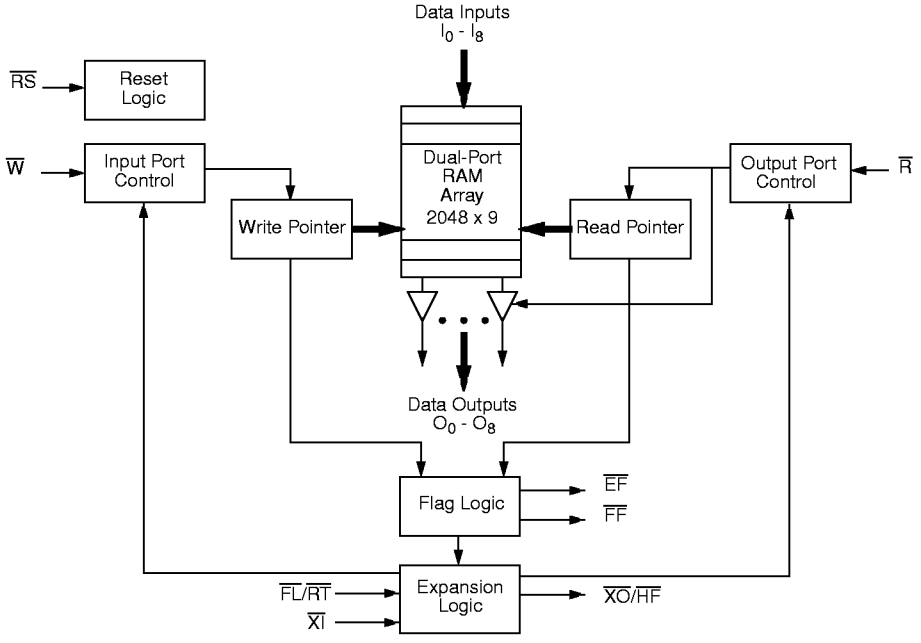
Drop-in replacement compatibility is maintained with both larger and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO memory array read-address pointer to be set back to zero (to point to the AP9A403A's first physical memory location) without affecting the internal FIFO memory array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address pointer value, may be read out repeatedly for an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an AP9A403A is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the AP9A403A to an initial state, empty and ready to be filled. An AP9A403A should be reset during every system power-up sequence. A reset operation causes the internal FIFO memory array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the AP9A403A's first physical memory location. Any information that previously had been stored within the AP9A403A is not recoverable after a reset operation.

A depth expansion scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}$/$\overline{HF}$) output signal. This allows a deeper 'effective FIFO' to be implemented by using two or more AP9A403A devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this expansion operating mode, one AP9A403A device must be designated as the 'first load' or 'master' device, by grounding its First-Load ($\overline{FL}$/$\overline{RT}$) control input; the remaining AP9A403A devices are designated as 'slaves' by tying their $\overline{FL}$/$\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' AP9A403A devices operating in Expansion mode.

Block Diagram



9A403A-3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -65°C to +150°C
V_{CC} Supply Relative to GND .....-0.5 V to +7 V
Short Circuit Output Current[1] .....±50mA
Voltage on any Pin Relative to GND [2, 3]...-0.5 to V_{CC} +0.5 V
DC Voltage Applied to Outputs
in High-Z State [3] ..... -0.5 to V_{CC} +0.5 V
Power Dissipation ..... 1.0 W

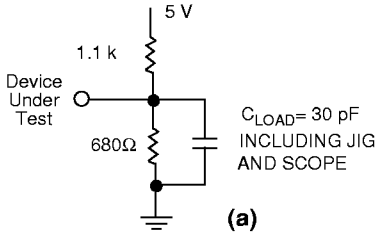
Electrical Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, V_{CC} = 5V ±10%)

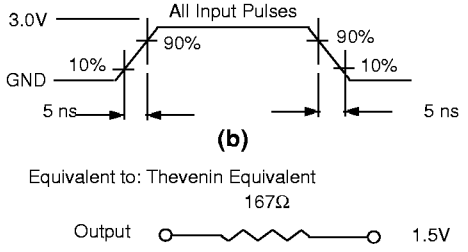
Symbol	Parameter	Test Conditions	9A403A-15		9A403A-20		9A403A-25		9A403A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{CC}	Supply Current[4]	Measured at f = 40 MHz		100		100		100		100	mA
I_{CC2}	Standby Current[4]	All Inputs = V_{IH}		15		15		15		15	mA
I_{CC3}	Power Down Current[4]	All Inputs = V_{CC} -0.2 V		5		5		5		5	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	-10	10	-10	10	-10	10	-10	10	A
I_{LO}	Output Leakage Current	$\overline{R} \ge V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	-10	10	-10	10	-10	10	-10	10	A
V_{OH}	Output High Voltage	I_{OH} = -2.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input High Voltage		2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V

Capacitance[5, 6]

Symbol	Description	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	I/O Capacitance	7	pF

AC Test Loads and Waveforms





Notes:

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Not to exceed +7 V.
4. I_{CC}, I_{CC2} and I_{CC3} are dependent upon output loading and cycle rates. Specified values are with outputs open.
5. Sample tested only
6. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{IN} = 0 V.

Switching Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$)[7]

Parameter	Description	9A403A-15		9A403A-20		9A403A-25		9A403A-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_A	Access Time		15		20		25		35	ns
t_{RR}	Read Recover Time	10		10		10		10		ns
t_{RPW}	Read Pulse Width[8]	15		20		25		35		ns
t_{RLZ}	Data Bus Active from Read LOW[9]	5		5		5		5		ns
t_{WLZ}	Data Bus Active from Write HIGH[9, 10]	10		10		10		10		ns
t_{DV}	Data Valid from Read Pulse HIGH	5		5		5		5		ns
t_{RHZ}	Data Bus High-Z from Read HIGH[9]		15		15		15		15	ns
Write Cycle										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{WPW}	Write Pulse Width[8]	15		20		25		35		ns
t_{WR}	Write Recovery Time	10		10		10		10		ns
t_{SD}	Data Set-up Time	10		10		10		15		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
Reset Timing										
t_{RSC}	Reset Cycle Time	25		30		35		45		ns
t_{RS}	Reset Pulse Width	15		20		25		35		ns
t_{RSR}	Reset Recovery Time	10		10		10		10		ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15		20		25		35		ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15		20		25		35		
Retransmit Timing										
t_{RTC}	Retransmit Cycle Time	25		30		35		45		ns
t_{RT}	Retransmit Pulse Width[8]	15		20		25		35		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		ns
Flag Timing										
t_{EFL}	Reset LOW to Empty Flag LOW		25		30		35		45	ns
$t_{HFH, FFH}$	Reset LOW to Half-Full and Full Flags HIGH		25		30		35		45	ns
t_{REF}	Read LOW to Empty Flag LOW		15		20		25		35	ns
t_{RFF}	Read HIGH to Full Flag HIGH		15		20		25		35	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		15		20		25		35	ns
t_{WFF}	Write LOW to Full Flag LOW		15		20		25		35	ns
t_{WHF}	Write LOW to Half-Full Flag LOW		15		20		25		35	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH		15		20		25		35	ns
Expansion Timing										
t_{XOL}	Expansion Out LOW		18		20		25		35	ns
t_{XOH}	Expansion Out HIGH		18		20		25		35	ns
t_{XI}	Expansion In Pulse Width	15		20		25		35		ns
t_{XIR}	Expansion In Recovery Time	10		10		10		10		ns
t_{XIS}	Expansion In Set-up Time	7		10		10		15		ns

Notes:

7. All timing measurements performed at 'AC Test Condition levels.
8. Pulse widths less than minimum value are not allowed.
9. Guaranteed but not tested.
10. Only applies to read data flow-through mode.

Operational Description

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}/\overline{RT}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode (*Tables 1 and 2*).

A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH before the reset operation is terminated by a rising edge of $\overline{RS}$ by a time t_{RRSS} (for Read) or t_{WRSS} (for Write), respectively.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data set-up and hold times must be observed on the data in (I_0 - I_8) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$ (*Table 3*).

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation that fills the last available location in the FIFO memory array. $\overline{FF}$=LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location (*Table 3*).

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (O_0 - O_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ that accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data (*Table 3*).

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when $\overline{W}$ is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$, which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an AP9A403A may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block that may be transmitted is 2048 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the AP9A403A is operating in Depth-expansion mode because the $\overline{FL}$/RT control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	Mode	$\overline{XO}/\overline{HF}$ Usage	$\overline{XI}$ Usage	$\overline{FL}/\overline{RT}$ Usage
H[11]	H	Expansion Slave[12]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H[11]	L	Expansion Master[12]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Stand-alone	$\overline{HF}$	(none)	$\overline{RT}$

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	Pin	Stand-alone	Expansion Master	Expansion Slave
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

Number of Unread Data Words Present Within 2048 x 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 1024	H	H	H
1025 to 2047	H	L	H
2048	L	L	H

Notes:

11. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.

12. The terms 'master' and 'slave' refer to operation in depth-expansion grouping mode.

Operational Modes

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset (*Table 1*).

Width Expansion

Word-width expansion is implemented by placing multiple AP9A403A devices in parallel. Each device should be configured for stand-alone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices (See *Figures 1, 2 and 3*).

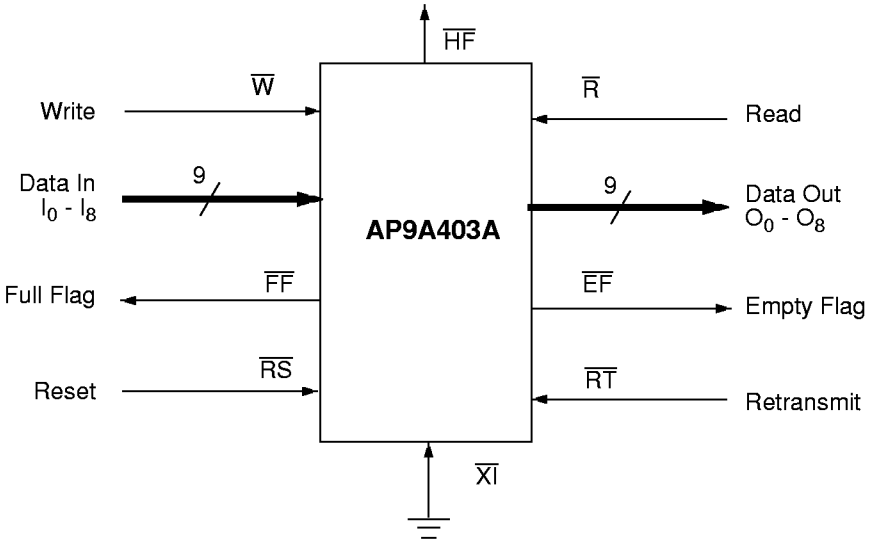


Figure 1. Single FIFO (2048 x 9)

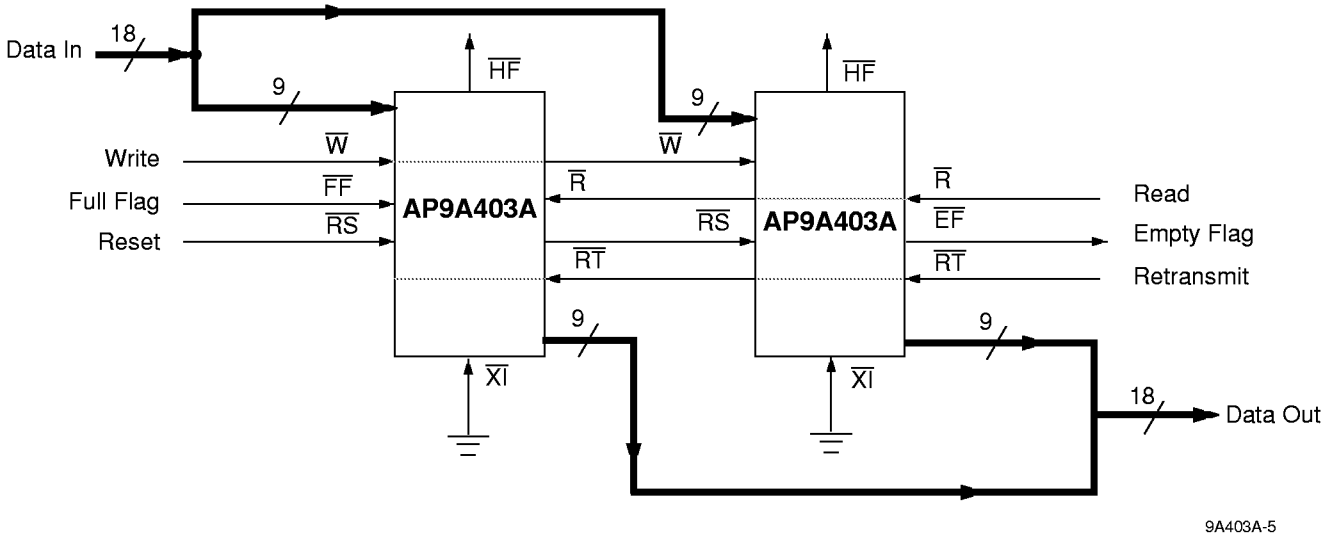


Figure 2. FIFO Width Expansion (2048 x 18)

Operational Modes (continued)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$/RT) of this device to ground. All other devices must have their $\overline{FL}$/RT pin tied to a high level. In this mode, $\overline{W}$, and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given write cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, only one FIFO is enabled during any given read cycle. The common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag, by ANDing the $\overline{FF}$ outputs of all AP9A403A devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in Depth-expansion mode.

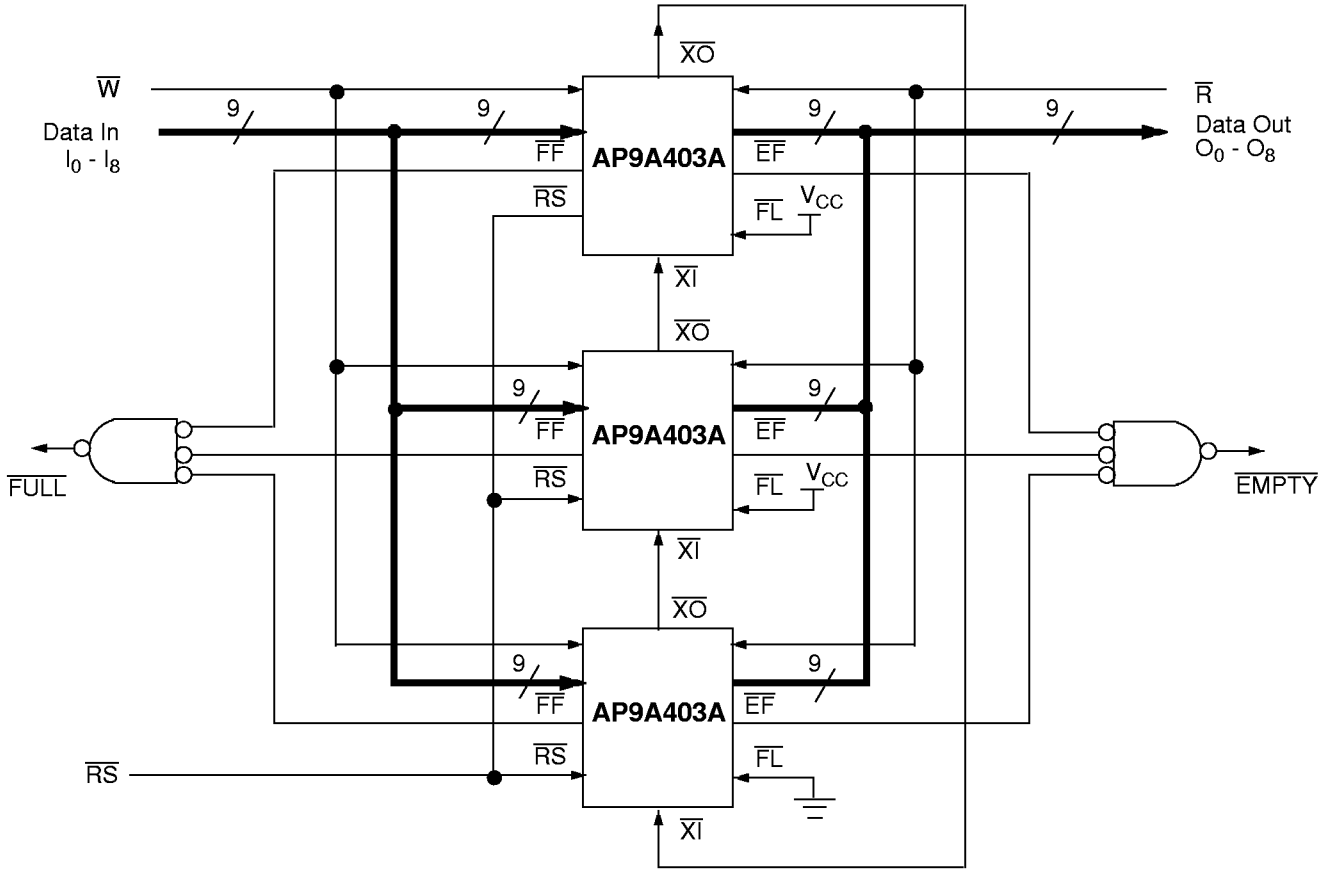


Figure 3. FIFO Depth Expansion (6144 x 9)

9A403A-6

Operational Modes (continued)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications that require bidirectional data buffering between two systems can be realized by operating AP9A403A devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

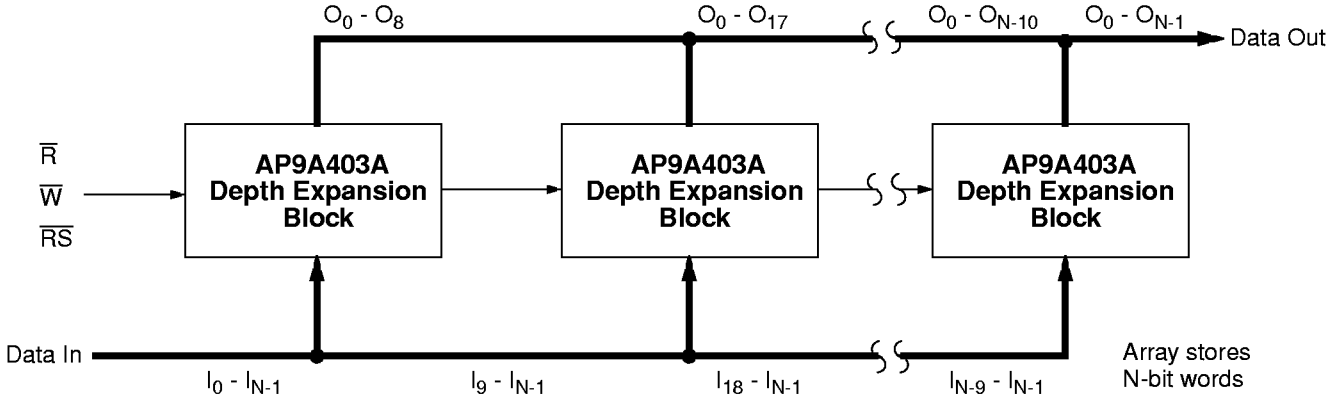
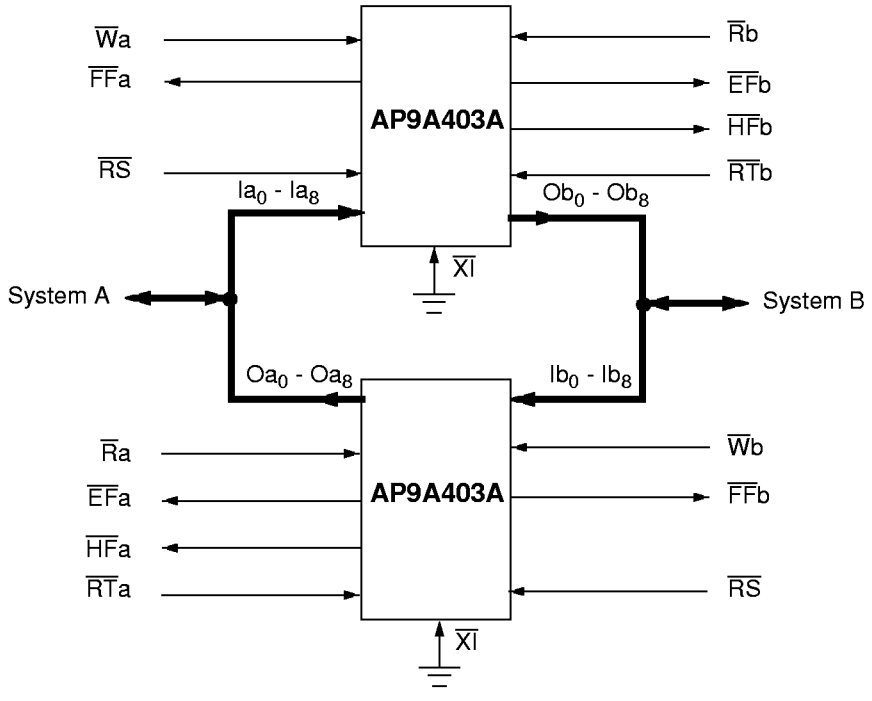


Figure 4. Compound FIFO Expansion

9A403A-7

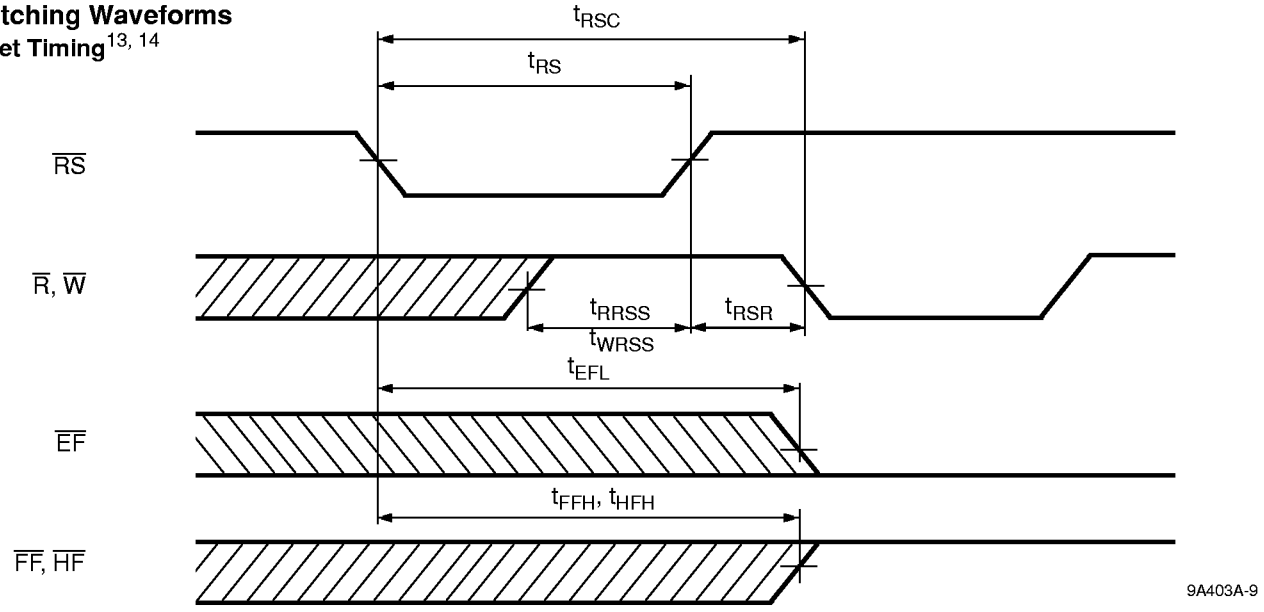


9A403A-8

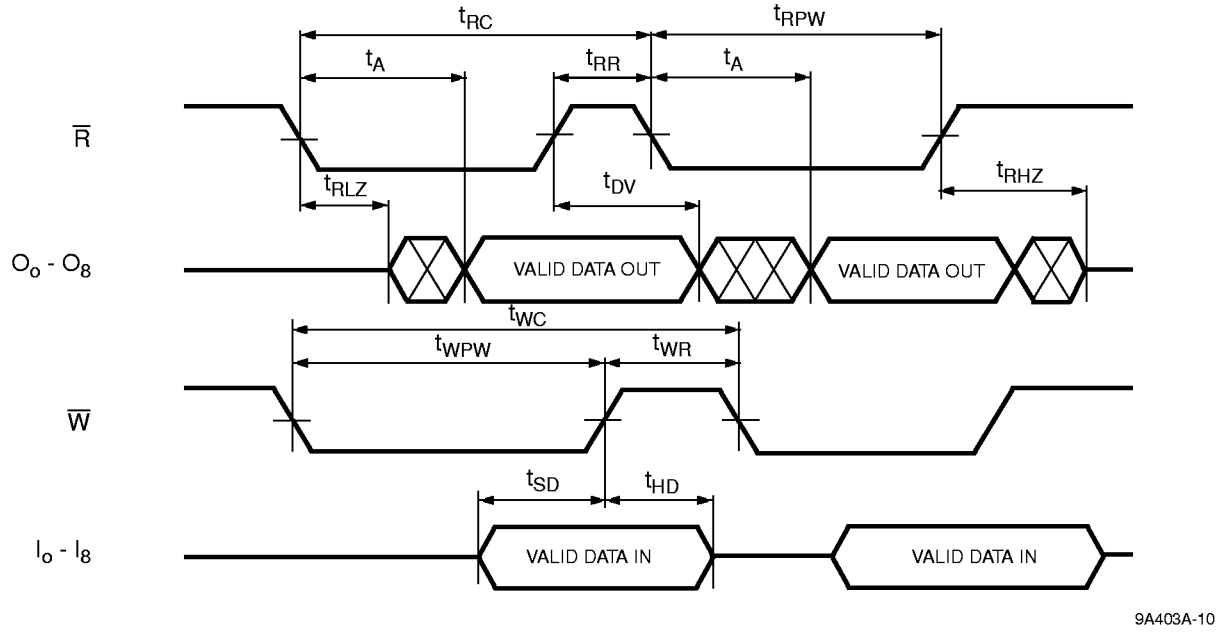
Figure 5. Bidirectional FIFO Buffer (2048 x 9 x 2)

Switching Waveforms

Reset Timing[13, 14]



Asynchronous Write and Read Operation

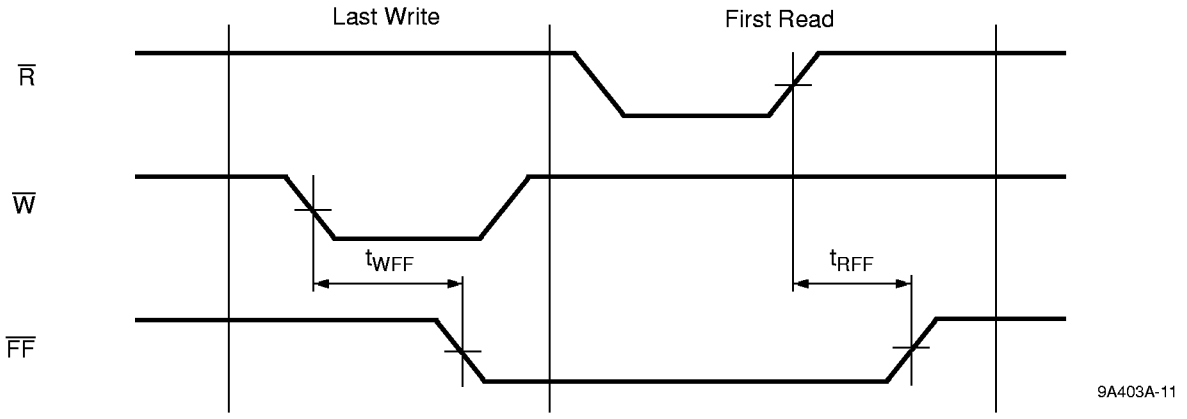


Notes:

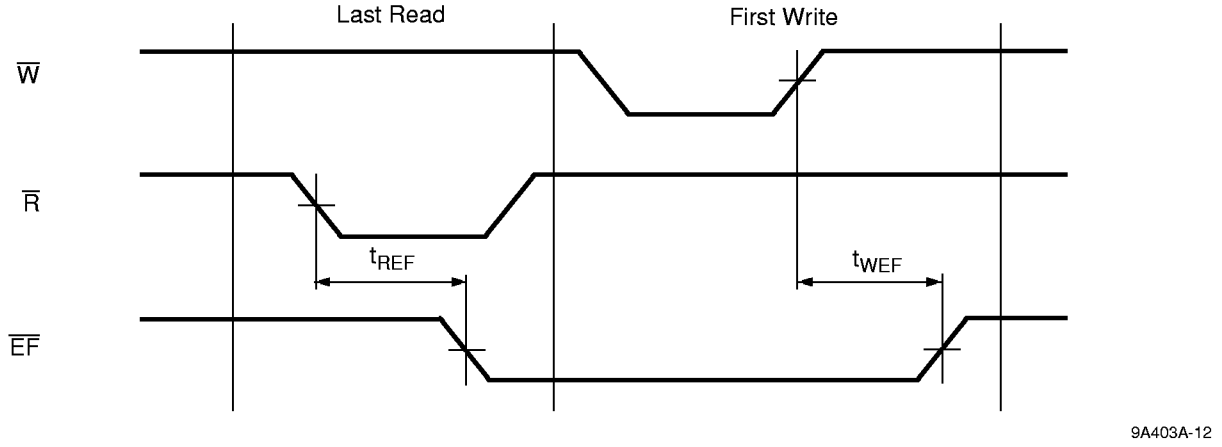
13. $t_{RSC} = t_{RS} + t_{RSR}$.
14. $\overline{W}$ and $\overline{R}$ $_{IH}$V around the rising edge of $\overline{RS}$.

Switching Waveforms (continued)

Full Flag from Last Write to First Read

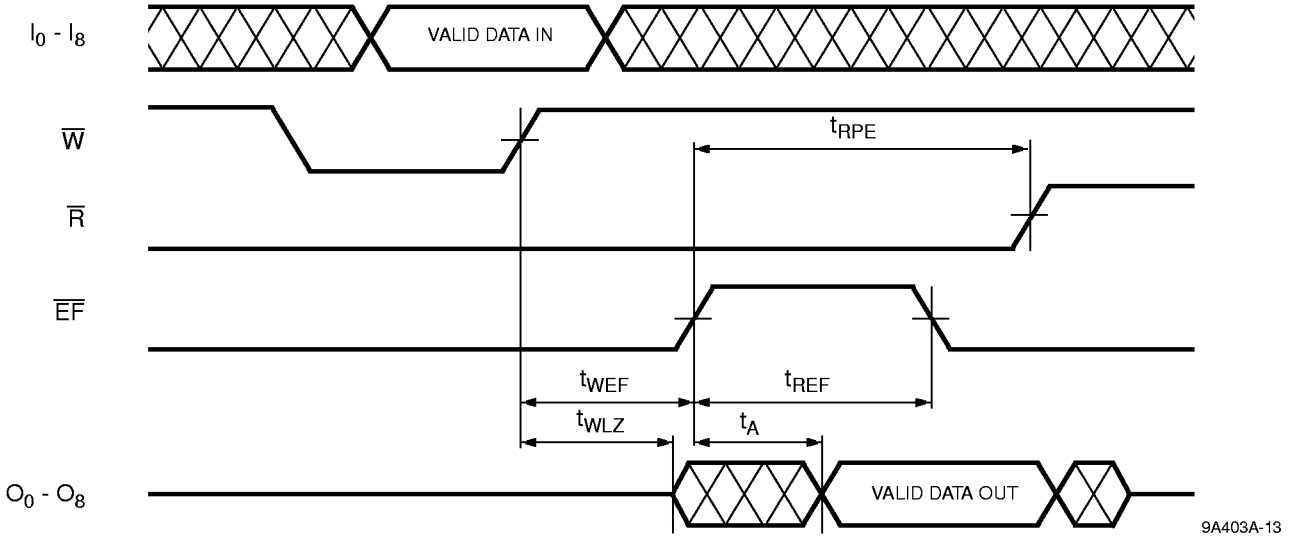


Empty Flag from Last Read to First Write

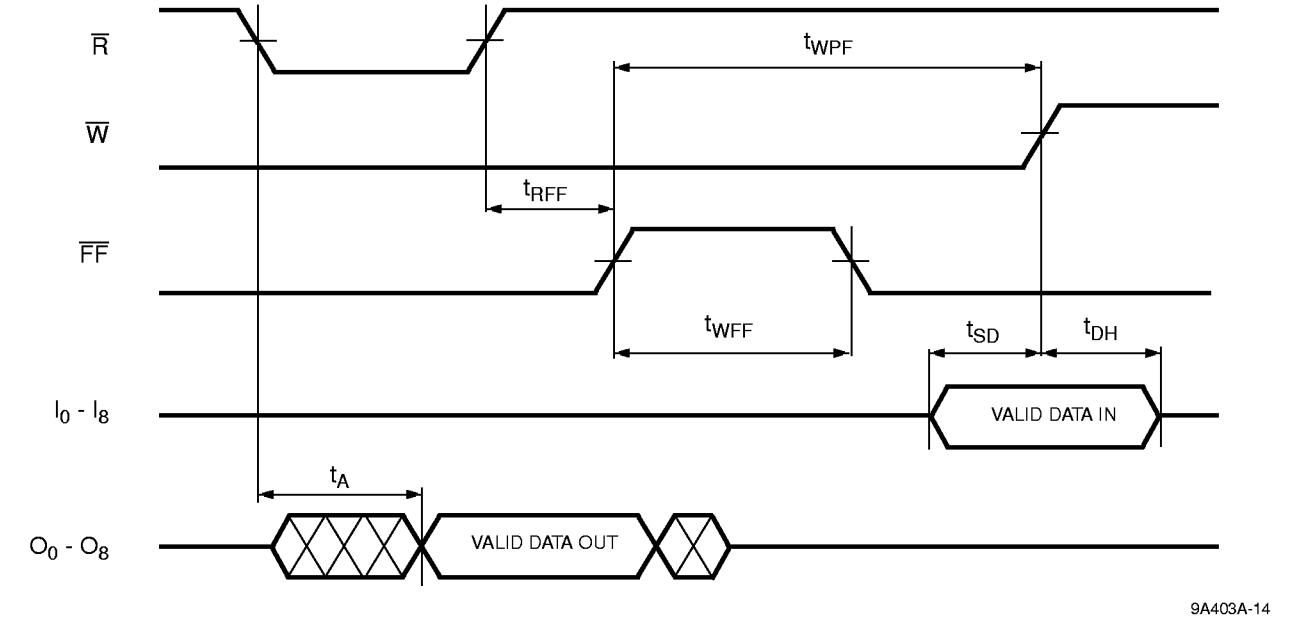


Switching Waveforms (continued)

Read Data Flow-Through [15, 16]



Write Data Flow-Through [17, 18]

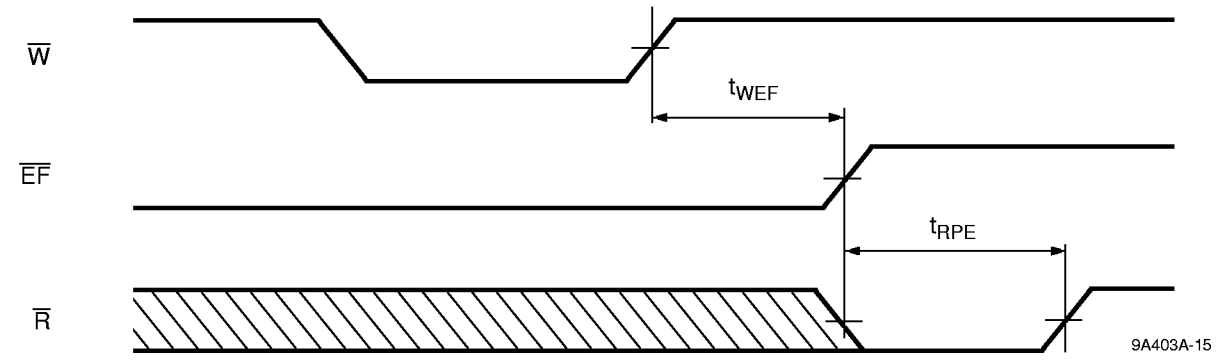


Notes:

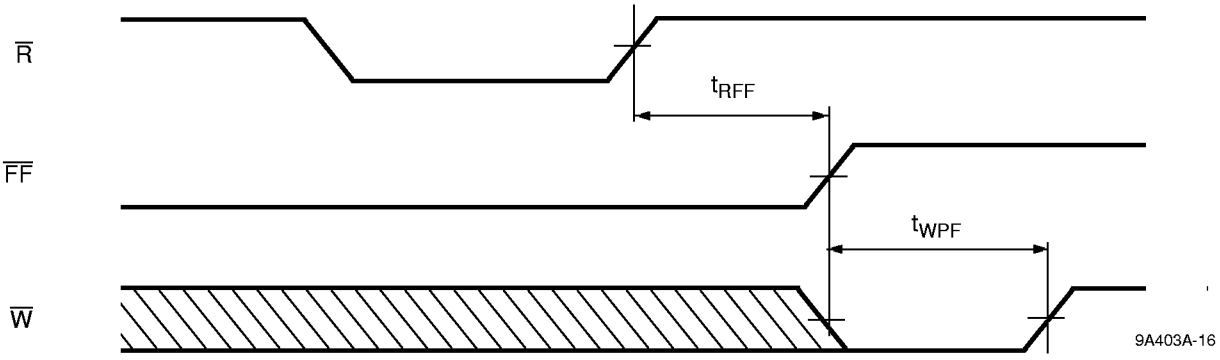
15. $t_{WPF} = t_{WPW}$
16. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

Switching Waveforms (continued)

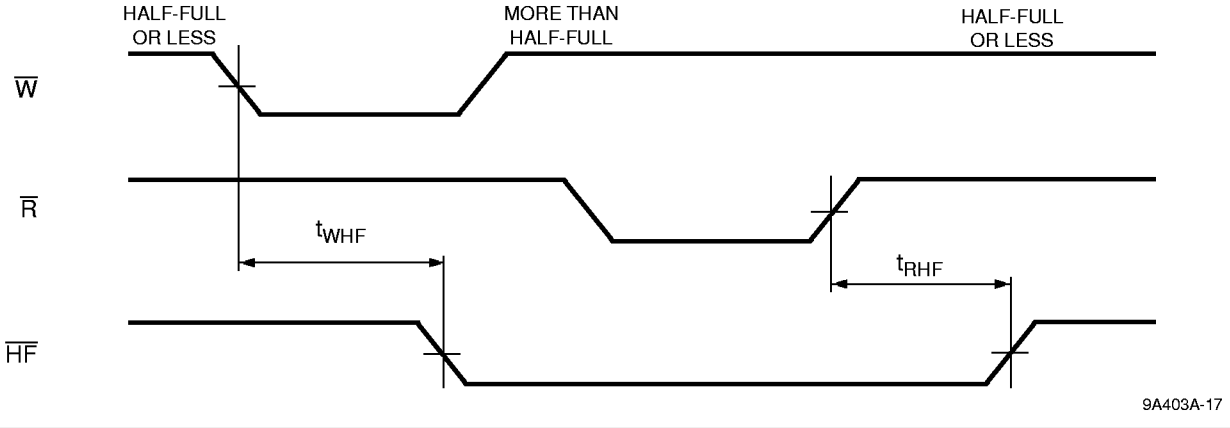
Empty Flag Timing [17, 18]



Full Flag Timing [15, 16]



Half-Full Flag Timing

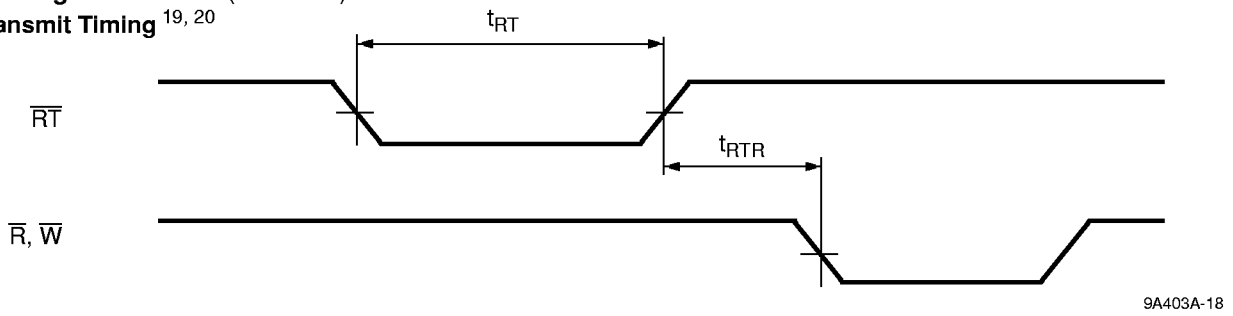


Notes:

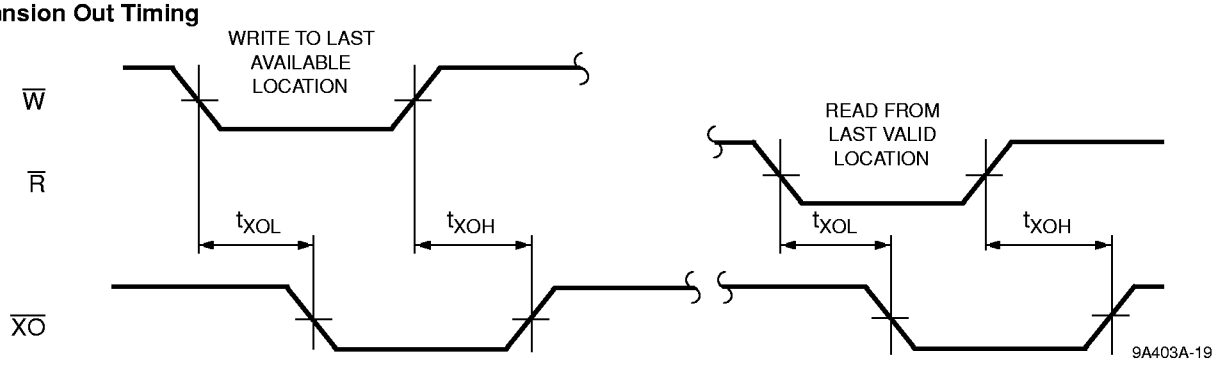
17. $t_{RPE} = t_{RPW}$.
18. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

Switching Waveforms (continued)

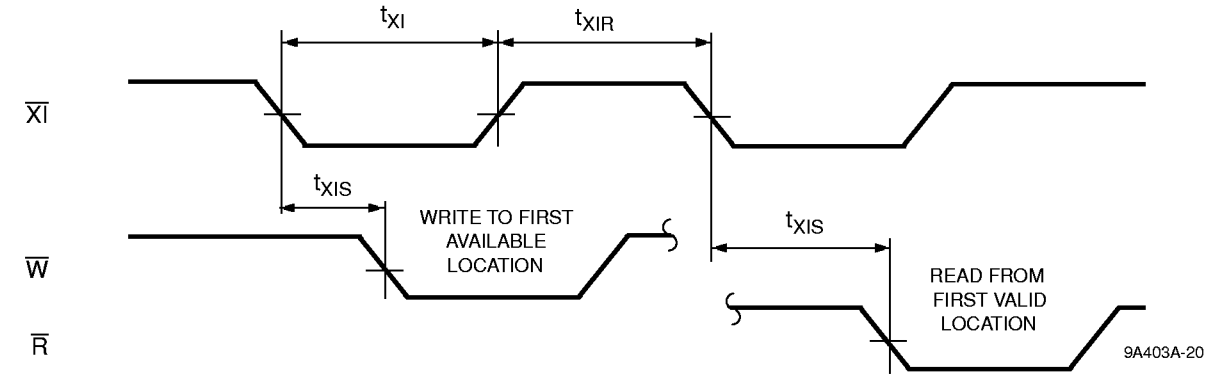
Retransmit Timing [19, 20]



Expansion Out Timing



Expansion In Timing



Notes:

19. $t_{RTC} = t_{RT} + t_{RTR}$
20. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit, but flags will be valid at t_{RTC}.

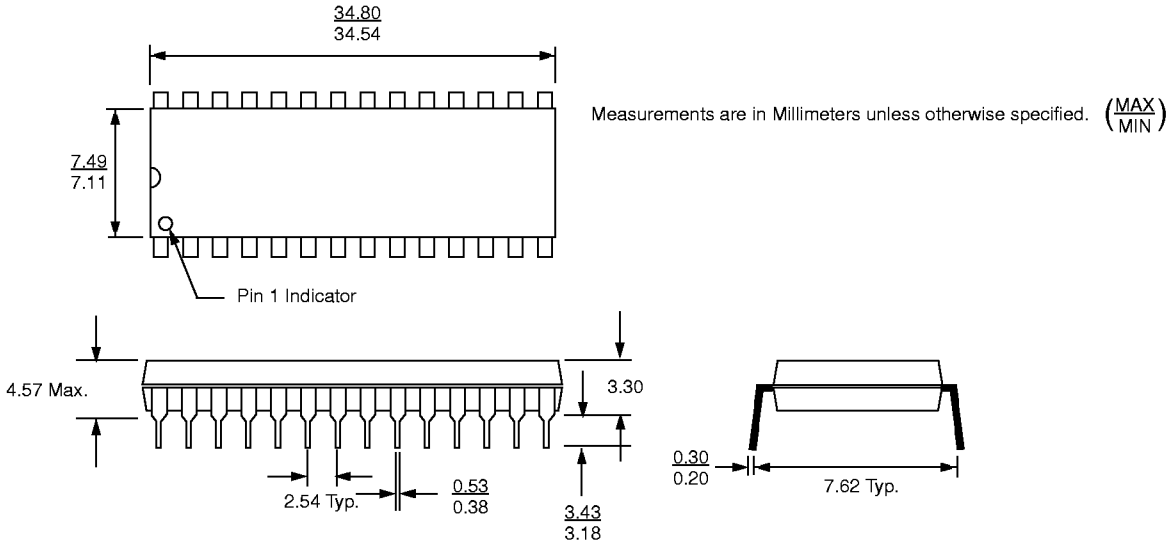
Ordering Information

Speed	Part Number	Package Name	Package Type
15	AP9A403A-15JC	J32.1	32-Pin Plastic Leaded Chip Carrier
	AP9A403A-15PC	P28.1	28-Pin Dual In-Line Package
20	AP9A403A-20JC	J32.1	32-Pin Plastic Leaded Chip Carrier
	AP9A403A-20PC	P28.1	28-Pin Dual In-Line Package
25	AP9A403A-25JC	J32.1	32-Pin Plastic Leaded Chip Carrier
	AP9A403A-25PC	P28.1	28-Pin Dual In-Line Package
35	AP9A403A-35JC	J32.1	32-Pin Plastic Leaded Chip Carrier
	AP9A403A-35PC	P28.1	28-Pin Dual In-Line Package

Document # DS-00023-Rev**

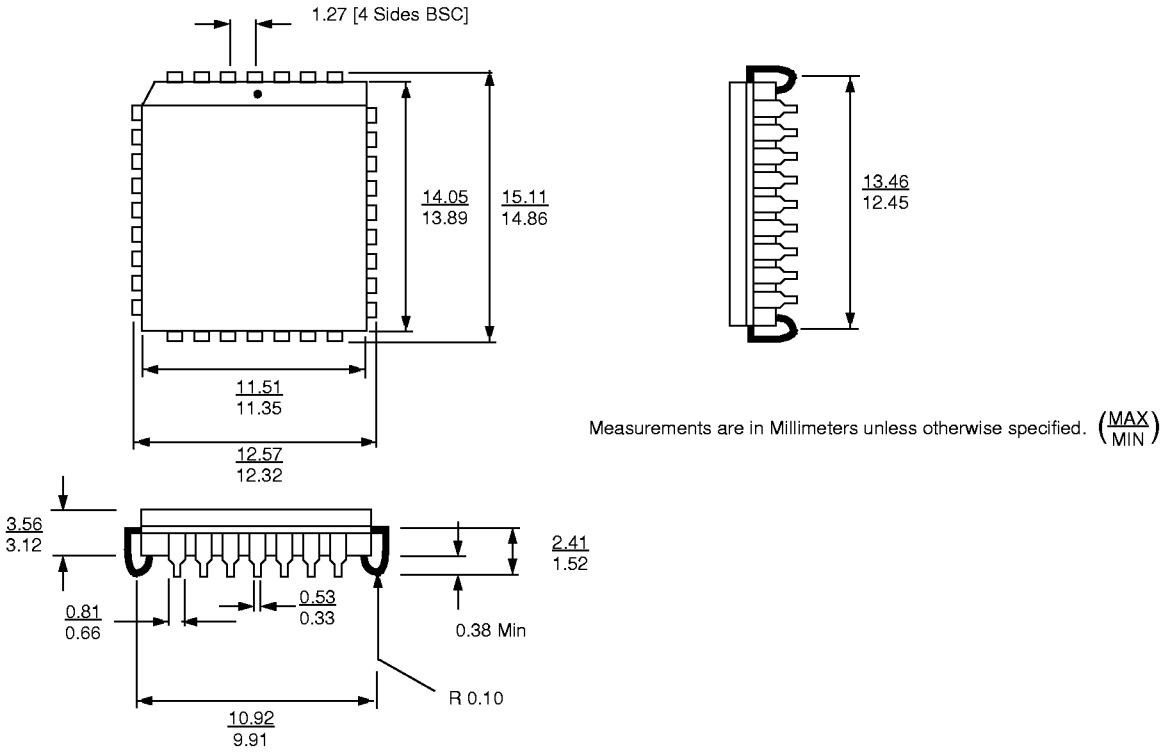
Package Diagrams

P28.1 - 28-Pin (300-Mil) Plastic Dual In-Line Package (DIP)



Package Diagrams (continued)

J32.1 - 32-Pin Plastic Leaded Chip Carrier (PLCC)



Measurements are in Millimeters unless otherwise specified. (MAX / MIN)