

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4053

Triple 2-channel analog multiplexer/demultiplexer

Product specification
File under Integrated Circuits, IC06

December 1990

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

FEATURES

- Low "ON" resistance:
80 Ω (typ.) at $V_{CC} - V_{EE} = 4.5$ V
70 Ω (typ.) at $V_{CC} - V_{EE} = 6.0$ V
60 Ω (typ.) at $V_{CC} - V_{EE} = 9.0$ V
- Logic level translation:
to enable 5 V logic to communicate with ± 5 V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the "4053" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

$V_{EE} = GND = 0$ V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZH}/t_{PZL}	turn "ON" time \bar{E} to V_{OS} S_n to V_{OS}	$C_L = 15$ pF; $R_L = 1$ kΩ; $V_{CC} = 5$ V	17	23	ns
			21	21	ns
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E} to V_{OS} S_n to V_{OS}		18	20	ns
			17	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	36	36	pF
C_S	max. switch capacitance independent (Y) common (Z)		5	5	pF
			8	8	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

$$\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\} = \text{sum of outputs}$$

C_L = output load capacitance in pF; C_S = max. switch capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

ORDERING INFORMATION

See "[74HC/HCT/HCU/HCMOS Logic Package Information](#)".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1	2Y ₀ to, 2Y ₁	independent inputs/outputs
5, 3	3Y ₀ to, 3Y ₁	independent inputs/outputs
6	Ē	enable input (active LOW)
7	V _{EE}	negative supply voltage
8	GND	ground (0 V)
11, 10, 9	S ₁ to S ₃	select inputs
12, 13	1Y ₀ , 1Y ₁	independent inputs/outputs
14, 15, 4	1Z to 3Z	common inputs/outputs
16	V _{CC}	positive supply voltage

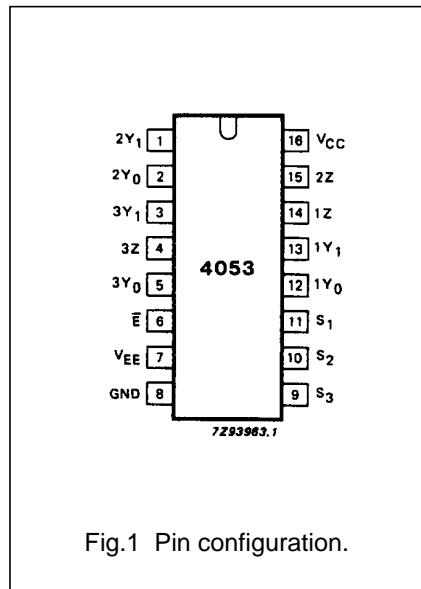


Fig.1 Pin configuration.

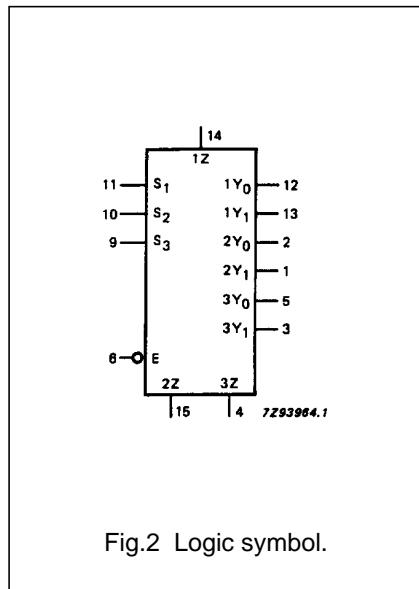


Fig.2 Logic symbol.

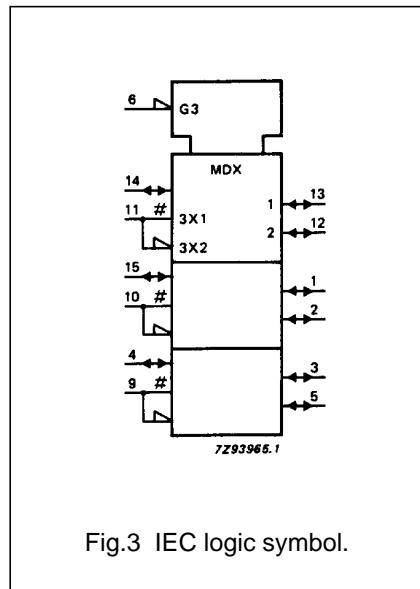


Fig.3 IEC logic symbol.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

APPLICATIONS

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

FUNCTION TABLE

INPUTS		CHANNEL ON
\bar{E}	S_n	
L	L	$nY_0 - nZ$
L	H	$nY_1 - nZ$
H	X	none

Note

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

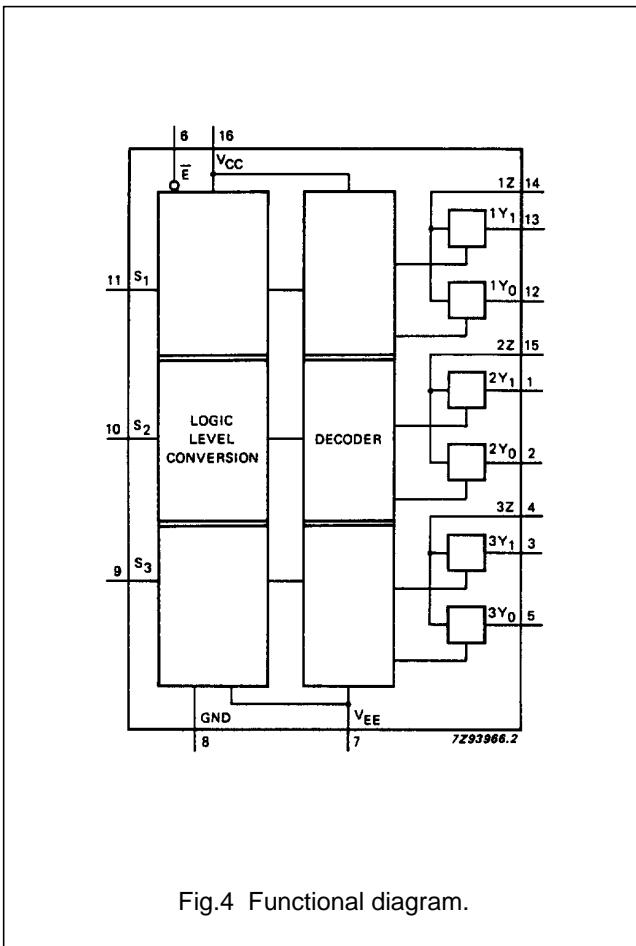


Fig.4 Functional diagram.

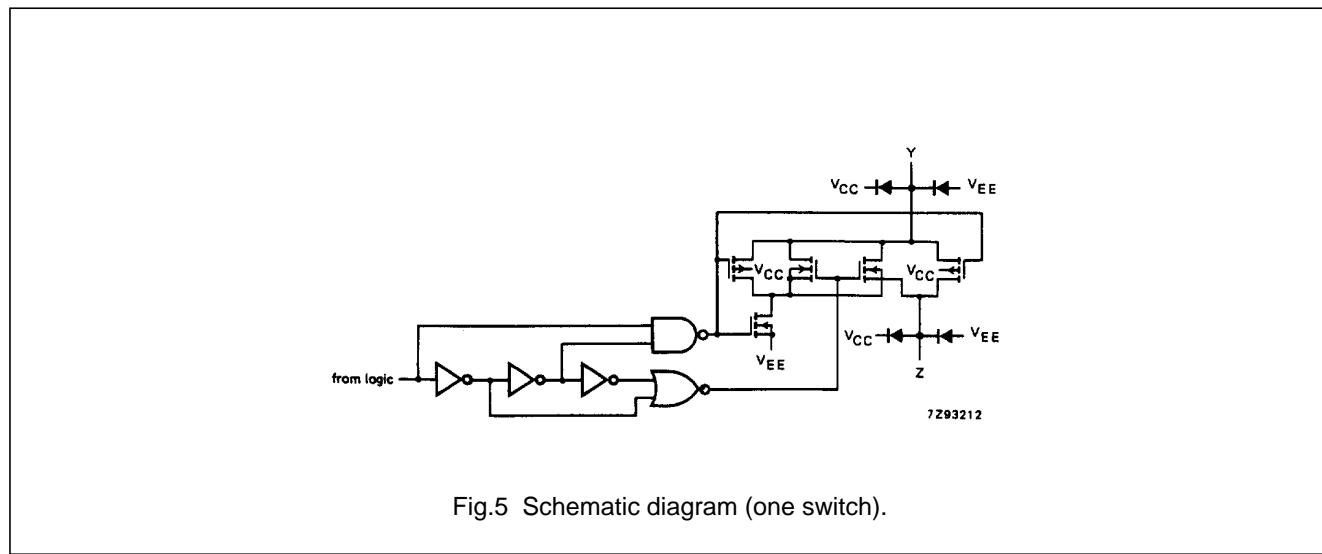


Fig.5 Schematic diagram (one switch).

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to V_{EE} = GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V
$\pm I_S$	DC switch current		25	mA	for -0.5 V < V_S < $V_{CC} + 0.5$ V
$\pm I_{EE}$	DC V_{EE} current		20	mA	
$\pm I_{CC}; \pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	-65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: -40 to + 125 °C 74HC/HCT
	plastic DIL		750	mW	above + 70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above + 70 °C: derate linearly with 8 mW/K
P_S	power dissipation per switch		100	mW	

Note to ratings

To avoid drawing V_{CC} current out of terminals nZ , when switch current flows in terminals nY_n , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ , no V_{CC} current will flow out of terminals nY_n . In this case there is no limit for the voltage drop across the switch, but the voltages at nY_n and nZ may not exceed V_{CC} or V_{EE} .

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage V_{CC} -GND	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
V_{CC}	DC supply voltage V_{CC} - V_{EE}	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
V_I	DC input voltage range	GND		V_{CC}	GND		V_{CC}	V	
V_S	DC switch voltage range	V_{EE}		V_{CC}	V_{EE}		V_{CC}	V	
T_{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t_r, t_f	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V $V_{CC} = 10.0$ V

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

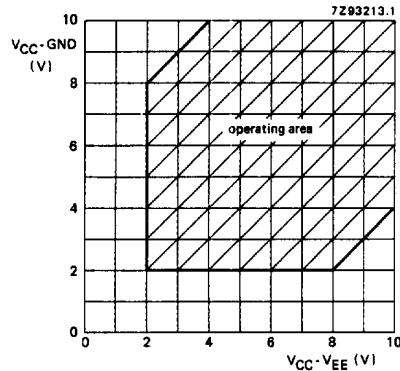


Fig.6 Guaranteed operating area as a function of the supply voltages for 74HC4053.

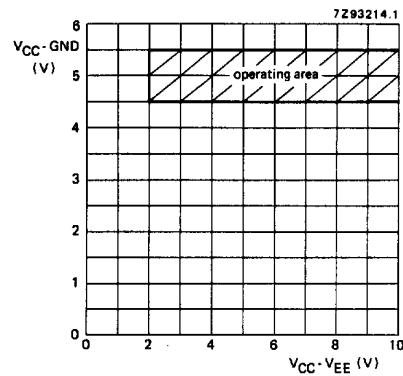


Fig.7 Guaranteed operating area as a function of the supply voltages for 74HCT4053.

DC CHARACTERISTICS FOR 74HC/HCT

For 74HC: $V_{CC} - GND$ or $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

For 74HCT: $V_{CC} - GND = 4.5$ and 5.5 V ; $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$ and 9.0 V

SYMBOL	PARAMETER	T_{amb} ($^{\circ}\text{C}$)							UNIT	TEST CONDITIONS										
		74HC/HCT																		
		+ 25			-40 to +85		-40 to +125													
		min.	typ.	max.	min.	max.	min.	max.												
R _{ON}	ON resistance (peak)	—	—	—	—	—	—	—	Ω	2.0	0	100	V_{CC} to V_{EE}	V_{IH} or V_{IL}						
		100	180	225	200	240	270	270	Ω	4.5	0	1000								
		90	160	200	165	195	240	240	Ω	6.0	0	1000								
		70	130	165	130	195	270	270	Ω	4.5	-4.5	1000								
R _{ON}	ON resistance (rail)	150	—	—	—	—	—	—	Ω	2.0	0	100	V_{EE}	V_{IH} or V_{IL}						
		80	140	175	150	180	210	210	Ω	4.5	0	1000								
		70	120	150	130	160	180	180	Ω	6.0	0	1000								
		60	105	130	105	160	160	160	Ω	4.5	-4.5	1000								
R _{ON}	ON resistance (rail)	150	—	—	—	—	—	—	Ω	2.0	0	100	V_{CC}	V_{IH} or V_{IL}						
		90	160	200	175	210	240	240	Ω	4.5	0	1000								
		80	140	175	150	180	210	210	Ω	6.0	0	1000								
		65	120	150	120	180	180	180	Ω	4.5	-4.5	1000								
ΔR_{ON}	maximum ΔR_{ON} resistance between any two channels	—	9	—	—	—	—	—	Ω	2.0	0	—	V_{CC} to V_{EE}	V_{IH} or V_{IL}						
		9	—	—	—	—	—	—	Ω	4.5	0	—								
		8	—	—	—	—	—	—	Ω	6.0	0	—								
		6	—	—	—	—	—	—	Ω	4.5	-4.5	—								

Notes to the characteristics

- At supply voltages ($V_{CC} - V_{EE}$) approaching 2.0 V the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring R_{ON} see Fig.8.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS							
		74HC							V _{CC} V	V _{EE} V	V _I	OTHER				
		+25			−40 to +85		−40 to +125									
		min.	typ.	max.	min.	max.	min.	max.								
V _{IH}	HIGH level input voltage	1.5 3.15 4.2 6.3	1.2 2.4 3.2 4.7		1.5 3.15 4.2 6.3		1.5 3.15 4.2 6.3		V	2.0 4.5 6.0 9.0						
V _{IL}	LOW level input voltage		0.8 2.1 2.8 4.3	0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7		0.5 1.35 1.8 2.7	V	2.0 4.5 6.0 9.0						
±I _I	input leakage current			0.1 0.2		1.0 2.0		1.0 2.0	µA	6.0 10.0	0	V _{CC} or GND				
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig.10)			
±I _S	analog switch OFF-state current all channels			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig.10)			
±I _S	analog switch ON-state current			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL}	V _S = V _{CC} − V _{EE} (see Fig.11)			
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	µA	6.0 10.0	0	V _{CC} or GND	V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE}			

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

AC CHARACTERISTICS FOR 74HCGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} ($^{\circ}$ C)						UNIT	TEST CONDITIONS					
		74HC							V _{CC} (V)	V _{EE} (V)	OTHER			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		15 5 4 4	60 12 10 8		75 15 13 10		90 18 15 12	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)		
t_{PZH}/t_{PZL}	turn "ON" time \bar{E} to V_{os}		60 20 16 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PZH}/t_{PZL}	turn "ON" time S_n to V_{os}		75 25 20 15	220 44 37 31		275 55 47 39		330 66 56 47	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		63 21 17 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PHZ}/t_{PLZ}	turn "OFF" time S_n to V_{os}		60 20 16 15	210 42 36 29		265 53 45 36		315 63 54 44	ns	2.0 4.5 6.0 4.5	0 0 0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS							
		74HCT							V _{CC} (V)	V _{EE} (V)	V _I	OTHER				
		+25		−40 to +85		−40 to +125										
		min.	typ.	max.	min.	max.	min.	max.								
V _{IH}	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5						
V _{IL}	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5						
±I _I	input leakage current			0.1		1.0		1.0	µA	5.5	0	V _{CC} or GND				
±I _S	analog switch OFF-state current per channel			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL} = V _{CC} − V _{EE} Fig.10				
±I _S	analog switch OFF-state current all channels			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL} = V _{CC} − V _{EE} Fig.10				
±I _S	analog switch ON-state current			0.1		1.0		1.0	µA	10.0	0	V _{IH} or V _{IL} = V _{CC} − V _{EE} Fig.11				
I _{CC}	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	µA	5.5 5.0	0 −5.0	V _{CC} or GND; V _{IS} = V _{EE} or V _{CC} ; V _{OS} = V _{CC} or V _{EE}				
ΔI _{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	µA	4.5 to 5.5	0	V _{CC} − 2.1 V	other inputs at V _{CC} or GND			

Note to HCT types

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S _n	0.50
E	0.50

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} ($^{\circ}$ C)						UNIT	TEST CONDITIONS					
		74HCT							V _{CC} (V)	V _{EE} (V)	OTHER			
		+25			−40 to +85		−40 to +125							
		min.	typ.	max.	min.	max.	min.	max.						
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}		5 4	12 8		15 10		18 12	ns	4.5 4.5	0 −4.5	$R_L = \infty$; $C_L = 50$ pF (see Fig.18)		
t_{PZH}/t_{PZL}	turn "ON" time \bar{E} to V_{os}		27 16	48 34		60 43		72 51	ns	4.5 4.5	0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PZH}/t_{PZL}	turn "ON" time S_n to V_{os}		25 16	48 34		60 43		72 51	ns	4.5 4.5	0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PHZ}/t_{PLZ}	turn "OFF" time \bar{E} to V_{os}		24 15	44 31		55 39		66 47	ns	4.5 4.5	0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		
t_{PHZ}/t_{PLZ}	turn "OFF" time S_n to V_{os}		22 15	44 31		55 39		66 47	ns	4.5 4.5	0 −4.5	$R_L = 1$ k Ω ; $C_L = 50$ pF (see Figs 19, 20 and 21)		

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

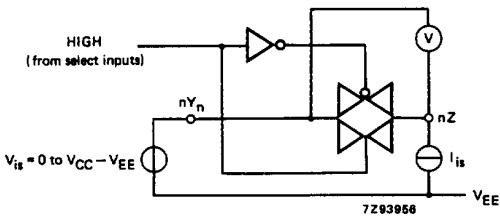


Fig.8 Test circuit for measuring R_{ON} .

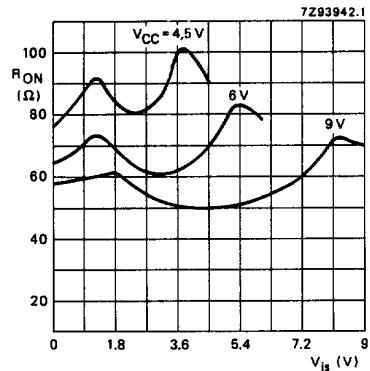


Fig.9 Typical R_{ON} as a function of input voltage V_{IS} for $V_{IS} = 0$ to $V_{CC} - V_{EE}$.

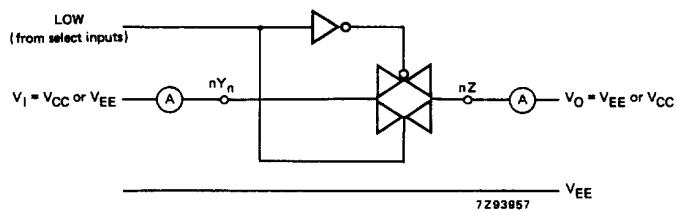


Fig.10 Test circuit for measuring OFF-state current.

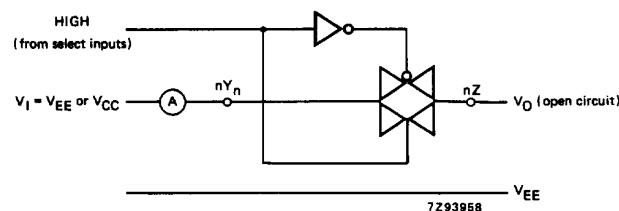


Fig.11 Test circuit for measuring ON-state current.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

Recommended conditions and typical values

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	typ.	UNIT	V_{CC} (V)	V_{EE} (V)	$V_{IS(p-p)}$ (V)	CONDITIONS
	sine-wave distortion $f = 1$ kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig.14)
	sine-wave distortion $f = 10$ kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	$R_L = 10 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ (see Fig.14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$ $f = 1$ MHz see (Fig.12 and 15)
	crosstalk between any two switches/multiplexers	-60 -60	dB dB	2.25 4.5	-2.25 -4.5	note 1	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$ $f = 1$ MHz (see Fig.16)
$V_{(p-p)}$	crosstalk voltage between control and any switch (peak-to-peak value)	110 220	mV mV	4.5 4.5	0 -4.5		$R_L = 600 \text{ k}\Omega$; $C_L = 50 \text{ pF}$ $f = 1$ MHz (E or S_n , square-wave between V_{CC} and GND, $t_r = t_f = 6$ ns (see Fig.17)
f_{max}	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	$R_L = 50 \Omega$; $C_L = 10 \text{ pF}$ (see Fig.13 and 14)
C_s	maximum switch capacitance independent (Y) common (Z)	5 8	pF pF				

Notes to the AC characteristics

1. Adjust input voltage V_{IS} to 0 dBm level (0 dBm = 1 mW into 600Ω).
2. Adjust input voltage V_{IS} to 0 dBm level at V_{OS} for 1 MHz (0 dBm = 1 mW into 50Ω).

General note

 V_{IS} is the input voltage at an nY_n or nZ terminal, whichever is assigned as an input. V_{OS} is the output voltage at an nY_n or nZ terminal, whichever is assigned as an output

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

Test conditions:
 $V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $V_{EE} = -4.5 \text{ V}$;
 $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

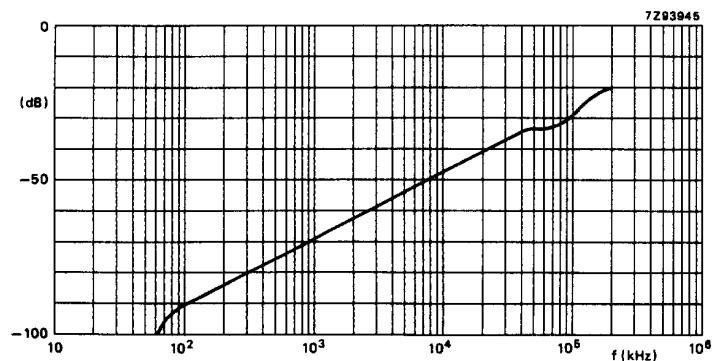


Fig.12 Typical switch "OFF" signal feed-through as a function of frequency.

Test conditions:
 $V_{CC} = 4.5 \text{ V}$; $GND = 0 \text{ V}$; $V_{EE} = -4.5 \text{ V}$;
 $R_L = 50 \Omega$; $R_{source} = 1 \text{ k}\Omega$.

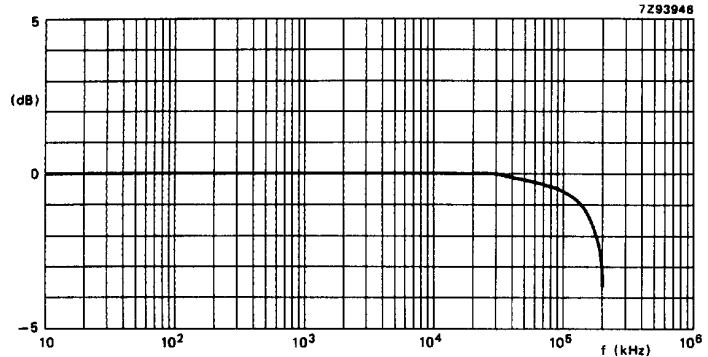


Fig.13 Typical frequency response.

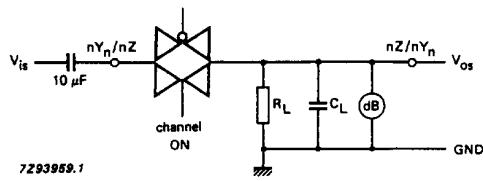


Fig.14 Test circuit for measuring sine-wave distortion and minimum frequency response.

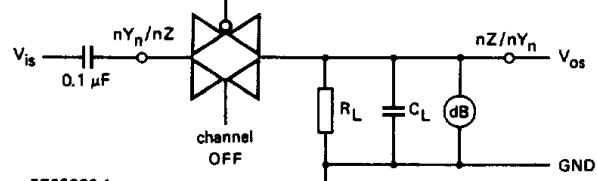


Fig.15 Test circuit for measuring switch "OFF" signal feed-through.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

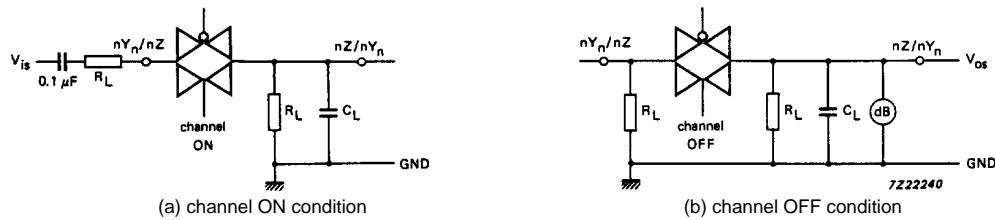


Fig.16 Test circuits for measuring crosstalk between any two switches/multiplexers.

The crosstalk is defined as follows
(oscilloscope output):

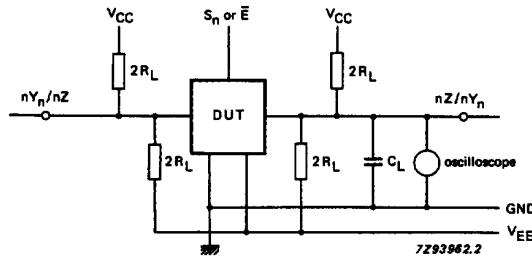
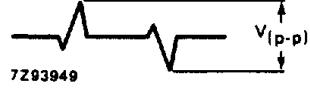


Fig.17 Test circuit for measuring crosstalk between control and any switch.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

AC WAVEFORMS

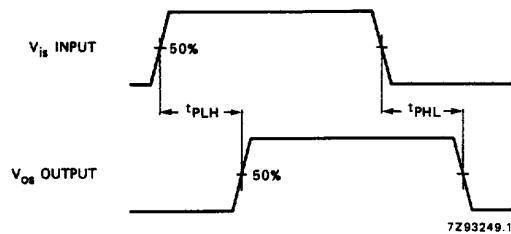
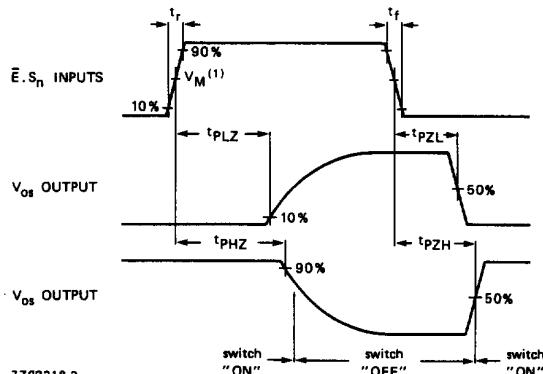
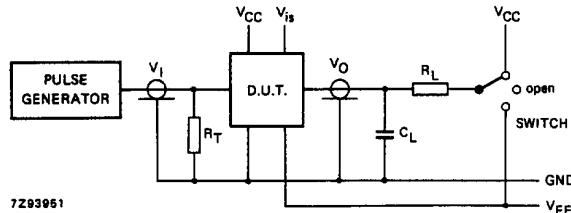
Fig.18 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.

Fig.19 Waveforms showing the turn-ON and turn-OFF times.

Triple 2-channel analog multiplexer/demultiplexer

74HC/HCT4053

TEST CIRCUIT AND WAVEFORMS



Conditions

TEST	SWITCH	V_{IS}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

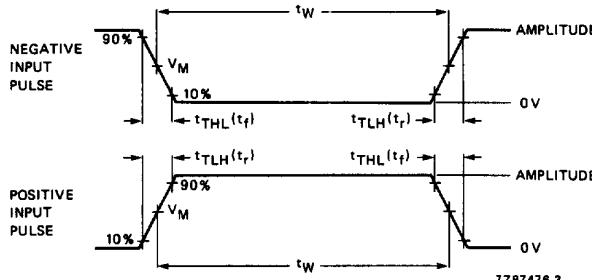
FAMILY	AMPLITUDE	V_M	$t_r; t_f$	
			$f_{max};$ PULSE WIDTH	OTHER
74HC	V_{CC}	50%	<2 ns	6 ns
74HCT	3.0 V	1.3 V	<2 ns	6 ns

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r, t_f with 50% duty factor.

Fig.20 Test circuit for measuring AC performance.



Conditions

TEST	SWITCH	V_{IS}
t_{PZH}	V_{EE}	V_{CC}
t_{PZL}	V_{CC}	V_{EE}
t_{PHZ}	V_{EE}	V_{CC}
t_{PLZ}	V_{CC}	V_{EE}
others	open	pulse

FAMILY	AMPLITUDE	V_M	$t_r; t_f$	
			$f_{max};$ PULSE WIDTH	OTHER
74HC	V_{CC}	50%	<2 ns	6 ns
74HCT	3.0 V	1.3 V	<2 ns	6 ns

C_L = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

$t_r = t_f = 6$ ns; when measuring f_{max} , there is no constraint to t_r, t_f with 50% duty factor.

Fig.21 Input pulse definitions.

Triple 2-channel analog
multiplexer/demultiplexer

74HC/HCT4053

PACKAGE OUTLINES

See "*74HC/HCT/HCU/HCMOS Logic Package Outlines*".

74HC/HCT4053; Triple 2-channel analog multiplexer/demultiplexer

Information as of 2003-04-22

My.Semiconductors.COM.
Your personal service from
Philips Semiconductors.
Please register now !

Use right mouse button to
download datasheet

[Download datasheet](#)

Stay informed

Products

General description	Features	Applications	Datasheet
Block diagram	Buy online	Support & tools	Email/translate
Products & packages	Parametrics	Similar products	

[MultiMarket](#)
[Semiconductors](#)

[Product Selector](#)

[Catalog by Function](#)

[Catalog by System](#)

[Cross-reference](#)

[Packages](#)

[End of Life information](#)

[Distributors Go Here!](#)

[Models](#)

[SoC solutions](#)

General description

The 74HC/HCT4053 are high-speed Si-gate CMOS devices and are pin compatible with the '4053' of the '4000B' series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4053 are triple 2-channel analog multiplexers/demultiplexers with a common enable input (E). Each multiplexer/demultiplexer has two independent inputs/outputs (nY_0 and nY_1), a common input/output (nZ) and three digital select inputs (S_1 to S_3).

With E LOW, one of the two switches is selected (low impedance ON-state) by S_1 to S_3 . With E HIGH, all switches are in the high impedance OFF-state, independent of S_1 to S_3 .

V_{CC} and GND are the supply voltage pins for the digital control inputs (S_1 , to S_3 , and E). The V_{CC} to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs (nY_0 and nY_1 , and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

▣ Features

- Low 'ON' resistance:
80 Ω (typ.) at V_{CC} - V_{EE} = 4.5 V
70 Ω (typ.) at V_{CC} - V_{EE} = 6.0 V
60 Ω (typ.) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation: to enable 5 V logic to communicate with ± 5 V analog signals
- Typical 'break before make' built in
- Output capability: non-standard
- I_{CC} category: MSI

▣ Applications

 [AN97022_1: TDA8752 Demonstration board documentation](#) (date 16-Dec-02)

▣ Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT4053	Triple 2-channel analog multiplexer/demultiplexer	12/1/1990	Product specification	17	121	 Download

Additional datasheet info

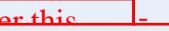
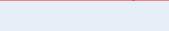
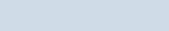
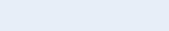
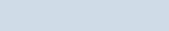
To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

Document	Description
1  HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications
2  HCT_PACKAGE_INFO	HC/T Package Info, The IC06 74HC/HCT/HCMOS Logic Package Information

▣ Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. Pins	Power of Dissipation	Logic Considerations	Switching Levels	Output Drive Capability
74HC4053D	SOT109 (SO16)	Triple 2-Channel Analog Multiplexer/Demultiplexer	10~15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low	
74HC4053DB	SOT338-1 (SSOP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer	10~15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low	
74HC4053N	SOT38-1 (DIP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer	10~15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low	
74HC4053PW	SOT403-1 (TSSOP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer	10~15	5 Volts +	16	Low Power or Battery Applications	CMOS	Low	
74HCT4053D	SOT109 (SO16)	Triple 2-Channel Analog Multiplexer/Demultiplexer; TTL Enabled	10~15	5 Volts +	16	Low Power or Battery Applications	TTL	Low	
74HCT4053DB	SOT338-1 (SSOP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer; TTL Enabled	10~15	5 Volts +	16	Low Power or Battery Applications	TTL	Low	
74HCT4053N	SOT38-1 (DIP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer; TTL Enabled	10~15	5 Volts +	16	Low Power or Battery Applications	TTL	Low	
74HCT4053PW	SOT403-1 (TSSOP16)	Triple 2-Channel Analog Multiplexer/Demultiplexer; TTL Enabled	10~15	5 Volts +	16	Low Power or Battery Applications	TTL	Low	

❑ Products, packages, availability and ordering

Type number	North American type number	Ordering code (12NC)	Marking/Packing  Discretes packing info	Package	Device status	Buy online
74HC4053D	74HC4053D	9337 148 40652	Standard Marking * Bulk Pack, CECC	SOT109 (SO16)	Full production	order this 
	74HC4053D-T	9337 148 40653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT109 (SO16)	Full production	order this 
74HC4053DB	74HC4053DB	9351 668 00112	Standard Marking * Bulk Pack	SOT338-1 (SSOP16)	Full production	order this 
	74HC4053DB-T	9351 668 00118	Standard Marking * Reel Pack, SMD, 13"	SOT338-1 (SSOP16)	Full production	order this 
74HC4053N	74HC4053N	9336 697 60652	Standard Marking * Bulk Pack, CECC	SOT38-1 (DIP16)	Full production	order this 
74HC4053PW	74HC4053PW	9351 869 40112	Standard Marking * Bulk Pack	SOT403-1 (TSSOP16)	Full production	order this 
	74HC4053PW-T	9351 869 40118	Standard Marking * Reel Pack, SMD, 13"	SOT403-1 (TSSOP16)	Full production	order this 
74HCT4053D	74HCT4053D	9337 153 20112	Standard Marking * Bulk Pack	SOT109 (SO16)	Full production	order this 
	74HCT4053D-T	9337 153 20118	Standard Marking * Reel Pack, SMD, 13"	SOT109 (SO16)	Full production	order this 
74HCT4053DB	74HCT4053DB	9351 667 80112	Standard Marking * Bulk Pack	SOT338-1 (SSOP16)	Full production	order this 
	74HCT4053DB-T	9351 667 80118	Standard Marking * Reel Pack, SMD, 13"	SOT338-1 (SSOP16)	Full production	order this 
74HCT4053N	74HCT4053N	9336 703 90112	Standard Marking * Bulk Pack	SOT38-1 (DIP16)	Full production	order this 

74HCT4053PW	74HCT4053PW	9351 884 80112	Standard Marking * Bulk Pack	SOT403-1 (TSSOP16)	Full production	Order this
	74HCT4053PW-T	9351 884 80118	Standard Marking * Reel Pack, SMD, 13"	SOT403-1 (TSSOP16)	Full production	Order this

Products in the above table are all in production. Some variants are discontinued; [click here](#) for information on these variants.

▣ Similar products

 [74HC/HCT4053](#) links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

▣ Support & tools

-  [I²C Bus Solutions - Industrial/Motor Control Applications: Numeric Control Machine](#)(date 01-Jun-02)
-  [HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications](#)(date 01-Mar-98)
-  [HC/T User Guide](#)(date 01-Nov-97)

▣ Email/translate this product information

- [Email this product information.](#)
- Translate this product information page from English to:

The English language is the official language used at the semiconductors.philips.com website and webpages. All translations on this website are created through the use of [Google Language Tools](#) and are provided for convenience purposes only. No rights can be derived from any translation on this website.