Integrated Device Technology, Inc.

VERY LOW POWER 3.3V CMOS FAST SRAM 1 MEG (128K x 8-BIT)

ADVANCE INFORMATION IDT713024SL

FEATURES:

- 128K x 8 advanced high-speed CMOS Static RAM
- Equal access and cycle times
  - — Commercial: 20/25ns
- True 3.3V design, not a re-characterized 5V device
- Ideal for battery-operated equipment, including notebook computers, portable instruments, and portable communications devices
- Low standby currents and 2V data retention mode
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Compliant with all JEDEC LVTTL standard specifications
- Single 3.3V (±0.3V) power supply, resulting in 57% dynamic power savings over equivalent 5 volt devices
- Available in 400 mil plastic DIP and plastic SOJ packages

DESCRIPTION:

The IDT713024SL is a 1,024,576-bit high-speed Static RAM organized as 128K x 8. It is fabricated using IDT's high-perfomance, high-reliability 3.3V CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, results in a unique combination of speed and low power consumption, with only a 3.3V supply.

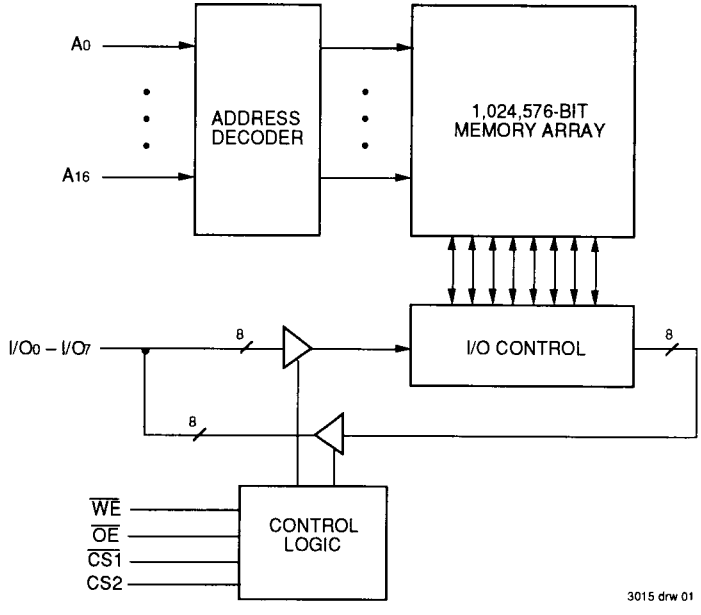
Unlike re-characterized 5V devices, the IDT713024SL is the result of a dedicated 3.3V design, which ensures full compliance with the JEDEC LVTTL standard of operation in terms of thresholds and noise margins. This dedicated 3.3V technology also allows for a faster device.

The IDT713024SL has address access times as fast as 20ns. All bidirectional inputs and outputs are TTL-compatible and operation is from a single 3.3V supply.

This SRAM offers a very low standby current, as well as a data retention mode that guarantees that data be preserved at voltages as low as 2 volts. These characteristics make the IDT713024SL ideal for high-performance applications that are powered by batteries, as well as AC-powered systems that need to minimize power consumption.

The IDT713024SL is packaged in a 32-pin 400 mil plastic DIP, and a 32-pin 400 mil plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



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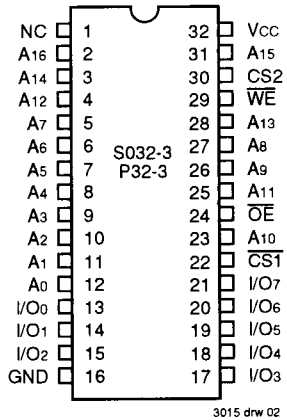
PIN CONFIGURATION



DIP/SOJ
TOP VIEW

TRUTH TABLE(1,2)

INPUTS				I/O	FUNCTION
$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$		
X	H	X	X	High-Z	Deselected–Standby (I_{SB})
X	V_{HC}(3)	X	X	High-Z	Deselected–Standby (I_{SB1})
X	X	L	X	High-Z	Deselected–Standby (I_{SB})
X	X	V_{LC}(3)	X	High-Z	Deselected–Standby (I_{SB1})
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

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NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.