

# 54ABT541

## Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The 'ABT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541 is similar to the 'ABT244 with broad-side pinout.

### Features

- Non-inverting buffers
- Output sink capability of 48 mA, source capability of 24 mA

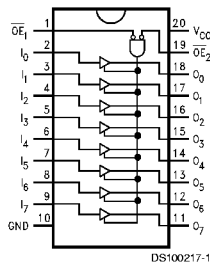
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Flow-through pinout for ease of PC board layout
- Disable time less than enable time to avoid bus contention
- Standard Microcircuit Drawing (SMD) 5962-9471801

### Ordering Code

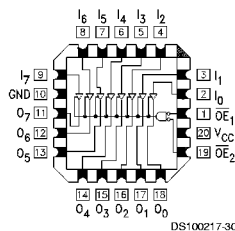
Military	Package Number	Package Description
54ABT541J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT541W-QML	W20A	20-Lead Cerpack
54ABT541E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

### Connection Diagram

Pin Assignment  
DIP and Cerpack



Pin Assignment  
LCC



Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active Low)
$I_0-I_7$	Inputs
$O_0-O_7$	Outputs

### Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	ABT541
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

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## Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential	
Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	-0.5V to 5.5V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output	

in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA
Over Voltage Latchup (I/O)	10V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns

## DC Electrical Characteristics

Symbol	Parameter	ABT541			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Note 4)
				5	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 4)
				-5	μA	Max	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			50	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$
I <sub>OZL</sub>	Output Leakage Current			-50	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$ ; All Others at V <sub>CC</sub> or Ground
I <sub>CCt</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled	2.5		mA		V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE	2.5		mA	Max	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
		Outputs TRI-STATE	50		μA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V; All Others at V <sub>CC</sub> or Ground
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 4)	No Load		0.1	mA/ MHz	Max	Outputs Open, $\overline{OE}_n = GND$ , One Bit Toggling (Note 3), 50% Duty Cycle

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**Note 3:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 4:** Guaranteed, but not tested.

## DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V <sub>CC</sub>	Conditions
						C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>		1.0	V	5.0	T <sub>A</sub> = 25°C (Note 5)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>		-1.45	V	5.0	T <sub>A</sub> = 25°C (Note 5)

**Note 5:** Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

## AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		T <sub>A</sub> = -55°C to +125°C		
		V <sub>CC</sub> = 4.5V–5.5V C <sub>L</sub> = 50 pF		
		Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.0	5.0	ns
t <sub>PHL</sub>	Data to Outputs	1.0	5.3	
t <sub>PZH</sub>	Output Enable Time	1.1	7.2	ns
t <sub>PZL</sub>		1.5	7.9	
t <sub>PHZ</sub>	Output Disable Time	1.5	7.5	ns
t <sub>PLZ</sub>		1.5	7.9	

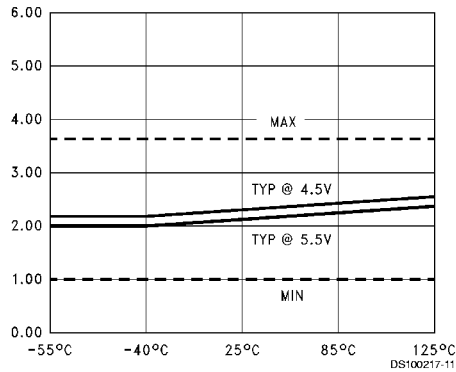
## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	5.0	pF	T <sub>A</sub> = 25°C V <sub>CC</sub> = 0.0V
C <sub>OUT</sub> (Note 6)	Output Capacitance	9.0	pF	V <sub>CC</sub> = 5.0V

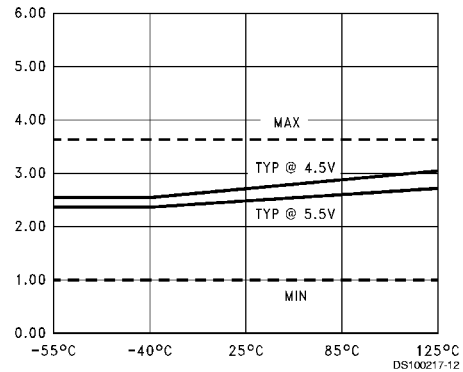
**Note 6:** C<sub>OUT</sub> is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.

## Capacitance (Continued)

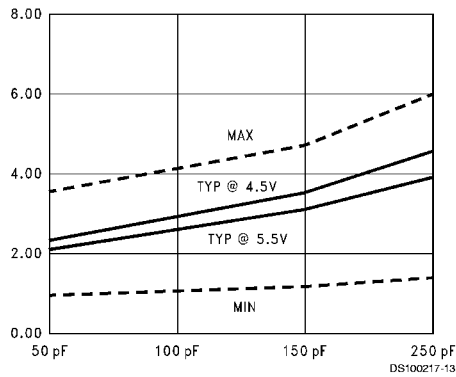
**$t_{PLH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



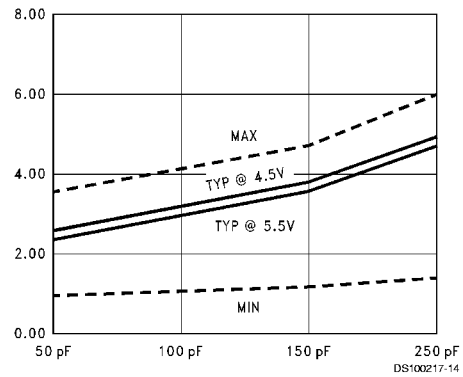
**$t_{PHL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



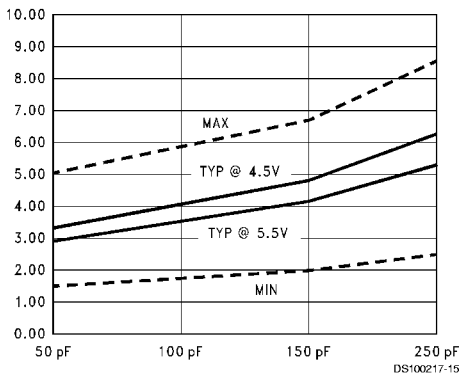
**$t_{PLH}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$



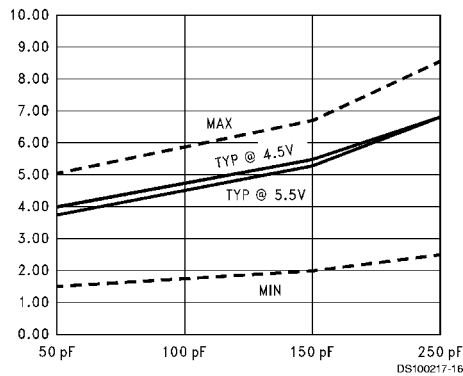
**$t_{PHL}$  vs Load Capacitance**  
 1 Output Switching,  $T_A = 25^\circ\text{C}$



**$t_{PLH}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$



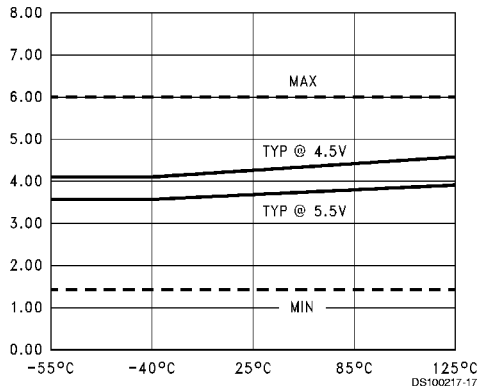
**$t_{PHL}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$



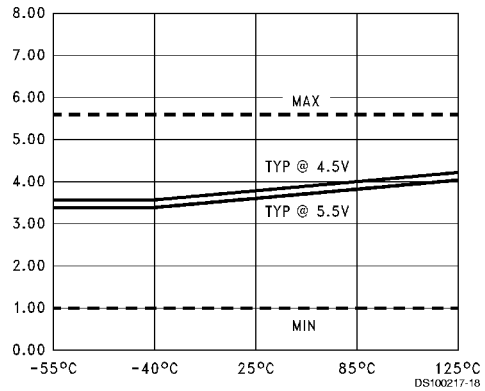
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## Capacitance (Continued)

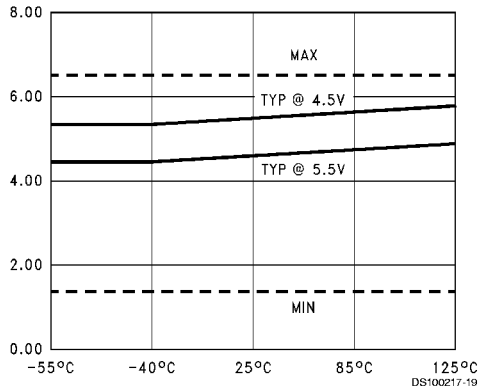
**$t_{PZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



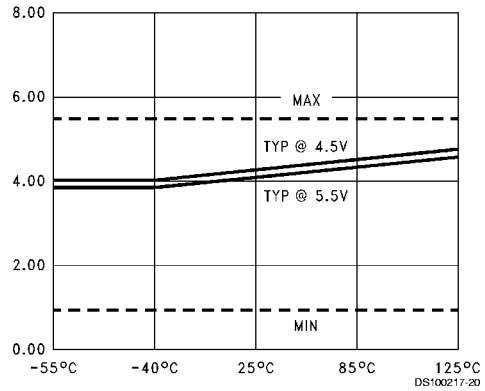
**$t_{PLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



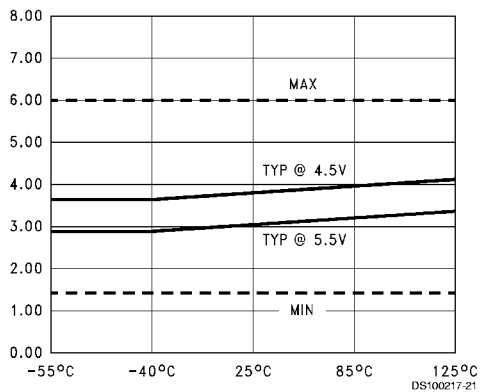
**$t_{PZL}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



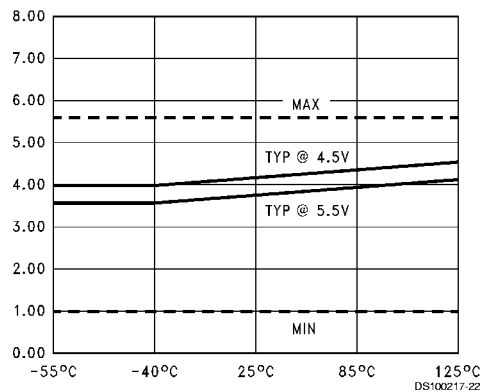
**$t_{PLZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



**$t_{PZH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



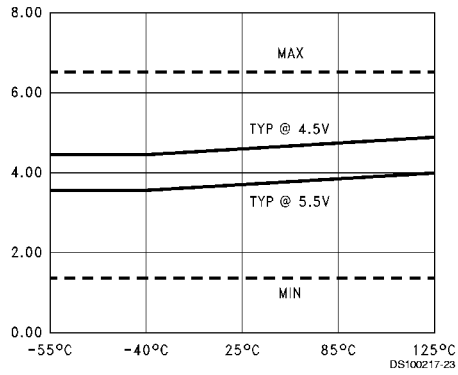
**$t_{PHZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 1 Output Switching



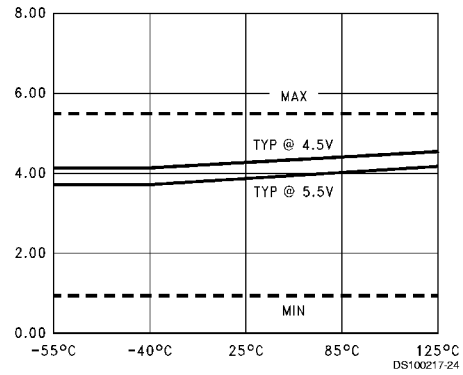
Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## Capacitance (Continued)

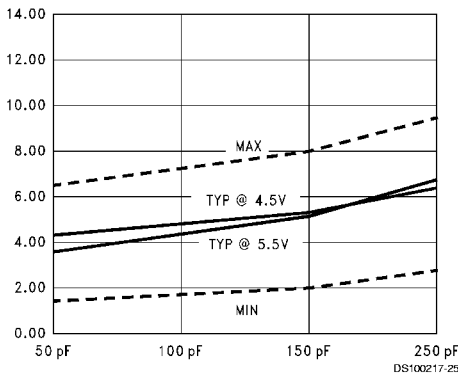
**$t_{PZH}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



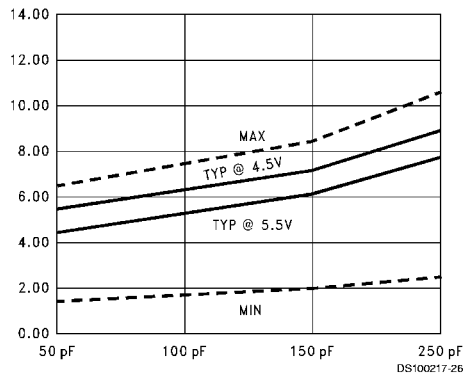
**$t_{PHZ}$  vs Temperature ( $T_A$ )**  
 $C_L = 50$  pF, 8 Outputs Switching



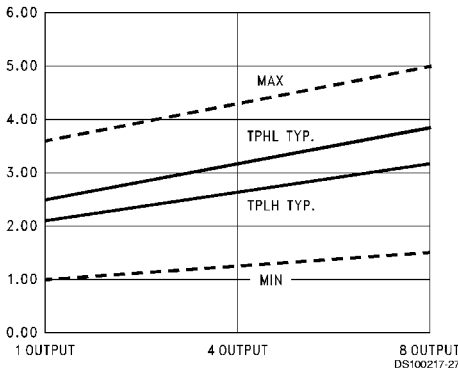
**$t_{PZH}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$



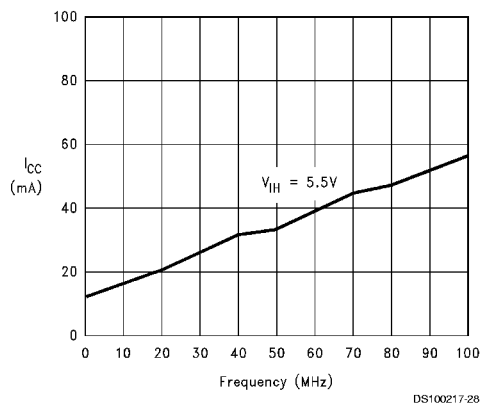
**$t_{PZL}$  vs Load Capacitance**  
 8 Outputs Switching,  $T_A = 25^\circ\text{C}$



**$t_{PLH}$  and  $t_{PHL}$  vs Number Outputs Switching**  
 $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ ,  $C_L = 50$  pF

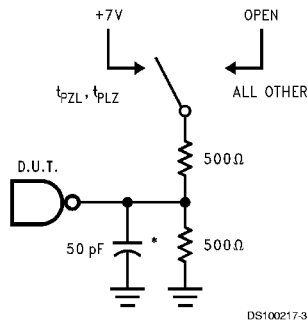


**$I_{CC}$  vs Frequency, Average,  $T_A = 25^\circ\text{C}$ , All Outputs Unloaded/Unterminated**



Dashed lines represent design characteristics; for specified guarantees refer to AC Characteristics Table.

## AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

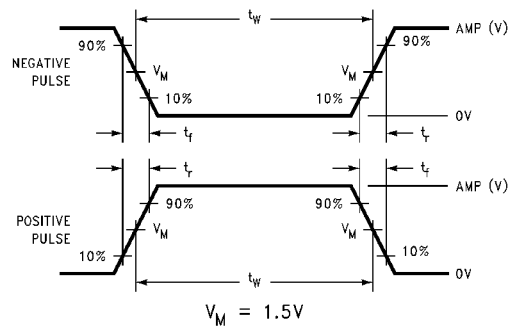


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

## AC Waveforms

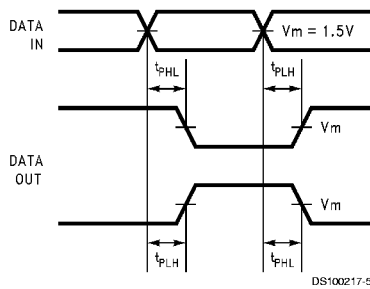


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

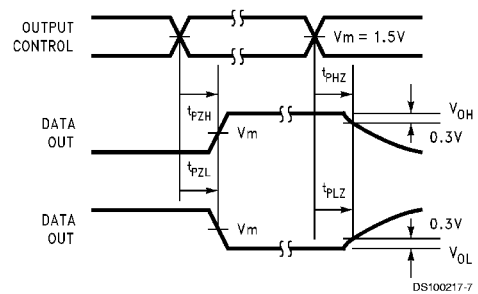
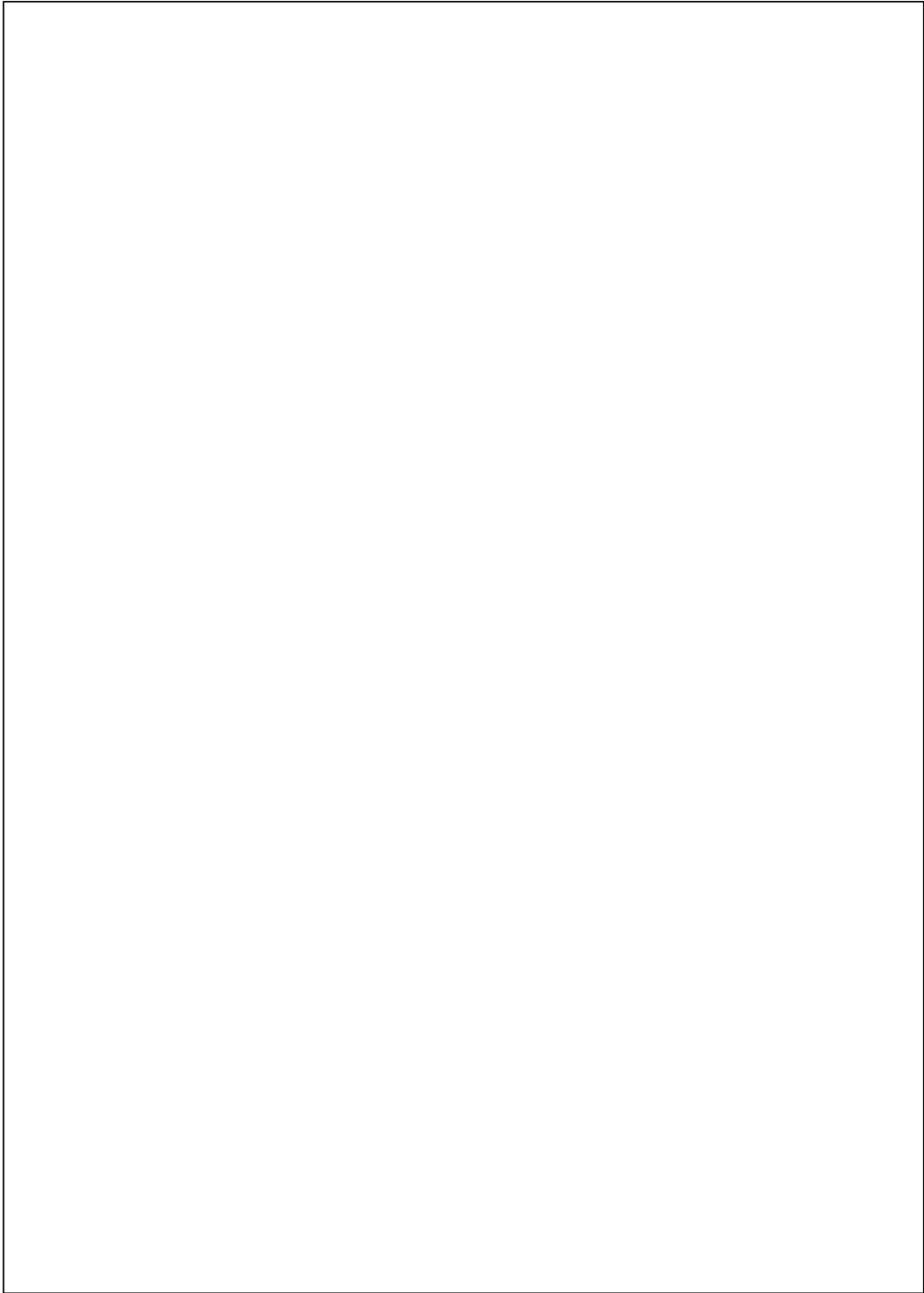
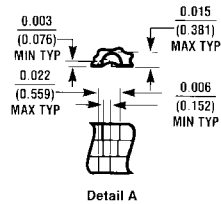
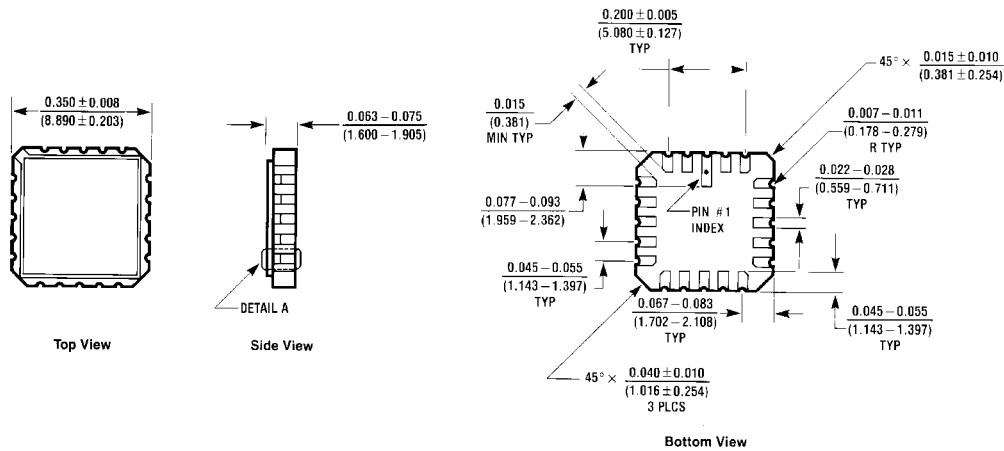


FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Time



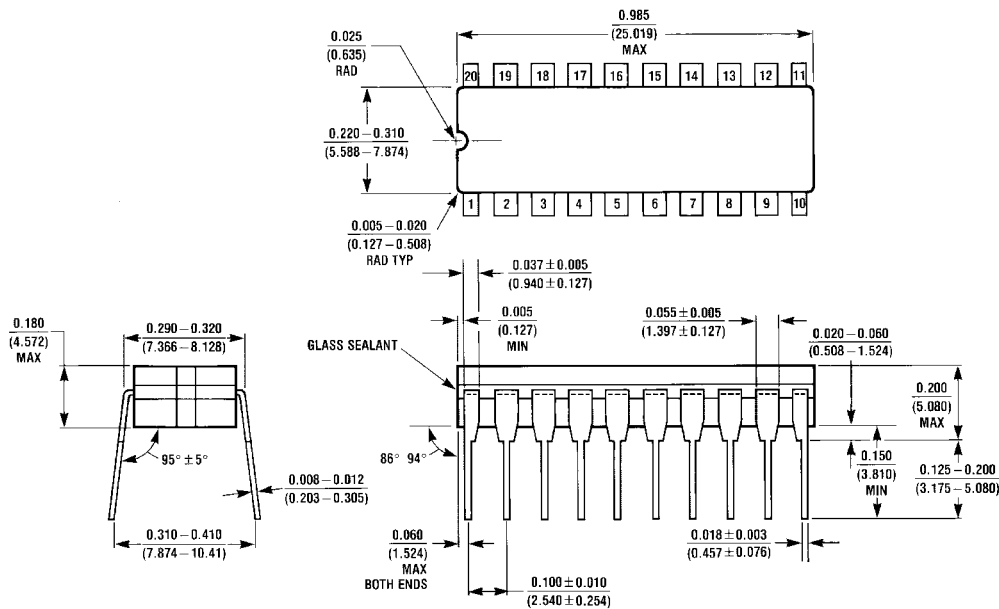


**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

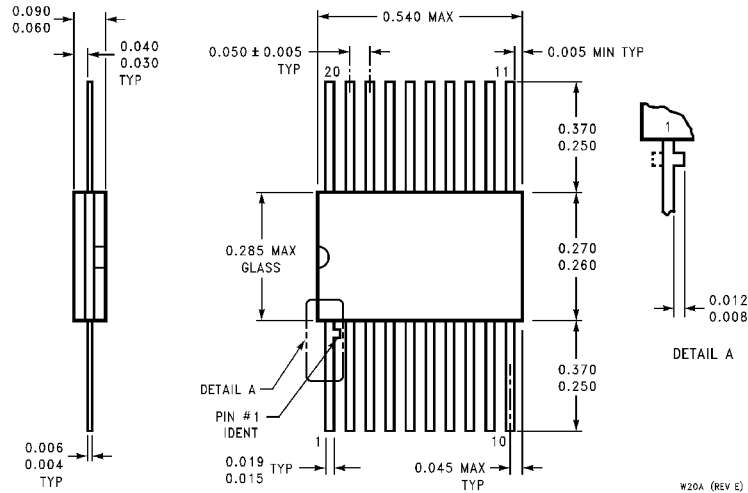
**20-Terminal Ceramic Chip Carrier**  
 NS Package Number E20A



J20A (REV M)

**20-Lead Ceramic Dual-In-Line Package**  
 NS Package Number J20A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpack  
NS Package Number W20A**

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