SRAM

512K x 8 SRAM

OUTPUT ENABLE, REVOLUTIONARY PINOUT

AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-95600
- MIL STD-883

FEATURES

- High speed: 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal .5um process
- Multiple center power and ground pins for improved noise immunity
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8, 10 and 12ns

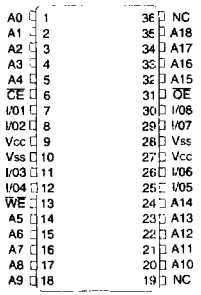
OPTIONS MARKING

• Timing		
20ns access (Contact factory)	-20	
25ns access	-25	
35ns access	-35	
• Packages		
Ceramic Flatpack	F	No. 305
Ceramic LCC	EC	No. 210
Ceramic SOJ	ECJ	No. 507
• 2V data retention/low power	L	
• Radiation Tolerant (EPI)	E	

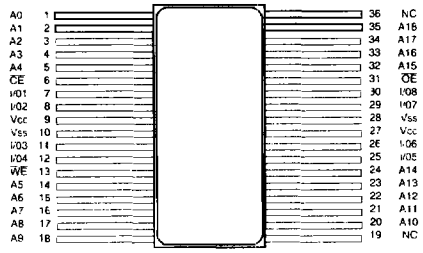
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

36-Pin LCC/SOJ



36-Pin Flat Pack



GENERAL DESCRIPTION

The AS5C512K8 is organized as 524,288 x 8 SRAM's using a four-transistor 2R memory cell with a high-speed, low-power CMOS process. ASI 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

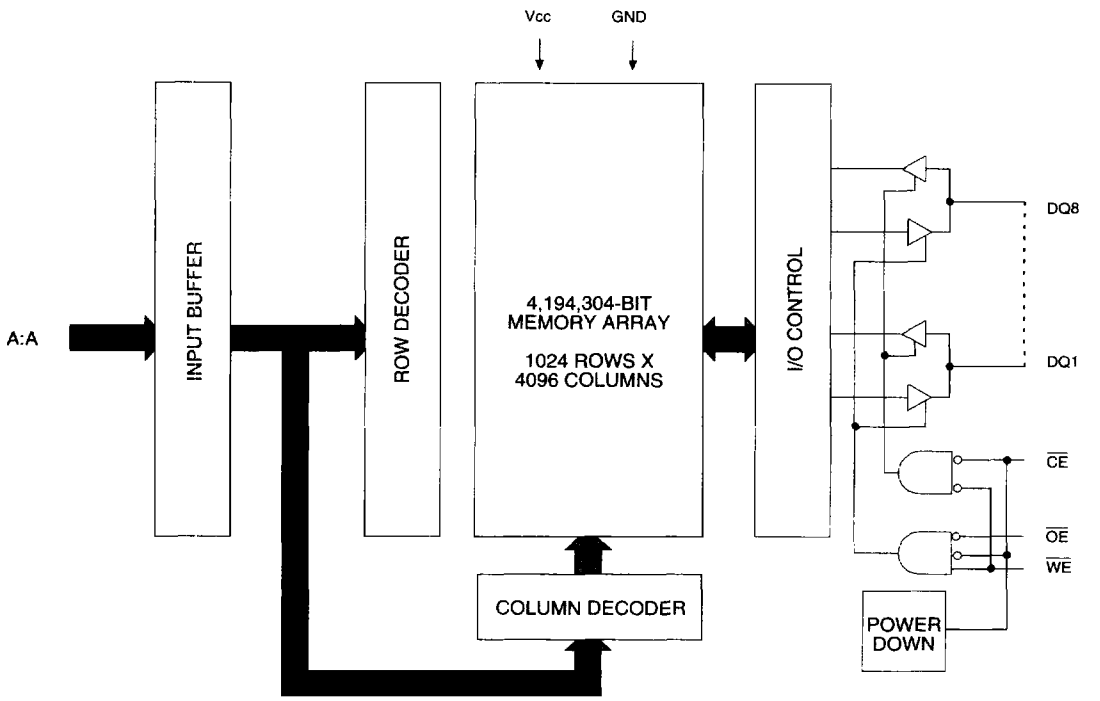
The revolutionary 36 pin version of this device offers multiple center power and ground pins for improved performance.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, ASI offers chip enable ($\overline{CE}$) and ouput enable ($\overline{OE}$) capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -.5V to +7V
Storage Temperature ..... -55°C to +150°C
Short Circuit Output Current (per I/O) 20mA
Voltage on Any Pin Relative to V_{SS} ..... -.5V to V_{CC}+1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	215	195	175	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SBT1}	60	50	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SBC}	20	20	20	mA	
	L version only		10	10	10		

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	8	pF	4
Output Capacitance		C_O	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5) (-55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle Time	tRC	20		25		35		ns	
Address access time	tAA		20		25		35	ns	
Chip Enable access time	tACE		20		25		35	ns	
Output hold from address change	tOH	2		2		2		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		3		ns	4,6,7
Chip disable to output in High-Z	tHZCE		9		10		12	ns	4,6,7
Chip Enable to power-up time	tPU	0		0		0		ns	4
Chip disable to power-down time	tPD		20		25		35	ns	4
Output Enable access time	tAOE		8		10		12	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		ns	4,6,7
Output disable to output in High-Z	tHZOE		9		10		12	ns	4,6,7
WRITE Cycle									
WRITE cycle time	tWC	20		25		35		ns	
Chip Enable to end of write	tCW	15		17		20		ns	
Address valid to end of write	tAW	15		17		20		ns	
Address setup time	tAS	0		0		0		ns	
Address hold from end of write	tAH	1		1		1		ns	
WRITE pulse width	tWP1	15		17		20		ns	
WRITE pulse width	tWP2	15		17		20		ns	
Data setup time	tDS	10		12		15		ns	
Data hold time	tDH	0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		ns	4,6,7
Write Enable to output in High-Z	tHZWE		10		12		15	ns	4,6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

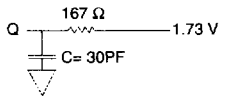


Fig. 1 OUTPUT LOAD EQUIVALENT

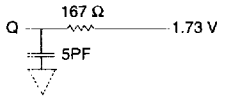


Fig. 2 OUTPUT LOAD EQUIVALENT

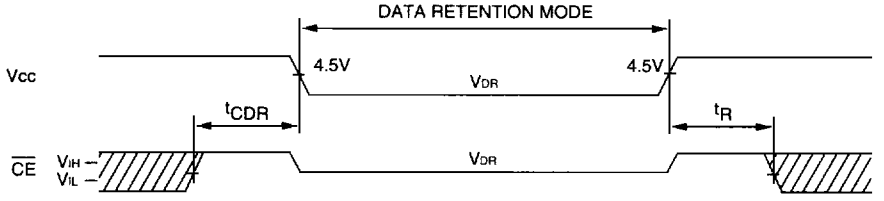
NOTES

1. All voltages referenced to Vss (GND).
2. -2V for pulse width < 20ns
3. Icc is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE , ^{t}HZWE ^{t}LZCE, ^{t}LZWE and ^{t}LZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE, and ^{t}HZ0E is less than ^{t}LZOE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable ($\overline{OE}$) is inactive (HIGH).
14. Output enable ($\overline{OE}$) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

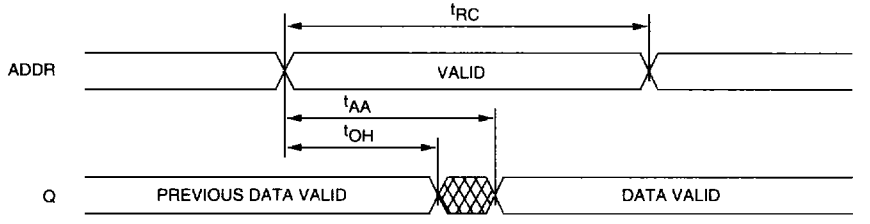
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		2	mA	
		Vcc = 3V	I_{CCDR}		4	mA	
Chip Deselect to Data Retention Time			^{t}CDR	0		ns	4
Operation Recovery Time			^{t}R	^{t}RC		ns	4, 11

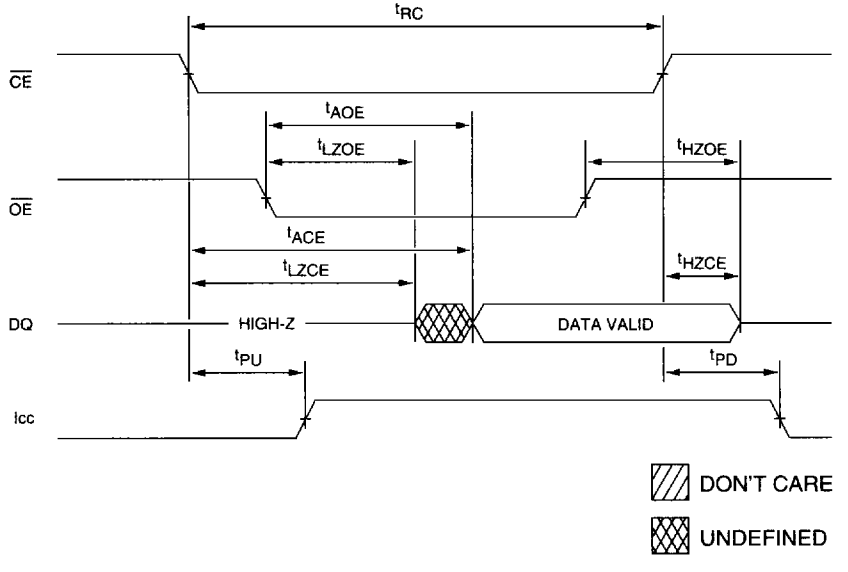
LOW Vcc DATA RETENTION WAVEFORM



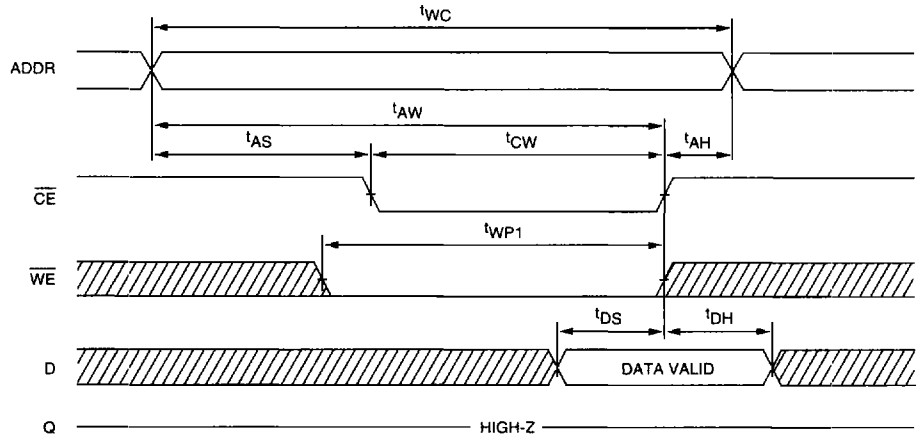
READ CYCLE NO. 1 [8, 9]



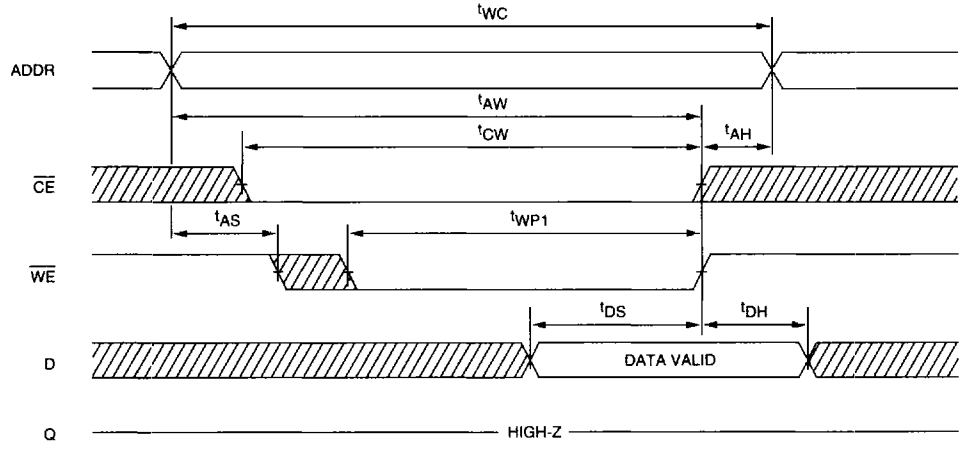
READ CYCLE NO. 2 [7, 8, 10]



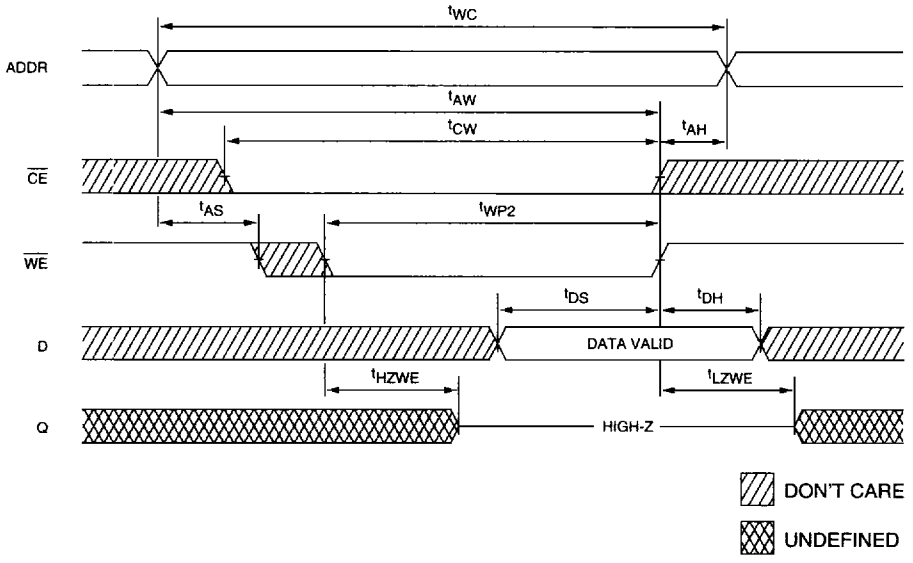
WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 14]
(Write Enable Controlled)



ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.