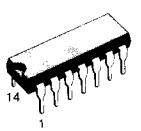
T54LS74A
T74LS74A

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

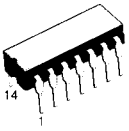
DESCRIPTION

The T54LS/T74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

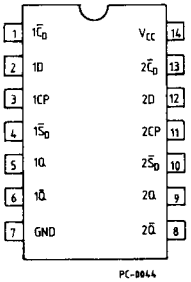
C1
Plastic Chip Carrier

ORDERING NUMBERS:

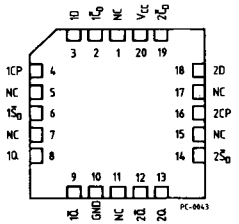
T54LS74A D2
T74LS74A D1
T74LS74A B1
T74LS74A C1
T74LS74A M1

PIN CONNECTION (top view)

DUAL IN LINE

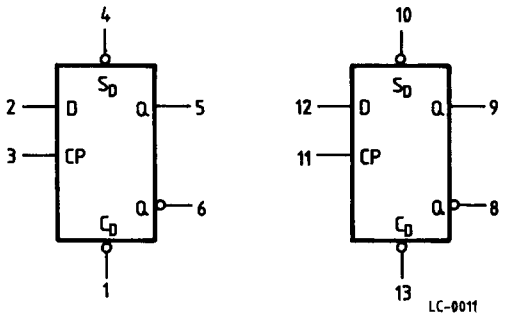


CHIP CARRIER

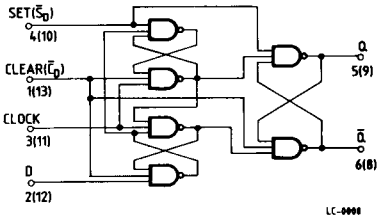


NC = No Internal Connection

LOGIC SIMBOL



LOGIC DIAGRAM AND MODE SELECT-TRUTH TABLE



OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	D	Q	$\overline{Q}$
Set	L	H	X	H	L
Reset (Clear)	H	L	X	L	H
* Undetermined	L	L	X	H	H
Load "1" (Set)	H	H	h	H	L
Load "0" (Reset)	H	H	l	L	H

* Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously. The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

H,h = HIGH Voltage Level
L,l = LOW Voltage Level
X = Don't Care
l,h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

V_{CC} = Pin 14
GND = Pin 7
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS74AD2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS74AXX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.7	3.4				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current	Data, Clock Set, Clear			20 40	V_{CC} = MAX, V_{IN} = 2.7V		μA
		Data, Clock Set, Clear			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current	Data, Clock Set, Clear			−0.4 −0.8	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX		mA
I_{CC}	Power Supply Current				8.0	V_{CC} = MAX		mA

AC CHARACTERISTICS: (T_A = 25°C)

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
f_{MAX}	Maximum Clock Frequency	25	33		Fig. 1	V_{CC} = 5.0V C_L = 15pF	MHz
t_{PLH} t_{PHL}	Clock, Clear, Set to Output		13 25	25 40	Fig. 1		ns

AC SET-UP REQUIREMENTS: T_A = 25°C

Symbol	Parameter		Limits			Test Conditions		Units
			Min.	Typ.	Max.			
t_W	Clock, Clear, Set Pulse Width		25			Fig. 3	V_{CC} = 5.0V	ns
t_s	Data Set-up Time	HIGH	25			Fig. 3		ns
		LOW	20					ns
t_h	Hold Time		5			Fig. 3		ns

Notes:

1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC WAVEFORMS

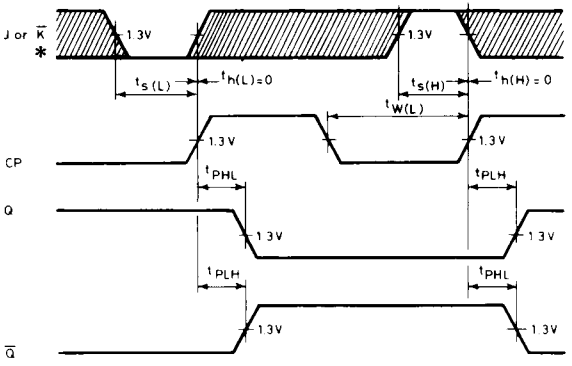


Fig. 1 Clock to Output Delays, Data Set-up and Hold Times, Clock Pulse Width

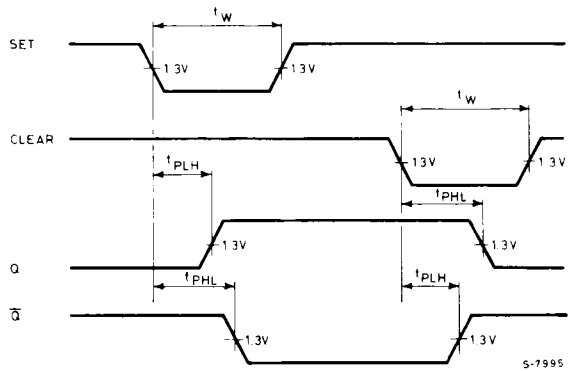


Fig. 2 Set and Clear to Ouput Delays, Set and Clear Pulse Widths

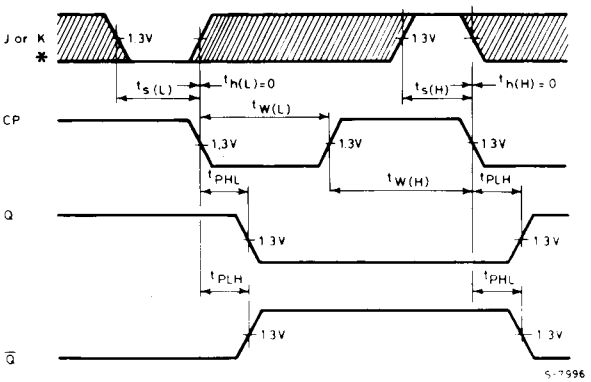


Fig. 3 Clock to Output Delays, Data Set-up and Hold times, Clock Pulse Width

* The shaded areas indicate when the input is permitted is change to predictable output performance.