N-channel enhancement mode vertical D-MOS transistor

BSN22

N AMER PHILIPS/DISCRETE 67E D

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

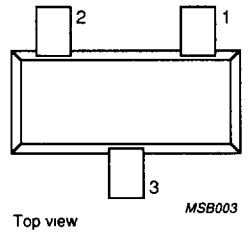
N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a surface-mounted device in general purpose small-signal fast switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	100	mA
$R_{DS(on)}$	drain-source on-resistance	50	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

PINNING

PIN	DESCRIPTION
Code: M18	
1	gate
2	source
3	drain



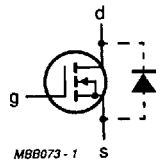


Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Transistor mounted on an FR-4 printboard.

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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	12	20	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	20	30	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	30	50	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	30	60	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	6	10	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	1	3	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	–	4	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	8	ns

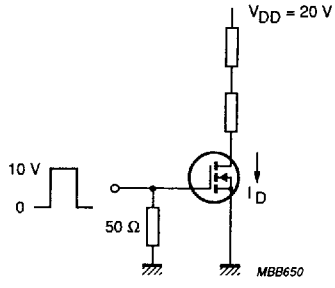

Fig.2 Switching times test circuit.

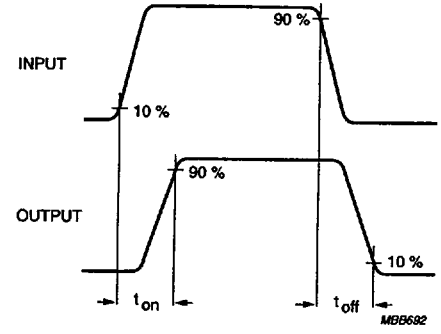

Fig.3 Input and output waveforms.