8-Bit Latch, 8-Bit Register with Inverting, 32 mA Outputs

SN74S535 SN74S536

Features/Benefits

- **Inverting outputs**
- **High-drive capability (I_{OL} = 32 mA)**
- **Three-state outputs drive bus lines**
- **20-pin SKINNYDIP® saves space**
- **8-bit data path matches byte boundaries**
- **Hysteresis improves noise margin**
- **Low current PNP inputs reduce loading**
- **Ideal for microprocessor interface**
- **Pin-compatible with SN74S533/4 — can be a direct replacement when high-drive capability is required**

Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA; also, inverting outputs instead of the standard noninverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32-mA requirements with the SN54/74365/366/367/368 hex buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive low.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
SN74S535	N,J	Com	Invert	Latch	S
SN74S536	N,J	Com		Register	

Function Tables

'S535 8-Bit Latch (Inverting)

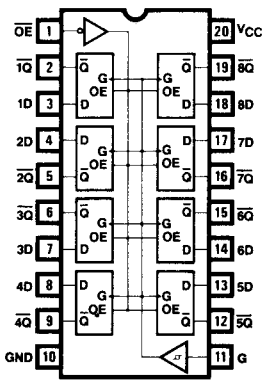
$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'S536 8-Bit Register (Inverting)

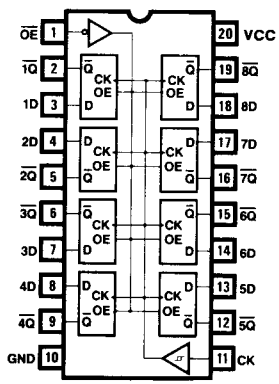
$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'S535 8-Bit Latch (Inverting)



'S536 8-Bit Register (Inverting)



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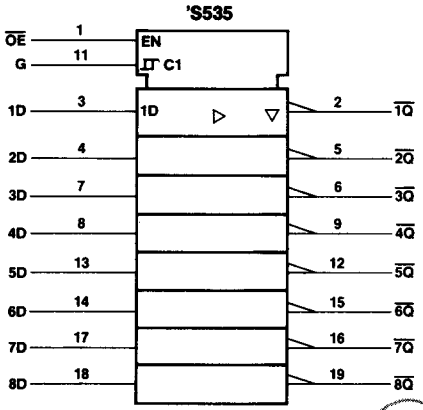
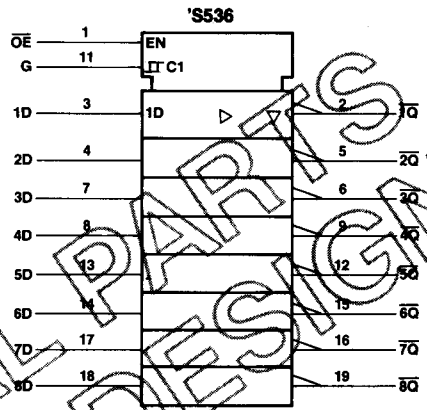
IEEE Symbols





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Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free air temperature		0		75	°C
t_w	Width of Clock/Enable	High	6	6		ns
		Low	7.3	7.3		
t_{su}	Setup time	S535	0↓	0↓		ns
		S536	5↓	5↓		
t_h	Hold time	S535	10↓	10↓		ns
		S536	5↓	2↓		

Electrical Maximum Ratings Over Operating Conditions

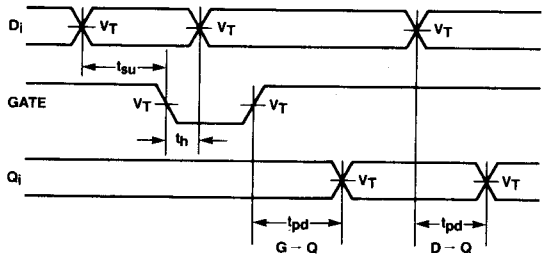
SYMBOL	PARAMETER	TEST CONDITIONS		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.5V			−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V			50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 32mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −6.5mA	2.4	3.1		V
I_{OZL}	Off-state output current	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			−50	μA
I_{OZH}			V_O = 2.4V			50	μA
I_{OS}	Output short-circuit current *	V_{CC}		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S535		105	160	mA
			S536		90	140	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

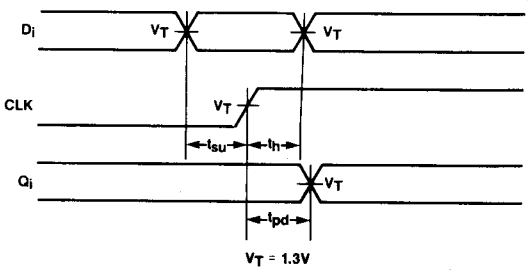
Switching Charcteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	S535 MIN	S535 TYP	S535 MAX	S536 MIN	S536 TYP	S536 MAX	UNIT
f_{MAX}	Maximum Clock frequency	C_L = 15pF R_L = 280Ω				75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Enable to output delay			12	22		11	20	ns
t_{PHL}				7	20		8	18	ns
t_{PZL}	Output Enable delay			11	20		11	20	ns
t_{PZH}				8	17		8	17	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16		7	16	ns
t_{PHZ}				6	13		5	13	ns

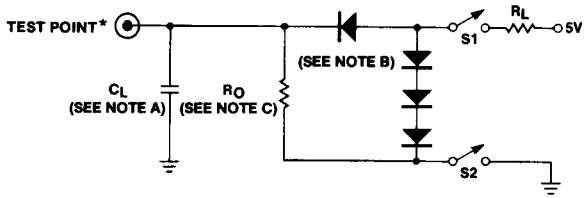
'S535 Timing Diagrams



'S536 Timing Diagrams

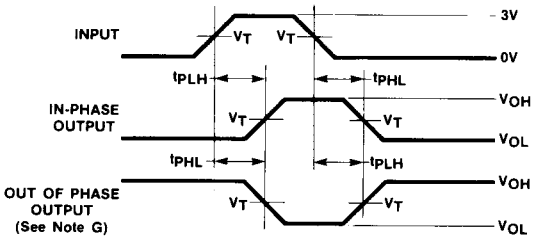


Test Load

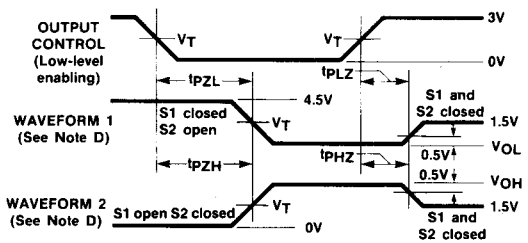


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Test Waveforms



Propagation Delay



Enable and Disable

V_T = 1.3 V

NOTES: A. C_L includes probe and jig capacitance.

B. All diodes are 1N916 or 1N3064.

C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
For Series 54/74S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.
For Series 54/74LS and PALs, t_R ≤ 15 ns. t_F ≤ 6 ns.

G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

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