

**P-Channel 20-V (D-S) MOSFET, ESD Protection**

**GENERAL DESCRIPTION**

The LT2349E is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

**FEATURES**

- $R_{DS(ON)} \leq 75m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 95m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 140m\Omega @ V_{GS} = -2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$

**APPLICATIONS**

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

**PIN CONFIGURATION**



**Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)**

Parameter		Symbol	Steady State	Unit
Drain-Source Voltage		$V_{DSS}$	-20	V
Gate-Source Voltage		$V_{GSS}$	$\pm 12$	V
Continuous Drain Current (Tj=150°C)*	$T_A = 25^\circ C$	$I_D$	-1.88	A
	$T_A = 70^\circ C$		-1.5	
Pulsed Drain Current		$I_{DM}$	-10	A
Continuous Source Current (Diode Conduction)		$I_S$	-1.7	A
Maximum Power Dissipation*	$T_A = 25^\circ C$	$P_D$	0.63	W
	$T_A = 70^\circ C$		0.4	
Operating Junction Temperature		$T_J$	-55 to 150	°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	<b>Typ</b>	90
			<b>Max</b>	125

\*The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

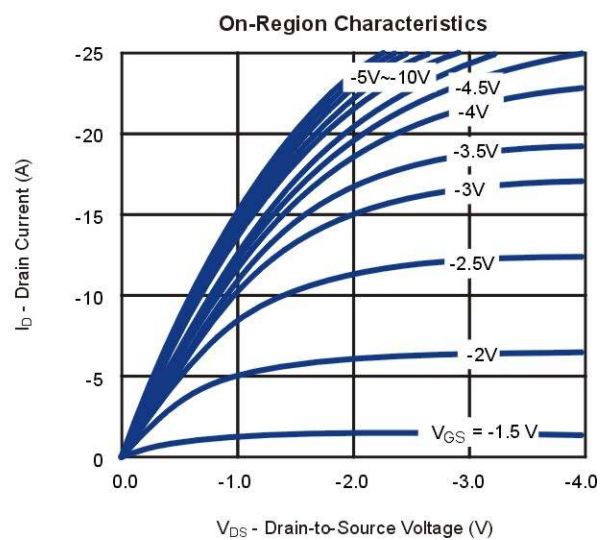
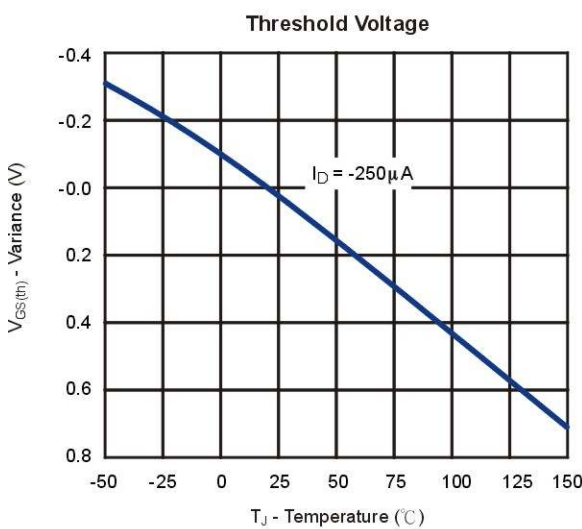
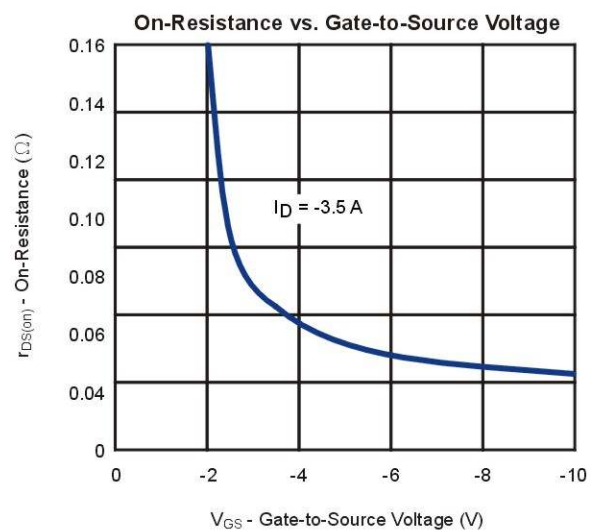
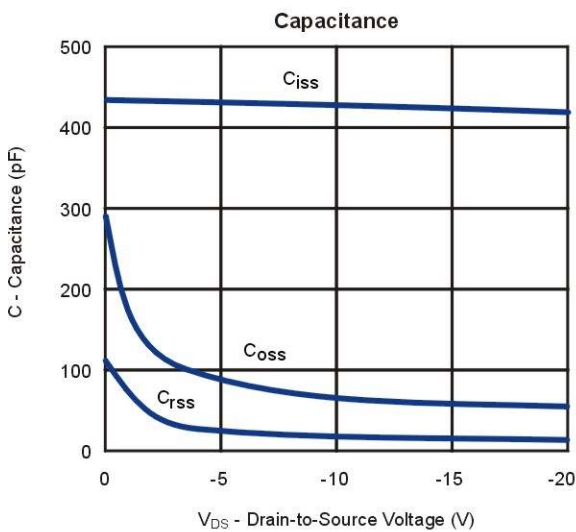
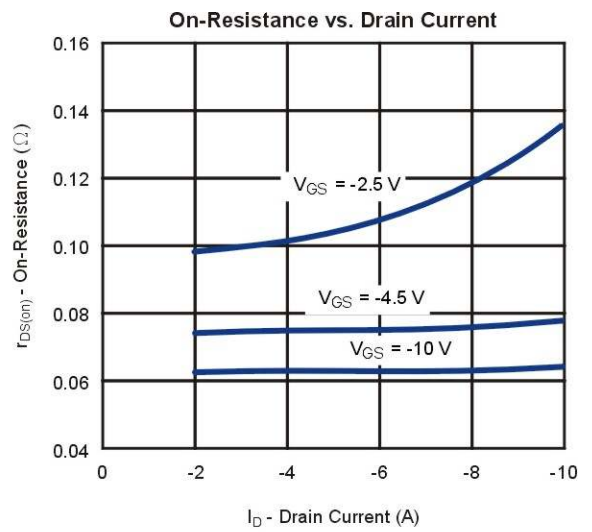
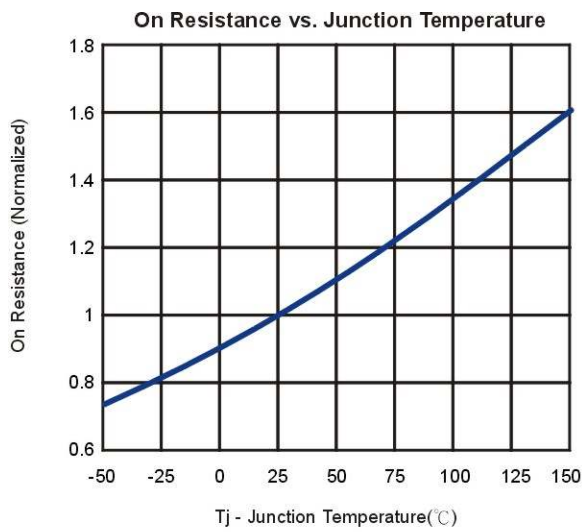
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**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$	-0.5		-1	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$			$\pm 15$	$\mu\text{A}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}$			-1	$\mu\text{A}$
		$V_{DS}=-30\text{V}, V_{GS}=0\text{V}$ $T_J=70^\circ\text{C}$			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=-2.0\text{A}$		65	75	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}, I_D=-1.3\text{A}$		75	95	
		$V_{GS}=-2.5\text{V}, I_D=-1.0\text{A}$		100	140	
$V_{SD}$	Diode Forward Voltage	$I_S=-1.7\text{A}, V_{GS}=0\text{V}$		0.8		V
<b>DYNAMIC</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=-15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		427		$\text{pF}$
$C_{oss}$	Output Capacitance			60		
$C_{rss}$	Reverse Transfer Capacitance			15		
$R_g$	Gate Resistance	$f=1\text{MHz}$		9		$\Omega$
$Q_g$	Total Gate Charge	$V_{DS}=-15\text{V}, V_{GS}=-10\text{V},$ $I_D=-20\text{A}$		6.5		$\text{nC}$
$Q_{gs}$	Gate-Source Charge			2.4		
$Q_{gd}$	Gate-Drain Charge			1.5		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15\text{V}, R_L=15\ \Omega$ $I_D=-1.0\text{A}, V_{GEN}=-10\text{V}$ $R_G=6\ \Omega$		19		$\text{ns}$
$t_r$	Turn-On Rise Time			8		
$t_{d(off)}$	Turn-Off Delay Time			43		
$t_f$	Turn-Off Fall Time			4.4		

Notes: a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

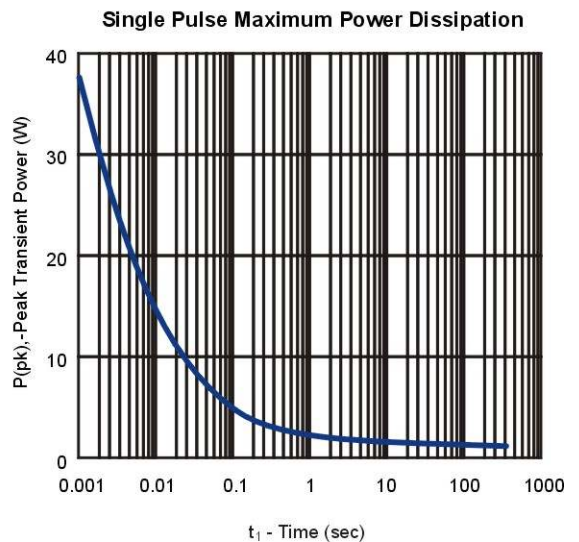
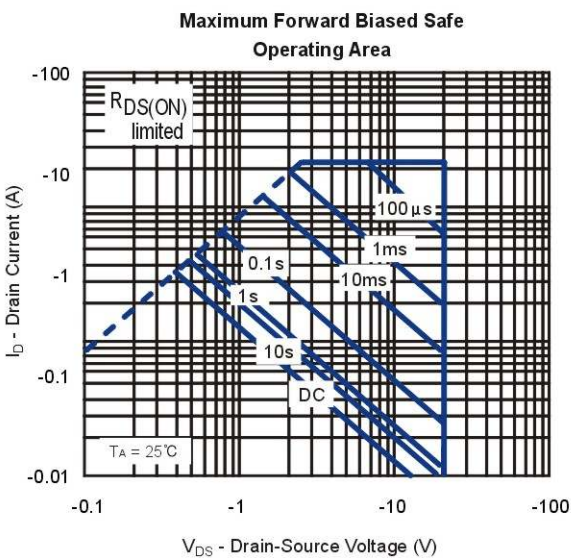
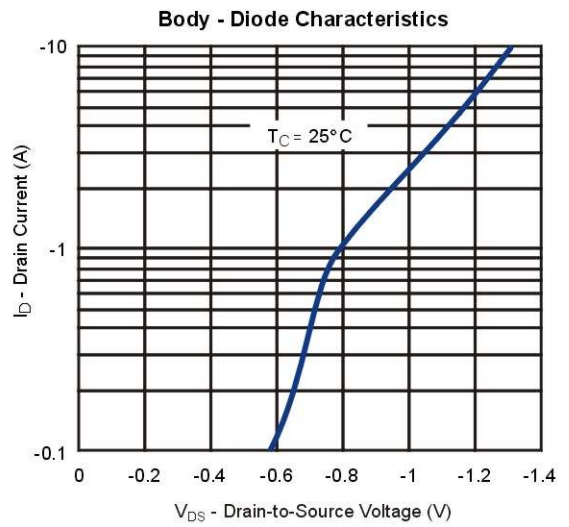
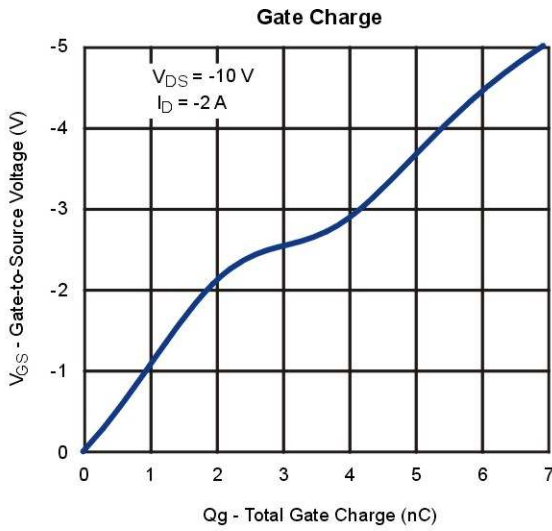
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**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

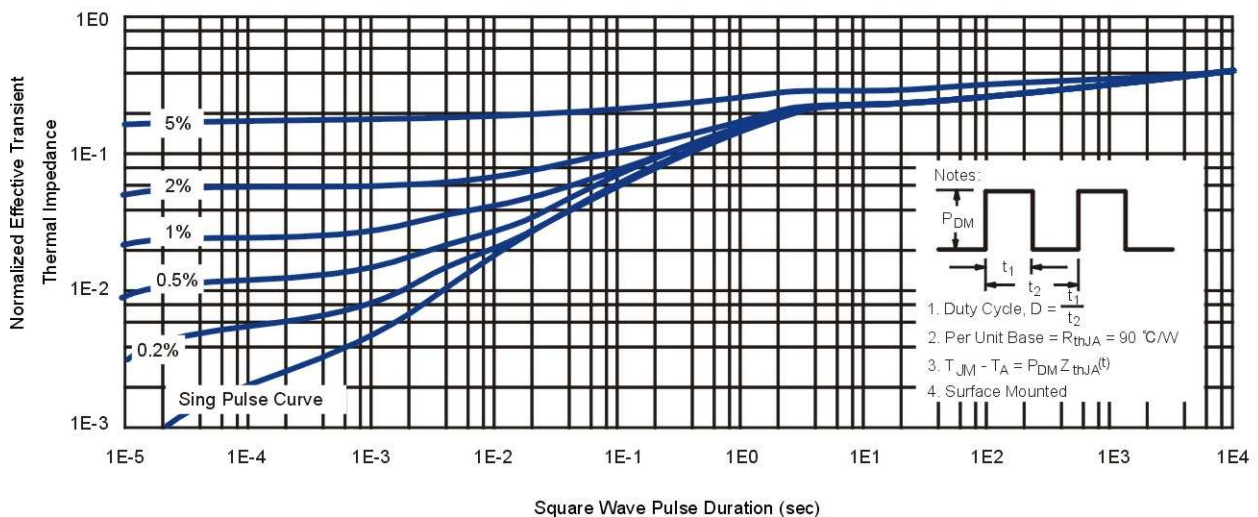


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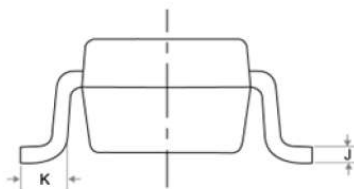
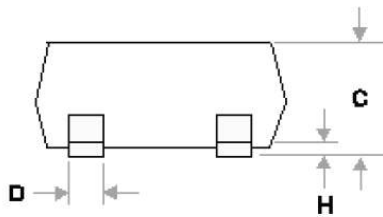
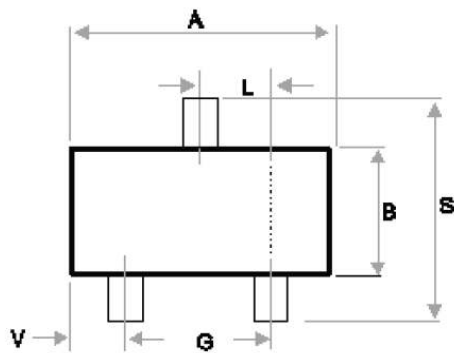


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



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**SOT-23 Package Outline**



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.80	3.00
B	1.20	1.70
C	0.90	1.30
D	0.35	0.50
G	1.78	2.04
H	0.010	0.15
J	0.085	0.20
K	0.30	0.65
L	0.89	1.02
S	2.10	3.00
V	0.45	0.60

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## **Important Notice and Disclaimer**

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