HS-7541A

CMOS 12 Bit Multiplying DAC

Features

- Improved Accuracy and Ruggedness Over The 7541
- 12 Bit Endpoint Linearity (± 1/2 LSB)
- Improved Gain Error: ± 1 LSB (No User Adjustment Required)
- Low Gain Tempco (5 ppm/°C Max)
- 2 and 4 Quadrant Multiplication
- Superior Power Supply Rejection.
- Low Feedthrough Error and Digital Charge Injection.
- Low Power Consumption.
- TTL/CMOS Compatible
- All Data Input Pins Designed To withstand 200IV ESD
- Direct Replacement for AD 7541 and AD 7541 A.

Applications

- Programmable Amplifiers
- Function Generators
- Digitally Controlled Attenuators
- Digitally Controlled Power Supplies
- Digital Filters
- Digital/Synchro Conversion
- Ratiometric A/D Conversion
- CRT Graphics Generator

Description

The HS-7541A is a 12-Bit, 4 quadrant multiplying digital-to-analog converter contained in a single high density monolithic CMOS chip. It is manufactured using an advanced oxide isolated, silicon-gate, monolithic CMOS technology.

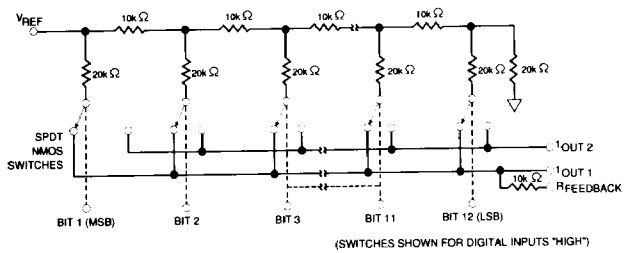
The HS-7541A features circuitry designed to protect data inputs against damage from 2001 volt electrostatic discharge.

The HS-7541A consists of a highly stable thin-film R-2R ladder network and twelve NMOS current switches on a monolithic chip. The thin-film resistors are laser trimmed to provide true 12 Bit linearity and excellent absolute linearity. The NMOS switches are temperature compensating and their "ON" resistances are binarily scaled so that the voltage drop across each switch is identical. This is essential in maintaining the accuracy of the binarily weighted current division performed by the ladder network. The internal feedback resistor used in the output current-to-voltage conversion operation is matched to the R-2R ladder.

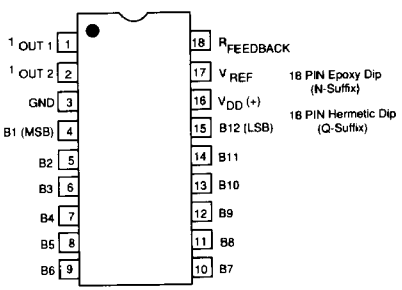
The HS-7541A is a superior pin-compatible replacement for the industry standard 7541 and the AD7541A. Available in standard Epoxy and CERDIP packages, the HS-7541A is compatible with automatic insertion equipment. The improved performance of the HS-7541A permits upgrading existing designs with greater ruggedness and accuracy. Tight linearity and gain error specifications may permit reduced system parts count by eliminating trimming circuitry.

7

Functional Diagram



Pin Connections



HS-7541A

CMOS 12-Bit Multiplying DAC

Absolute Maximum Ratings

(T_A=+25°C, unless otherwise noted)

V_{DD} (to GND)	+17V
V_{REF}(to GND)	±25V
V_{RFB}(to GND)	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	-0.3V, to V_{DD}
Power Dissipation (Package)	450mW
Derate Above +75°C	6mW/°C

Operating Temperature Range (T_A = Full)		
Commerical	(KN ,LN GRADES)	0° C to 70°C
Industrial	(BQ, CQ GRADES)	-25°C to +85°C
Military	(TQ, UQ GRADES)	-55°C to +125°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 Sec)	+300°C

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
Use proper ESD handling procedures

Electrical Characteristics:

V_{DD}=+15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V; T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity	INL				± 1/2	LSB
Differential NonLinearity	DNL	HS-7541A - KN/BQ/TQ			± 1/2	LSB
		HS-7541A - JN/AQ/SQ			± 1	LSB
Gain Error	G_{FSE}	Using Internal Feedback Resistor				
		HS-7541A - KN/BQ/TQ				
		T_A = 25°C			1	LSB
		T_A = Full			2	LSB
		HS-7541A - JN/AQ/SQ				
		T_A = 25°C			2	LSB
		T_A = Full			3	LSB
GAIN TEMPCO (Δ Gain/Δ Temp.)	TC_{GFS}			± 2	± 5	PPM/°C
Power Supply Rejection Ratio (Δ Gain/ Δ V_{DD})	PSRR	T_A = 25°C, Δ V_{DD} = ±5%			±0.001	%/%
		T_A = Full, ΔV_{DD} = ±5%			±0.002	%/%
Output Leakage Current	I_{LKG}	For I_{OUT1} Digital Inputs = V_{IL}				
		HS-7541A - KN/BQ/TQ				
		T_A = 25°C			5	NA
		T_A = Full			10	NA
		HS-7541A - JN/AQ/SQ				
		T_A = 25°C			5	NA
		T_A = Full			100	NA
Zero Scale Error	I_{ZSE}	V_{REF}=+10V, all digital inputs=0V				
		HS-7541A - KN/BQ/TQ				
		T_A=25°C		0.002		LSB
		T_A=Full		0.01		LSB
		HS-7541A- JN/AQ/SQ				
		T_A=°25C		0.002		LSB
		T_A=Full		0.05		LSB

Electrical Characteristics:

V_{DD}=+15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V; T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Reference Input						
Input Resistance	R_{PEF}		7	11	15	kΩ
Input Resistance Tempco (Δ R/ΔT)	TC R-REF			50		ppm/°C
Power Supply						
Supply Current	I_{DD}	Digital Inputs = V_{IL} OR V_{IH} Digital Inputs = 0V or V_{DD}		100	2 μA	ma
Digital Input						
Digital Input High	V_{IH}		2.4			V
Digital Input Low	V_{IL}				0.8	V
Input Leakage Current	I_{IL}	T_A = 25°C T_A = Full		±1	 ±1	NA μA
Input Capacitance	C_{IN}	V_{IN} = 0V			8	PF
Dynamic Performance						
Propagation Delay	T_{PD}	I_{OUT} LOAD = 100Ω, C_{EXT} = 13 PF, Measured Fom Digital Input Change to 90% Of Final Analog Output, T_A = 25°C		100	150	NS
Output Current Settling Time	T_S	To ± 1/2 LSB, T_A = 25°C Extrapolated Measurement		0.6	1	μS
Feedthrough Error (V_{REF} to I_{OUT})	FT	V_{REF} = 20 V_{PP} @ f = 10 kHz All Digital Inputs Low TA = 25°C		2	5	mV_{P-P}
Digital To Analog Glitch Energy	Q	V_{REF} = 0V, All Digital Inputs = 0V To V_{DD} Or V_{DD} To 0V, T_A = 25°C		700	1000	NVS
Analog Outputs						
Output Capacitance	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IH} Digital Inputs = V_{IL} Digital Inputs = V_{IH} Digital Inputs = V_{IL}		85 30 30 85	120 50 50 120	PF PF PF PF

7

Circuit Description

General

The HS7541A is a 12-bit multiplying D/A converter consisting of a highly stable, silicon-chrome thin film R-2R resistor ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the HS754A1 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R2-R ladder's terminating resistor. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection) V_{DD} must be present to turn "ON" these series switches.

2001 ESD Protection

In the design of the HS-7541A's data inputs, 2001 V ESD resistance has been incorporated through careful layout and the inclusion of input protection circuitry.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are LOW and $I_{OUT\,1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore varied between the low and high values.

Output Impedance

The output resistance, as in the case of the output capacitance,varies with the digital input code. The resistance, looking back into the $I_{OUT\,1}$ terminal, may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations.

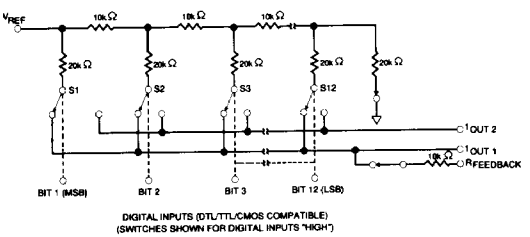


FIGURE 1: Simplified DAC Circuit

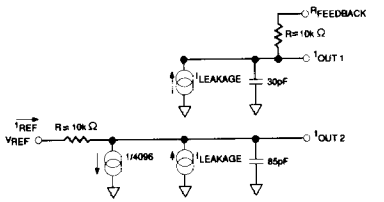


FIGURE 2: HS-7541A Equivalent Circuit
(All Inputs Low)

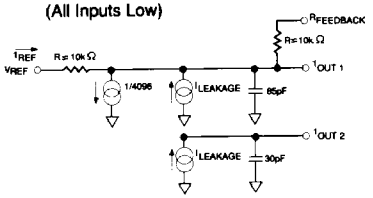


FIGURE 3: HS-7541A Equivlalent Circuit
(All Inputs High)

Application Information

Unipolar Operation

The connections required for digital unipolar operation are shown in Figure 4. The reference voltage V_{REF} may be either positive or negative. The 2kΩ potentiometer in the V_{REF} line and the 1kΩ resistor in the feedback loop are optional and are only needed when the gain error must be trimmed to less than 0.3% F.S.R. They should track each other to better than 0.1%, but don't have to track 7541's internal network resistors.

As shown in Figure 4 the DAC current output is typically connected to an external OP-AMP with it's non-inverting input tied to ground. The amplifier selected should have a low input bias current and low drift over temperature. To maintain specified HS7541 linearity, the amplifiers input offset voltage should be nulled to less than ±200μV (o.1LSB). Table 1 shows the code table for unipolar operation.

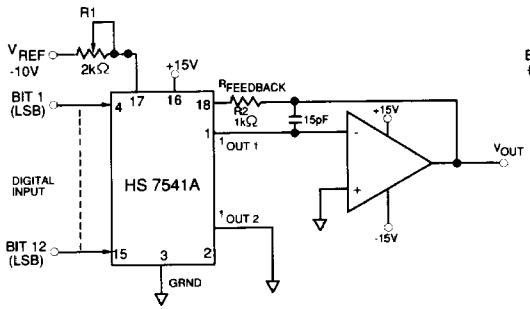


FIGURE 4: Unipolar Operation

Bipolar Operation

The connections required for bipolar operation are shown in Figure 5. The digital input is offset binary coded and produces an output according to the code table shown in Table 2.

As in the case of unipolar operation the gain trim resistors can be omitted in applications that do not require minimum gain error. Amplifier considerations of low input bias current, low drift and offset nulling are also applicable for bipolar operation.

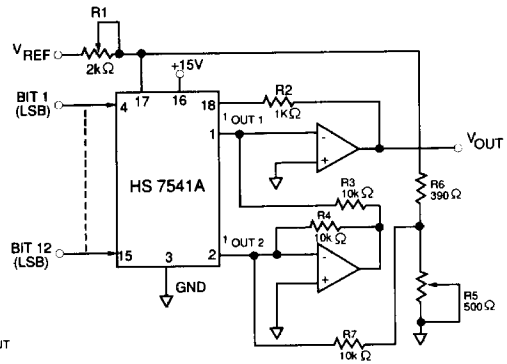


FIGURE 5: Bipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99975 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.50000V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	-0.49975 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	0

TABLE 1: Unipolar Operation Code Table

DITGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99951 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.00049V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	+0.50000 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	+1.00000 V_{REF}

TABLE 2: Bipolar Operation Code Table

Ordering Information

PART #	PACKAGE	T_A-TEMP RANGE (°C)	RELATIVE ACCURACY (LSB's)	GAIN ERROR (LSB's)
HS-7541A JN	20-Pin Epoxy Dip	0 to 70	± 1/2	± 3
HS-7541A KN	20-Pin Epoxy Dip	0 to 70	± 1/2	± 2
HS-7541A AQ	20-Pin Hermetic Cerdip	-25 to 85	± 1/2	± 3
HS-7541A BQ	20-Pin Hermetic Cerdip	-25 to 85	± 1/2	± 2
HS-541A SQ	20-Pin Hermetic Cerdip	-55 to 125	± 1/2	± 3
HS-541A TQ	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 2
HS-7541A SQ/883	20-Pin Hermetic Cerdip	-55 to125	+1/2	± 3
HS-7541A TQ/883	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 2

NOTES: 1) Consult Factory For 883 Data Sheet
2) Package Designations: Suffix N-Plastic Dip, Suffix Q-Hermetic Dip. For package mechanical dimensions, call DataLinear at (408) 945-9080.

CROSS REFERENCE INFORMATION

ADI Part No.	DataLinear Part No.
AD 7541A JN	HS 7541A JN
AD 7541A KN	HS 7541A KN
AD 7541A AD	HS 7541A AQ
AD 7541A BD	HS 7541A BQ
AD 7541A SD	HS 7541A SQ
AD 7541A TD	HS 7541A TQ
AD 7541A SD/883	HS 7541A SQ/883
AD 7528A TD/883	HS 7541A TQ/883