



SANYO Semiconductors DATA SHEET

ECH8503 — PNP Epitaxial Planar Silicon Transistor Motor Drive Applications

Features

- Composite type, facilitating high-density mounting
- Mounting height 0.9mm
- Halogen free compliance

Specifications

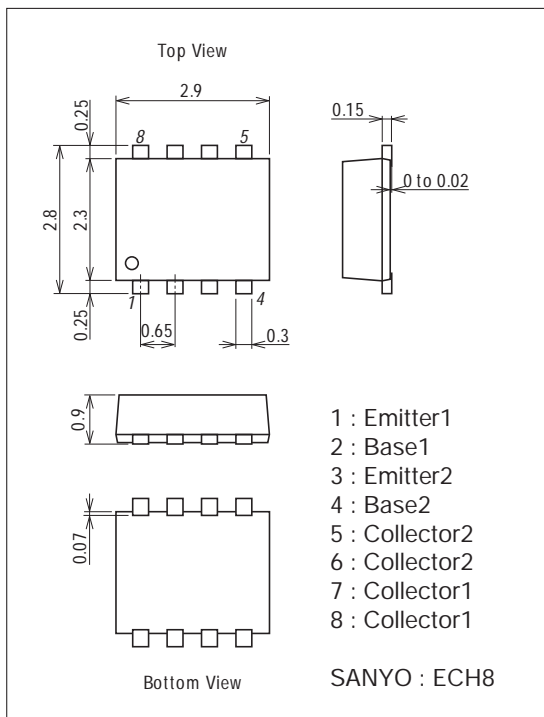
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V _{CB0}		-50	V
Collector-to-Emitter Voltage	V _{CE0}		-50	V
Emitter-to-Base Voltage	V _{EB0}		-6	V
Collector Current	I _C		-5	A
Collector Current (Pulse)	I _{CP}		-10	A
Base Current	I _B		-1	A
Collector Dissipation	P _C	When mounted on ceramic substrate (900mm ² ×0.8mm) 1unit	1.3	W
Total Dissipation	P _T	When mounted on ceramic substrate (900mm ² ×0.8mm)	1.6	W
Junction Temperature	T _J		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Package Dimensions

unit : mm (typ)

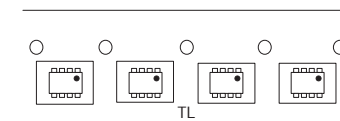
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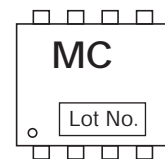
Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

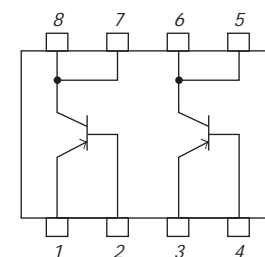
Taping Type : TL



Marking



Electrical Connection

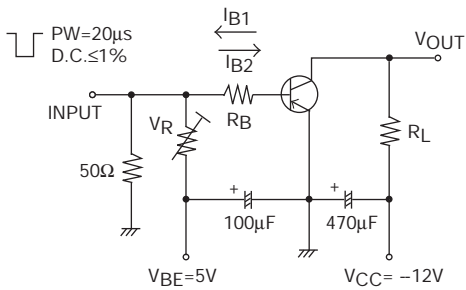


Electrical Characteristics at Ta=25°C

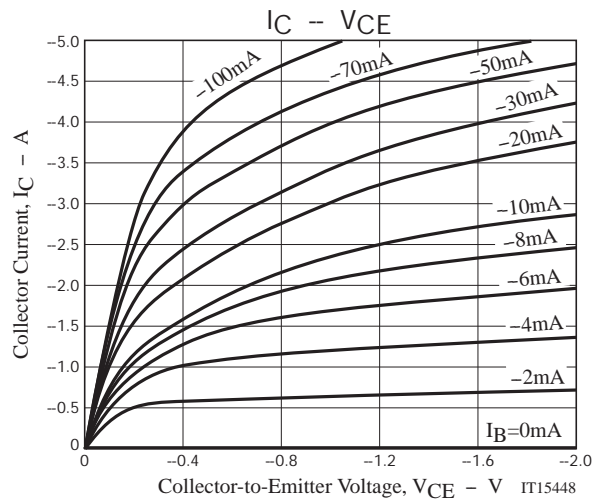
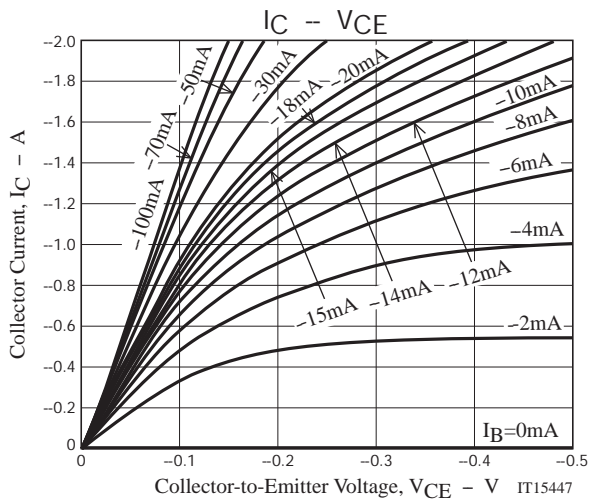
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	ICBO	V _{CB} = -50V, I _E = 0A			-0.1	μA
Emitter Cutoff Current	I _{EBO}	V _{EB} = -4V, I _C = 0A			-0.1	μA
DC Current Gain	h _{FE}	V _{CE} = -2V, I _C = -500mA	200		560	
Gain-Bandwidth Product	f _T	V _{CE} = -10V, I _C = -500mA		280		MHz
Output Capacitance	C _{ob}	V _{CB} = -10V, f = 1MHz		42		pF
Collector-to-Emitter Saturation Voltage	V _{CE(sat)1}	I _C = -1A, I _B = -50mA		-60	-100	mV
	V _{CE(sat)2}	I _C = -2.5A, I _B = -125mA		-110	-190	mV
Base-to-Emitter Saturation Voltage	V _{BE(sat)}	I _C = -2.5A, I _B = -125mA		-0.9	-1.1	V
Collector-to-Base Breakdown Voltage	V _{(BR)CBO}	I _C = -10μA, I _E = 0A	-50			V
Collector-to-Emitter Breakdown Voltage	V _{(BR)CEO}	I _C = -1mA, R _{BE} = ∞	-50			V
Emitter-to-Base Breakdown Voltage	V _{(BR)EBO}	I _E = -10μA, I _C = 0A	-6			V
Turn-On Time	t _{on}	See specified Test Circuit.		30		ns
Storage Time	t _{stg}	See specified Test Circuit.		170		ns
Fall Time	t _f	See specified Test Circuit.		17		ns

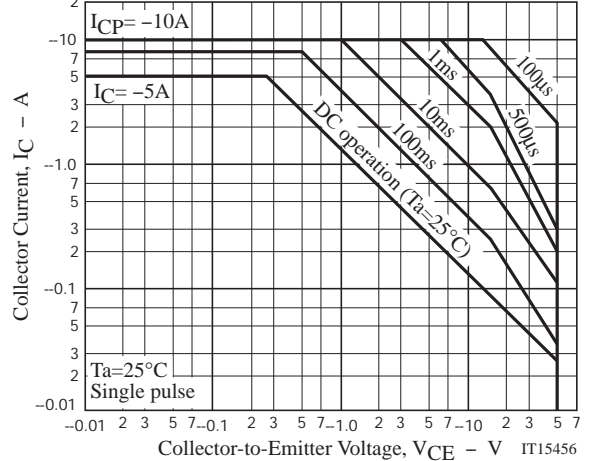
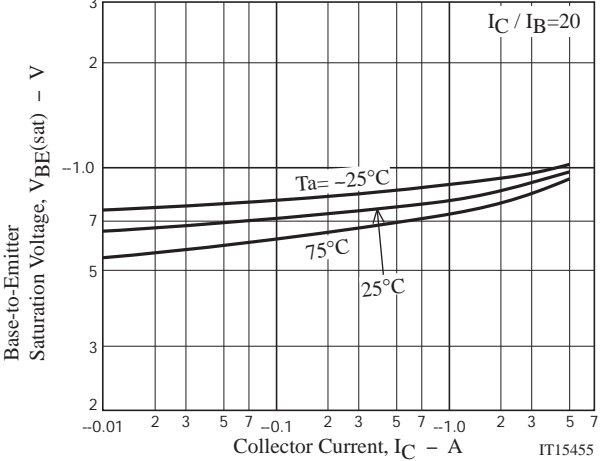
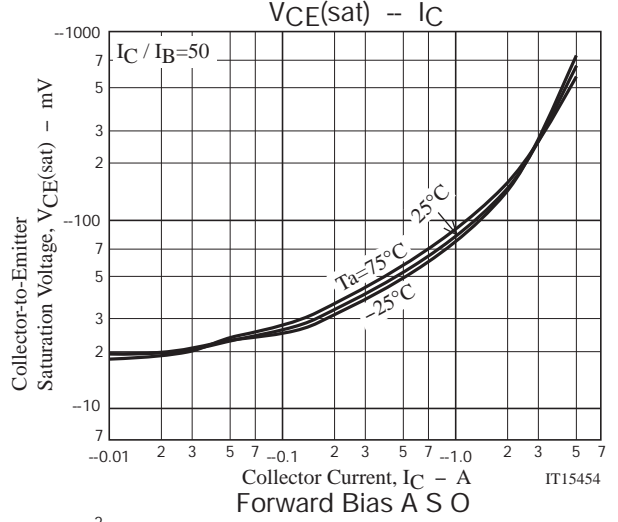
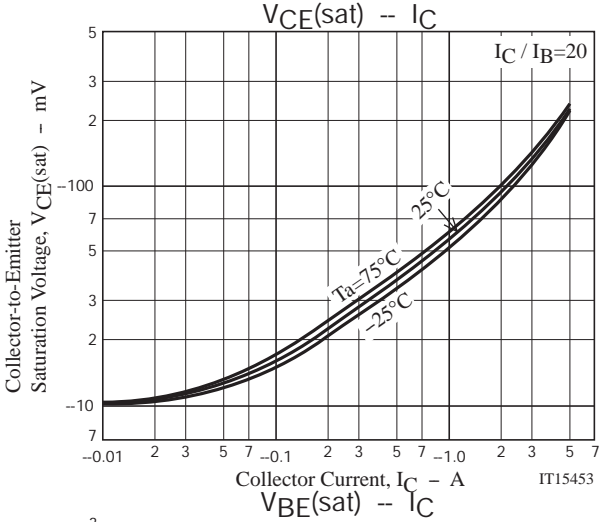
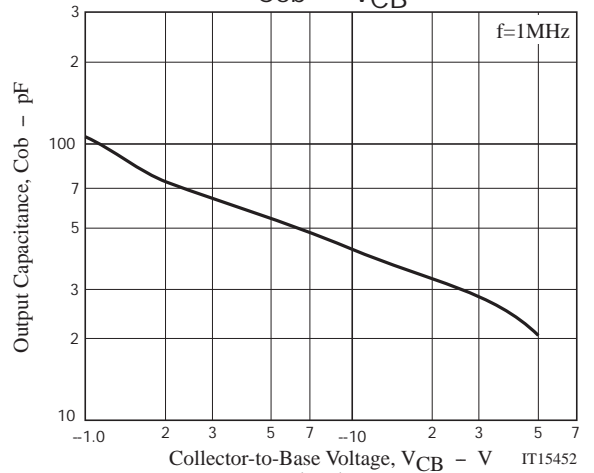
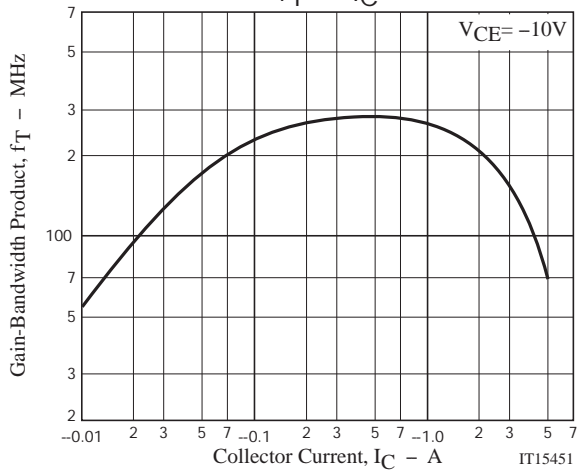
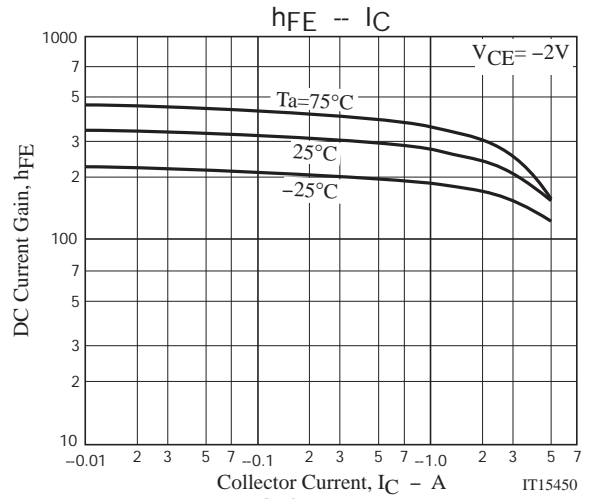
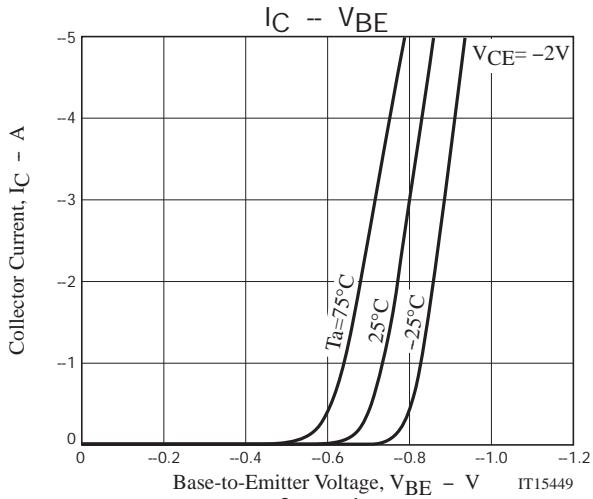
Note) The specifications shown above are for each individual transistor.

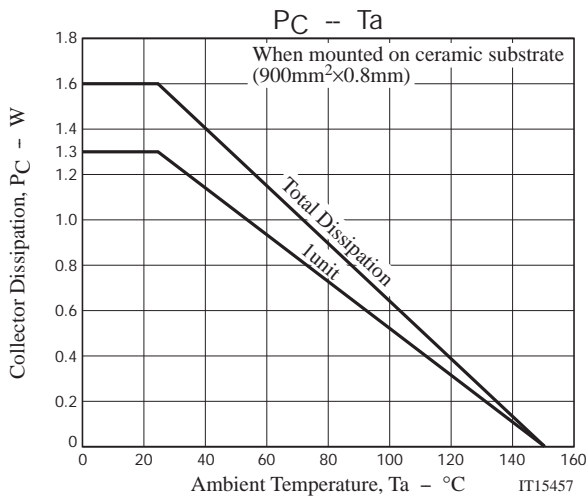
Switching Time Test Circuit



$$I_C = -20I_{B1} = 20I_{B2} = -2.5A$$







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