# MC54/74HC257

T-67-21-51

# Quad 2-Input Data Selector/ Multiplexer with 3-State Outputs

## High-Performance Silicon-Gate CMOS

The MC54/74HC257 is identical in pinout to the LS257. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device selects a (4-bit) nibble from either the A or B inputs as determined by the Select input. The nibble is presented at the outputs in noninverted form when the Output Enable pin is at a low level. A high level on the Output Enable pin switches the outputs into the high-impedance state.

The HC257 is similar in function to the HC157 which do not have 3-state outputs.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 108 FETs or 27 Equivalent Gates

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

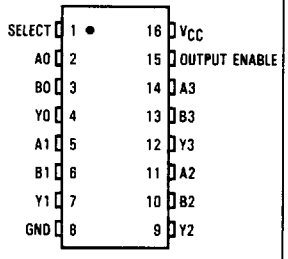
D SUFFIX
SOIC
CASE 751B-04

### ORDERING INFORMATION

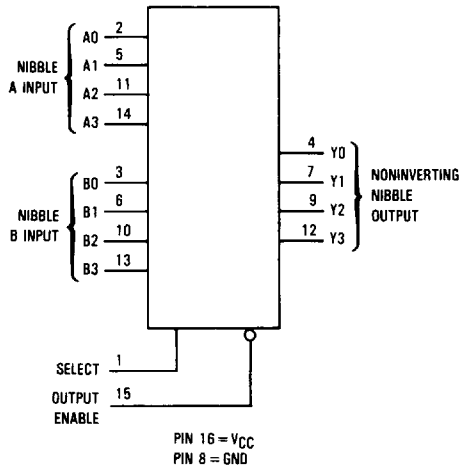
| | |
|---|---|
| MC74HCXXXN | Plastic |
| MC54HCXXXJ | Ceramic |
| MC74HCXXXD | SOIC |

$T_A$ = −55° to 125°C for all packages.
Dimensions in Chapter 6.

### PIN ASSIGNMENT




### LOGIC DIAGRAM




### FUNCTION TABLE

| Inputs | | Outputs |
|---|---|---|
| Output Enable | Select | Y0-Y3 |
| H | X | Z |
| L | L | A0-A3 |
| L | H | B0-B3 |

X = don't care
Z = high-impedance state
A0-A3, B0-B3 = the levels of the respective Nibble Inputs.

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# MC54/74HC257

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −1.5 to $V_{CC}$+1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | −0.5 to $V_{CC}$+0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±35 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±75 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic or Ceramic DIP† | 750 | mW |
| | SOIC Package† | 500 | |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | | °C |
| | (Plastic DIP or SOIC Package) | 260 | |
| | (Ceramic DIP) | 300 | |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $GND \le (V_{in} \text{ or } V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 4.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time | $V_{CC}$=2.0 V | 0 | 1000 | ns |
| | (Figure 1) | $V_{CC}$=4.5 V | 0 | 500 | |
| | | $V_{CC}$=6.0 V | 0 | 400 | |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $V_{IH}$ | Minimum High-Level Input Voltage | $V_{out}$=0.1 V or $V_{CC}$−0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| $V_{IL}$ | Maximum Low-Level Input Voltage | $V_{out}$=0.1 V or $V_{CC}$−0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{in}$=$V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 6.0$ mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | $\|I_{out}\| \le 7.8$ mA | 6.0 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum Low-Level Output Voltage | $V_{in}$=$V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{in}$=$V_{IH}$ or $V_{IL}$ $\|I_{out}\| \le 6.0$ mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | $\|I_{out}\| \le 7.8$ mA | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$=$V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three-State Leakage Current | Output in High-Impedance State<br>$V_{in}$=$V_{IL}$ or $V_{IH}$<br>$V_{out}$=$V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$=$V_{CC}$ or GND<br>$I_{out}$=0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 4.

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**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | 25°C to −55°C | ≤85°C | ≤125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Nibble A or B to Output Y (Figures 1 and 4) | 2.0 | 100 | 125 | 150 | ns |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Select to Output Y (Figures 2 and 4) | 2.0 | 100 | 125 | 150 | ns |
| | | 4.5 | 20 | 25 | 30 | |
| | | 6.0 | 17 | 21 | 26 | |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0 | 150 | 190 | 225 | ns |
| | | 4.5 | 30 | 38 | 45 | |
| | | 6.0 | 26 | 33 | 38 | |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 | 60 | 75 | 90 | ns |
| | | 4.5 | 12 | 15 | 18 | |
| | | 6.0 | 10 | 13 | 15 | |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three-State Output Capacitance (Output in High-Impedance State) | — | 15 | 15 | 15 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

| | | | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)<br>Used to determine the no-load dynamic power consumption:<br>$P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$<br>For load considerations, see Chapter 4. | Typical @ 25°C, $V_{CC}$ = 5.0 V<br>39 | pF |

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (PINS 2, 5, 11, 14)** — Nibble A input. The data present on these pins is transferred to the output when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (PINS 3, 6, 10, 13)** — Nibble B input. The logic data present on these pins is transferred to the output when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12)** — Nibble output. The selected nibble input is presented at these outputs when the Output Enable input is at a low level. For the Output Enable input at a high level, the outputs are switched to the high impedance state.

### CONTROL INPUTS

**SELECT (PIN 1)** — Nibble select. This input determines the nibble to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**OUTPUT ENABLE (PIN 15)** — Output Enable. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input forces the outputs into the high-impedance state.

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## SWITCHING WAVEFORMS

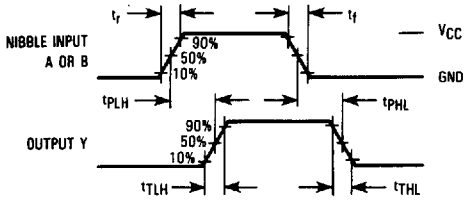



Figure 1.

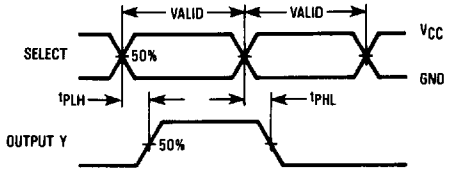



Figure 2.

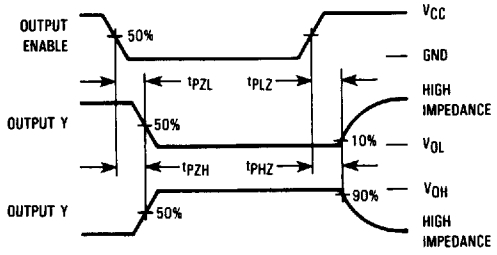
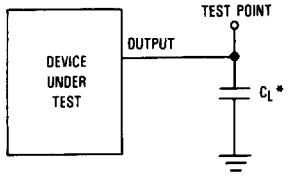


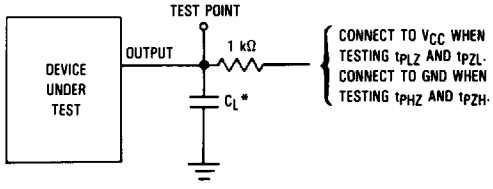

Figure 3.

## TEST CIRCUITS




*Includes all probe and jig capacitance.

Figure 4.




*Includes all probe and jig capacitance.

Figure 5.

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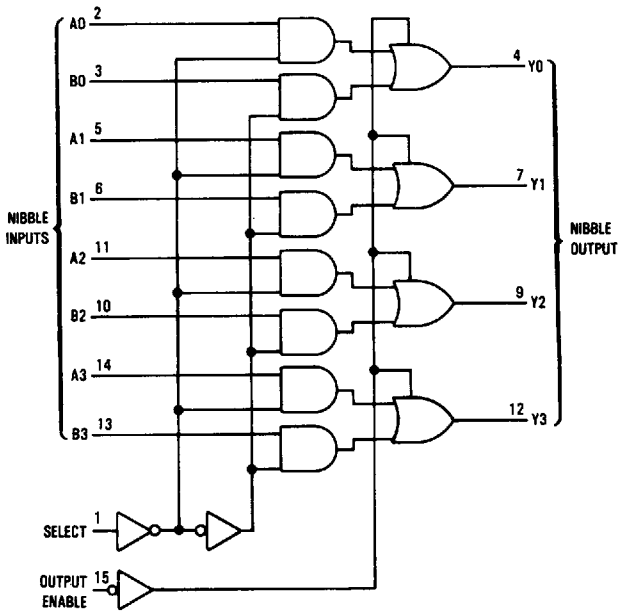
EXPANDED LOGIC DIAGRAM

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