

**Description**

The GM23C8000A high performance read only memory is organized as 1,048,576 x 8 bits and has an access time of 120/150ns. The GM23C8000A offers automatic power down controlled by the mask programmed CE or  $\overline{CE}$  input. The low power feature allow the battery operation. An additional feature of GM23C8000A is the Output Enable. OE functions (may be mask programmed as OE/ $\overline{OE}$ ) in order to eliminate bus contention in multiple bus micro processor systems. This ROM is packaged 32 Pin DIP or 32 Pin SOP.

**Features**

- 1,048,576 x 8 bit Organization
- Single + 5V Supply
- Access Time : 120/150ns (Max)
- Operating current : 50mA (Max)
- Standby current : 50 $\mu$ A (Max)
- TTL-compatible inputs and outputs
- Polarity programmable chip enable and out enable pin
- 3-State outputs for wired-OR expansion
- Fully static operation
- Package :
  - GM23C8000A : 32 Pin Plastic DIP (600 mil)
  - GM23C8000AFW : 32 Pin Plastic SOP (525 mil)

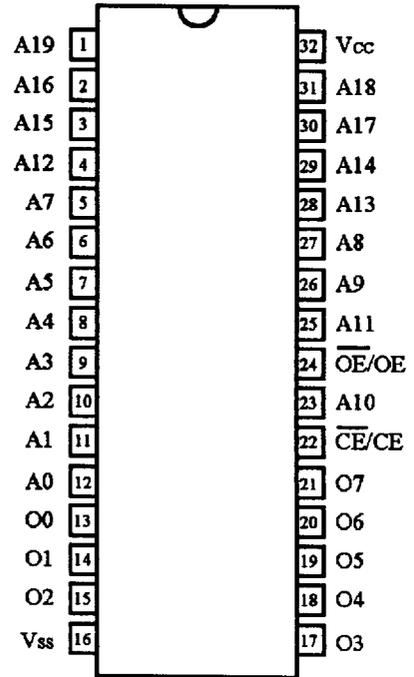
**Pin Description**

Pin	Function
A0-A19	Address Inputs
O0-O7	Data Outputs
CE/ $\overline{CE}$ *	Chip Enable Input
OE/ $\overline{OE}$ *	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground

\*User Selectable Polarity.

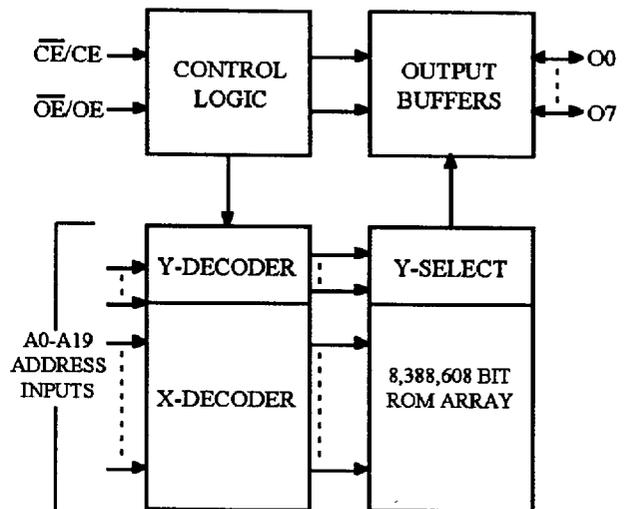
**Pin Configuration**

**32 DIP/SOP**



(Top View)

**Block Diagram**



**Absolute Maximum Ratings\***

Symbol	Parameter	Rating	Unit
T <sub>A</sub>	Ambient Operating Temperature	-10 ~ 80	°C
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C
V <sub>CC</sub>	Supply Voltage to Ground Potential	-0.5 ~ V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	Output Voltage	-0.5 ~ V <sub>CC</sub> + 0.5	V
V <sub>IN</sub>	Input Voltage	-0.5 ~ 7.0	V

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = 0 ~ 70°C)**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	-	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage	-0.3	-	0.8	V

**DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%, T<sub>A</sub> = 0 ~ 70°C)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA			0.4	V
I <sub>I(L)</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>			± 10	μA
I <sub>O(L)</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>			± 10	μA
I <sub>CC</sub>	Operating Supply Current (f = 6.7 MHz)	$\overline{CE} = V_{IL}, CE = V_{IH}$			50	mA
I <sub>SB1</sub>	Standby Current (TTL)	$\overline{CE} = V_{IH}$ , all Output Open			1	mA
I <sub>SB2</sub>	Standby Current (CMOS)	$\overline{CE} = V_{CC}$ , all Output Open			50	μA

**Capacitance (T<sub>A</sub> = 25°C, f = 1.0 MHz)**

Symbol	Parameter	Condition	Min	Max	Unit
C <sub>I</sub>	Input Capacitance	V <sub>IN</sub> = 0V		10	pF
C <sub>O</sub>	Output Capacitance	V <sub>OUT</sub> = 0V		10	pF

Note : Capacitance is periodically sampled and not 100% tested.

**Mode Selection**

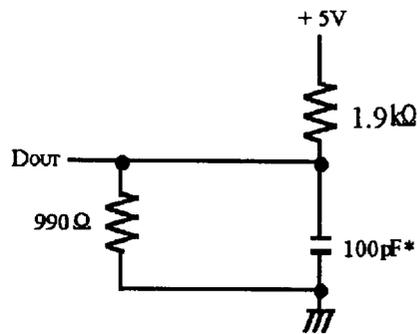
CE/ $\overline{\text{CE}}$	OE/ $\overline{\text{OE}}$	Mode	Data	Power
L/H	X	Standby	High Z	Standby
H/L	L/H	Operating	High Z	Active
	H/L		Down	

**AC Operating Characteristics** ( $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ\text{C}$ )

Symbol	Parameter	GM23C8000A-12		GM23C8000A-15		Unit
		Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	120		150		ns
$t_{ACE}$	Chip Enable Access Time		120		150	ns
$t_{AA}$	Address Access Time		120		150	ns
$t_{AOE}$	Output Enable Access Time		60		70	ns
$t_{OH}$	Output Hold From Address Change	10		10		ns
$t_{OHZ}$ $t_{CHZ}$	Output or Chip Disable to Output High-Z		50		60	ns
$t_{OLZ}$ $t_{CLZ}$	Output or Chip Enable to Output Low-Z	10		10		ns

**AC Test Condition**

Input Pulse Level	0.4V to 2.4V
Input Rise and Fall Time	10ns
Input and Output Timing Level	0.8V to 2.0V
Output Load	See Fig. 1

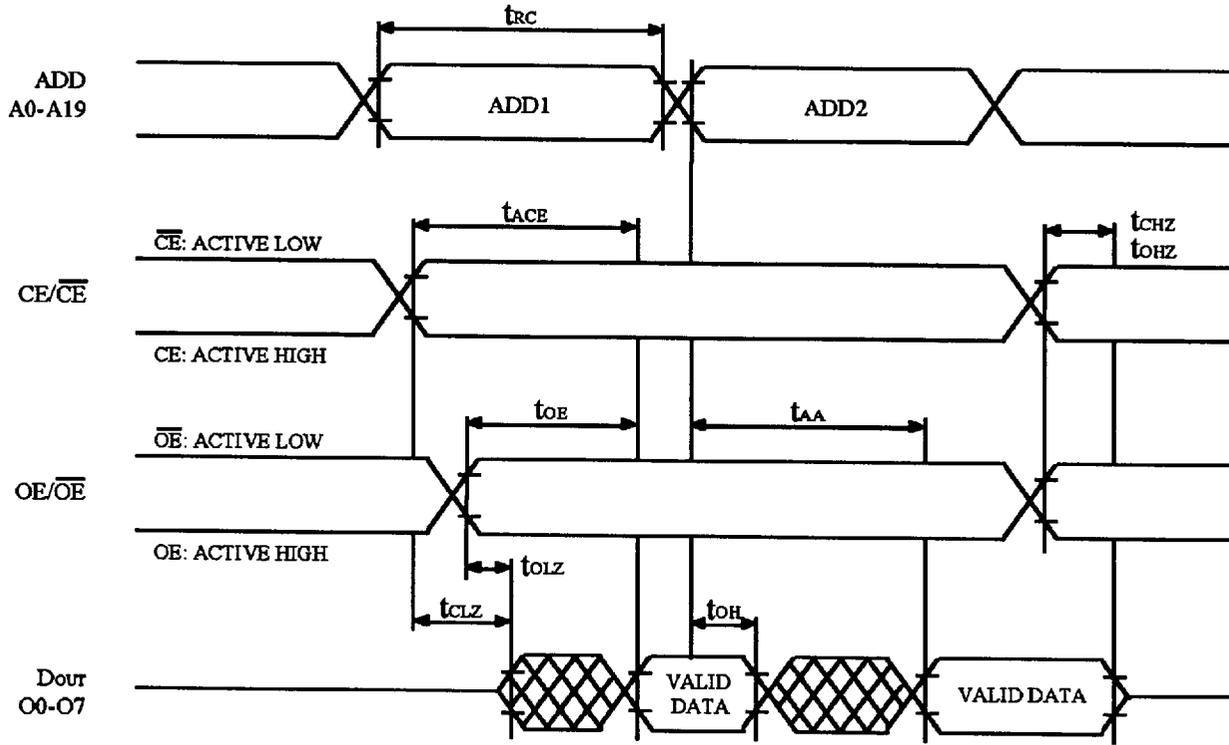


\*Including scope and jig.

**Fig. 1 Output Load Circuit**

Timing Waveforms

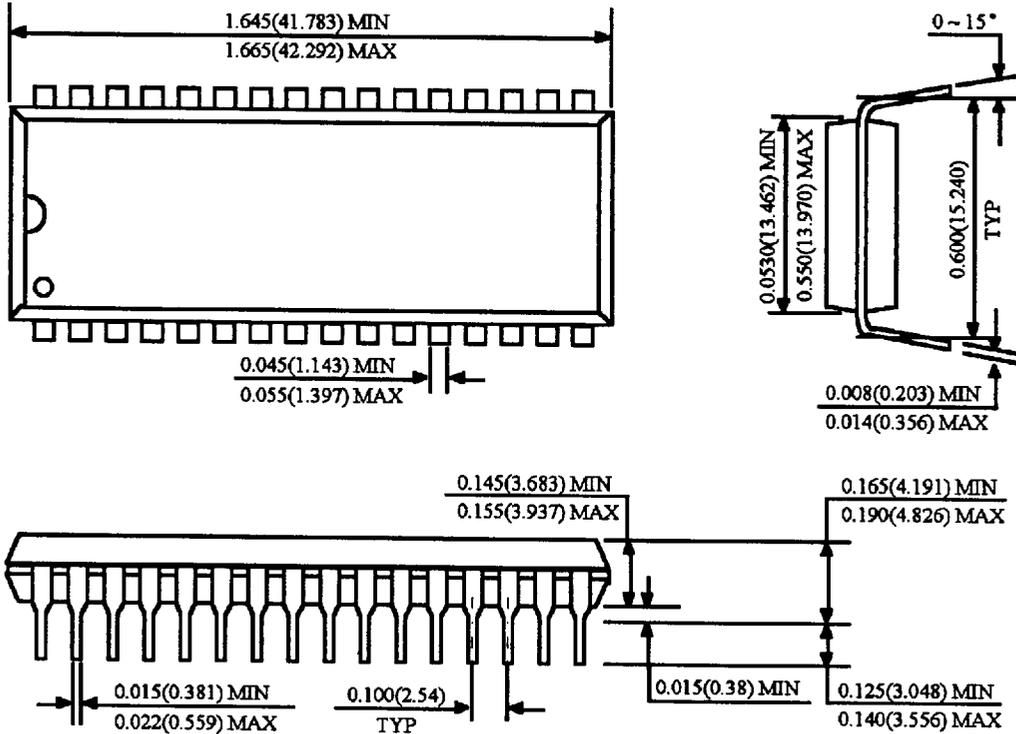
Read



**Package Dimensions**

Unit: Inches (mm)

**32 DIP - B**



**32 SOP - B**

