

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
D	Change R <sub>L</sub> to 2 KΩ. Convert to military drawing format. Remove vendor, CAGE 27014.	86-10-16	N. A. Hauck
E	Add footnote to table I. Change max frequency. Add LCC package. Add vendor CAGE 04713. Editorial changes throughout. Change logic diagram.	87-10-21	R. P. Evans
F	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-04-14	Raymond Monnin
G	Update to reflect latest changes in format and requirements. Correct paragraph in 3.5. Editorial changes throughout. --les	05-05-31	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

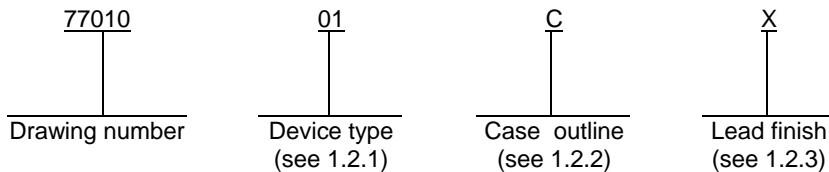
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PMIC N/A	PREPARED BY	<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsc.dla.mil">http://www.dsc.dla.mil</a></p>																		
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY	<p>N. A. Hauck</p>																		
	APPROVED BY	<p>N. A. Hauck</p>																		
	DRAWING APPROVAL DATE	<p align="center">77-05-17</p>																		
	REVISION LEVEL	SIZE	CAGE CODE																	
<b>G</b>	A	<b>14933</b>	<b>77010</b>																	
	SHEET	1 OF 10																		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type. The device type identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	54LS196	30 MHz presetable decade or binary counter

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
C	GDIP1-T14 or CDIP2-T14	14	dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	flat
2	CQCC1-N20	20	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage .....	-0.5 V dc to +7.0 V dc
Input voltage range .....	-1.5 V dc at -18 mA to +5.5 V dc
Storage temperature range.....	-65°C to +150°C
Maximum power dissipation (P <sub>D</sub> ) 1/.....	149 mW
Lead temperature (soldering, 10 seconds) .....	+300°C
Thermal resistance, junction-to-case (θ <sub>JC</sub> ) .....	See MIL-STD-1835
Junction temperature (T <sub>J</sub> ) .....	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V <sub>CC</sub> ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V <sub>IH</sub> ) .....	2.0 V dc
Maximum low level input voltage (V <sub>IL</sub> ) .....	0.7 V dc
Case operating temperature range (T <sub>C</sub> ) .....	-55°C to +125°C

1/ Maximum power dissipation is defined as V<sub>CC</sub> x I<sub>CC</sub>, and must withstand the added P<sub>D</sub> due to short-circuit test; e.g., I<sub>OS</sub>.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

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3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
High level output voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -400 μA V <sub>IN</sub> = 0.7 V or 2.0 V	1, 2, 3	All	2.5		V	
Low level output voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4 mA V <sub>IN</sub> = 0.7 V or 2.0 V	1, 2, 3	All		0.4	V	
Input clamp voltage	V <sub>IC</sub>	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA, T <sub>C</sub> = +25°C	1, 2, 3	All		-1.5	V	
High level input current	I <sub>IH1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 2.7 V	Data, $\overline{\text{LOAD}}$	1, 2, 3	All		20	μA
	I <sub>IH2</sub>		$\overline{\text{CLR}}$ , CLK 1	1, 2, 3	All		40	μA
			CLK 2	1, 2, 3	All		80	μA
	I <sub>IH3</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IH</sub> = 5.5 V	Data, $\overline{\text{LOAD}}$	1, 2, 3	All		100	μA
			$\overline{\text{CLR}}$ , CLK 1	1, 2, 3	All		200	μA
				CLK 2	1, 2, 3	All		400
Low level input current	I <sub>IL1</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V	Data, $\overline{\text{LOAD}}$	1, 2, 3	All		-400	μA
	I <sub>IL2</sub>		$\overline{\text{CLR}}$	1, 2, 3	All		-800	μA
	I <sub>IL3</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IL</sub> = 0.4 V	CLK 1	1, 2, 3	All		-2.4	mA
	I <sub>IL4</sub>		CLK 2	1, 2, 3	All		-2.8	mA
Short circuit output current	I <sub>OS</sub>	V <sub>CC</sub> = 5.5 V 1/	1, 2, 3	All	-6	-130	mA	
Supply current	I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V	1, 2, 3	All		27	mA	
Functional tests		See 4.3.1c	7	All				
Maximum clock frequency CLK 1	f <sub>MAX</sub>	V <sub>CC</sub> = 5.0 V, R <sub>L</sub> = 2 KΩ ±5%, C <sub>L</sub> = 50 pF ±10% 2/	9	All	25		MHz	
			10, 11	All	17		MHz	
Propagation delay time, CLK 1 to Q <sub>A</sub>	t <sub>PLH1</sub>	C <sub>L</sub> = 50 pF ±10% 2/	9	All		20	ns	
			10, 11	All		28	ns	
	t <sub>PHL1</sub>		9	All		30	ns	
			10, 11	All		35	ns	
Propagation delay time, CLK 2 to Q <sub>B</sub>	t <sub>PLH2</sub>	C <sub>L</sub> = 50 pF ±10% 2/	9	All		29	ns	
			10, 11	All		41	ns	
	t <sub>PHL2</sub>		9	All		42	ns	
			10, 11	All		53	ns	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C 1/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay time, CLK 2 to Q <sub>C</sub>	t <sub>PLH3</sub>	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 50 pF ±10% R <sub>L</sub> = 2 kΩ ±5%	9	All		68	ns
			10, 11	All		87	ns
	t <sub>PHL3</sub>		9	All		72	ns
			10, 11	All		94	ns
Propagation delay time, CLK 2 to Q <sub>D</sub>	t <sub>PLH4</sub>		9	All		23	ns
			10, 11	All		32	ns
	t <sub>PHL4</sub>		9	All		54	ns
			10, 11	All		70	ns
Propagation delay time, A, B, C, D to Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	t <sub>PLH5</sub>		9	All		35	ns
			10, 11	All		49	ns
	t <sub>PHL5</sub>		9	All		53	ns
			10, 11	All		69	ns
Propagation delay time, LOAD to any output	t <sub>PLH6</sub>		9	All		45	ns
			10, 11	All		64	ns
	t <sub>PHL6</sub>		9	All		54	ns
			10, 11	All		70	ns
Propagation delay time, high-to-low level, CLR to any output	t <sub>PHL7</sub>		9	All		60	ns
			10, 11	All		78	ns

1/ Not more than one output should be shorted at a time and the duration of the short circuit condition should not exceed one second.

2/ Propagation delay time testing and maximum clock frequency testing may be performed using either C<sub>L</sub> = 15 pF or C<sub>L</sub> = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50 pF load.

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Device types	01	01
Case outlines	C, D	2
Terminal number	Terminal symbols	Terminal symbols
1	$\overline{\text{LOAD}}$	N/C
2	$Q_C$	$\overline{\text{LOAD}}$
3	C	$Q_C$
4	A	C
5	$Q_A$	N/C
6	CLK 2	A
7	GND	N/C
8	GND	$Q_A$
9	CLK 1	CLK 2
10	$Q_B$	GND
11	B	N/C
12	D	CLK 1
13	$\overline{\text{CLR}}$	$Q_B$
14	$V_{CC}$	B
15	---	N/C
16	---	D
17	---	N/C
18	---	$Q_D$
19	---	$\overline{\text{CLR}}$
20	---	$V_{CC}$

FIGURE 1. Terminal connections.

Count	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

H = High voltage level  
L = Low voltage level

NOTE: Output  $Q_A$  connected to CLK2 input

FIGURE 2. Truth table.

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Device type 01

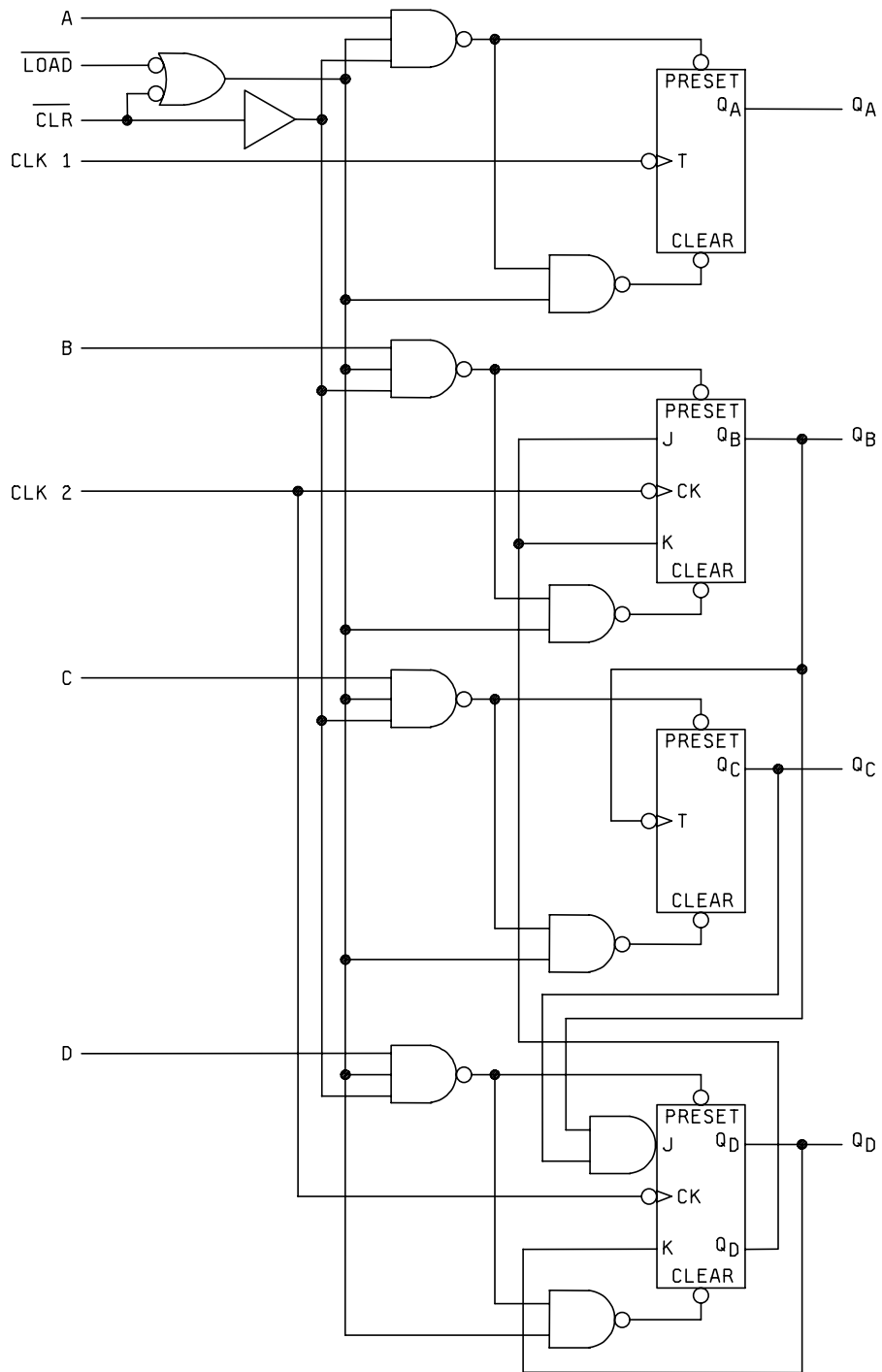


FIGURE 3. Logic diagram.

<b>STANDARD MICROCIRCUIT DRAWING</b> DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>77010</b>
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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

\* PDA applies to subgroup 1.

\*\* Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 shall include verification of the truth table.

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4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
  - (2)  $T_A = +125^{\circ}\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-05-31

Approved sources of supply for SMD 77010 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>	Reference military specification PIN
7701001CA	<u>3/</u> <u>3/</u> 0DSK7	SNJ54LS196J 54LS196/BCAJC GEM31001QCA	M38510/32001BCA
7701001CC	0DKS7	GEM31001QCC	
7701001DA	<u>3/</u> 0DSK7	SN54LS196W GEM31001QDA	M38510/32001BDA
7701001DC	0DKS7	GEM31001QDC	
77010012A	<u>3/</u> <u>3/</u>	SNJ54LS196FK 54LS196M/B2AJC	

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source.

Vendor CAGE  
number

Vendor name  
and address

0DKS7

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