March 1994

DATA SHEET

M 65864

8,192 x 8 STATIC RAM

FEATURES

- **BICMOS FOR OPTIMUM SPEED/POWER**
- **HIGH SPEED**
  COMMERCIAL : 9/10/12/15 ns (max)
  MILITARY : 10/12/15 ns (max)
- **LOW ACTIVE POWER**
  – 825 mW
- **LOW STANDBY POWER**
  – 275 mW
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **CAPABLE OF WITH STANDING GREATER THAN 2001V ELECTROSTATIC DISCHARGE**

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INTRODUCTION

The M-65864 is a high-performance BiCMOS static RAM organized as 8,192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have a power-down feature ($\overline{CE_1}$) that reduces the power consumption by 67 % when deselected. An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE_1}$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

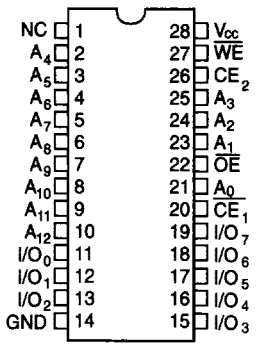
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

The M-65864 is 100 % processed following the test methods of MIL STD 883C and/or ESA/SCC 9000 making it ideally suitable for military/space applications that demand superior levels of performance and reliability.

INTERFACE

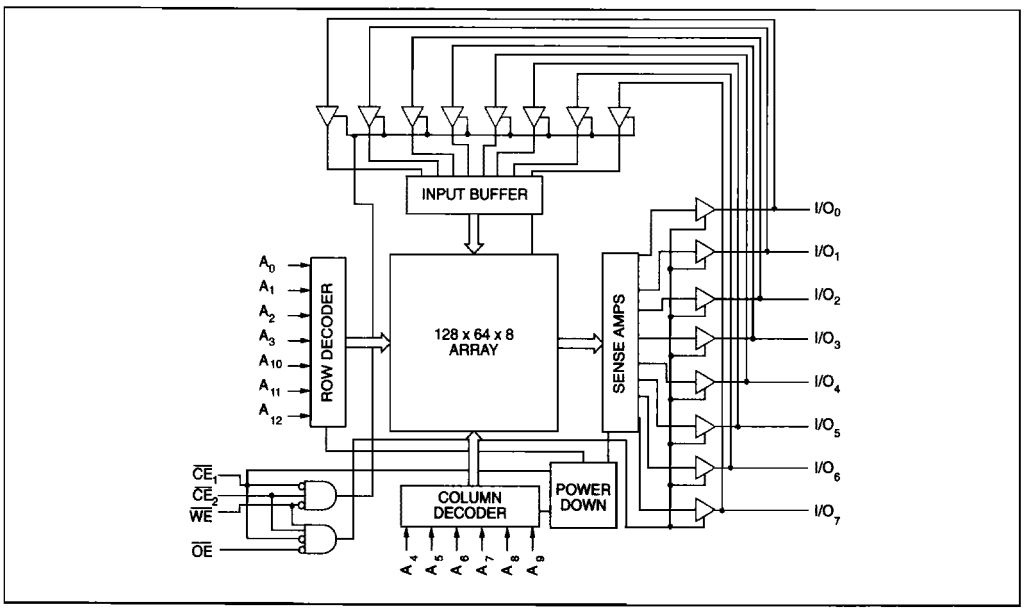
PIN CONFIGURATION

Plastic 300 mils, 28 pins, DIL
Ceramic 300 mils, 28 pins, DIL
SOJ 300 mils, 28 pins



Pinout DIL/SO 28 pins (top view)

BLOCK DIAGRAM



SELECTION GUIDE

		M-65864-09	M-65864-10	M-65864-12	M-65864-15
Maximum Access Time (ns)		9	10	12	15
Maximum Operating Current (mA)	Commercial	150	145	140	135
	Military		155	150	145
Maximum Standby Current (mA)	Commercial	50	45	40	40
	Military		60	55	50

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested).

Storage Temperature..... – 65°C to + 150°C

Supply Voltage
to Ground Potential..... – 0.5 V to + 7.0 V

DC Voltage Applied
to Outputs in High Z State..... – 0.5 V to + 7.0 V

DC Input Voltage..... – 3.0 V to + 7.0 V

Output Current into Outputs (Low).. 20 mA

Static Discharge Voltage ..... > 2001 V
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

OPERATING RANGE

RANGE		AMBIENT TEMPERATURE	Vcc
Military	(2)	– 55°C to + 125°C	5 V ± 10 %
Commercial	(2)	– 0°C to + 70°C	5 V ± 10 %

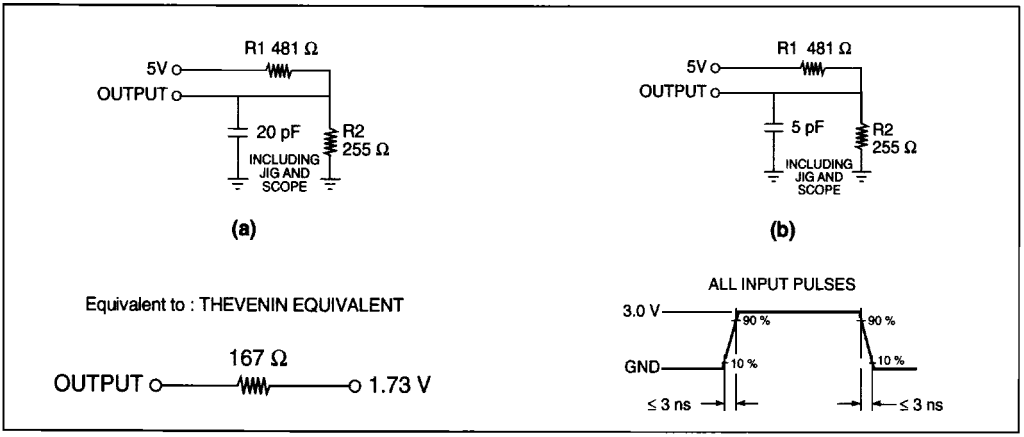
PARAMETERS	DESCRIPTION	TEST CONDITIONS			M-65864-09		M-65864-10		M-65864-12		M-65864-15		UNITS
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = – 4 mA	Com'l	2.4		2.4		2.4		2.4		V
			I_{OH} = – 2 mA	Mil	2.4		2.4		2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	2.2	Vcc	2.2	Vcc	V
V_{IL}	Input LOW Voltage(1)				– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ Vcc			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ Vcc Output Disabled			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		150		145		140		135	mA
				Mil				155		150		145	
I_{SB}	$\overline{CE_1}$ Power-Down Current	$\overline{CE_1}$ ≤ V_{IH}		Com'l		50		45		40		40	mA
				Mil				60		55		50	

CAPACITANCE (3)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MAXIMUM(4)	UNITS
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz, 5	pF	
C_{OUT}	Output capacitance	V_{CC} = 5.0 V	7	pF

Notes : 1. V_{IL} (min) = – 3.0 V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except Ceramic DIL, which has maximum of C_{IN} = 8 pf, C_{OUT} = 9 pF.

AC TEST LOADS AND WAVEFORMS



SWITCHING CHARACTERISTICS (OVER THE OPERATING RANGE [5])

READ CYCLE

SYMBOL	PARAMETER	M-65864-09		M-65864-10		M-65864-12		M-65864-15		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAV	Read Cycle Time	9		10		12		15		ns
TAVQV	Address to Data Valid		9		10		12		15	ns
TAVQX	Data Hold from Address Change	2.5		3		3		3		ns
TEL1QV	$\overline{CE_1}$ LOW to Data Valid		9		10		12		15	ns
TEL2QV	$\overline{CE_2}$ HIGH to Data Valid		9		10		12		15	ns
TGLQV	$\overline{OE}$ LOW to Data Valid		4.5		5		6		8	ns
TGLQX	$\overline{OE}$ LOW to Low Z	1.5		2		2		3		ns
TGHQZ	$\overline{OE}$ HIGH to High Z (6)		4		5		6		7	ns
TEL1QX	$\overline{CE_1}$ to Low Z (7)	2		2		2		3		ns
TEH2QX	$\overline{CE_2}$ HIGH to Low Z (7)	2		2		2		3		ns
TEHQZ	$\overline{CE_1}$ HIGH to HIGH Z (6) $\overline{CE_2}$ LOW to High Z		4		5		6		7	ns

WRITE CYCLE[8]

SYMBOL	PARAMETER	M-65864-09		M-65864-10		M-65864-12		M-65864-15		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAV	Write Cycle Time	9		10		12		15		ns
TEL1WH	$\overline{CE_1}$ LOW to Write End	8		8		8		10		ns
TEH2WH	$\overline{CE_2}$ HIGH to Write End	8		8		8		10		ns
TAVWH	Address Set-Up to Write End	8		8		8		10		ns
TWHAX	Address Hold From Write End	0		0		0		0		ns
TAVWL	Address Set-Up to Write Start	0		0		0		0		ns
TWLWH	$\overline{WE}$ Pulse Width	7		8		8		10		ns
TDVWH	Data Set-up to Write End	4.5		5		6		7		ns
TWHDX	Data Hold from Write End	0		0		0		0		ns
TWLQZ	$\overline{WE}$ LOW to High Z [6]	0	4	0	5	0	6	0	7	ns
TWHQX	$\overline{WE}$ HIGH to Low Z	2		2		2		3		ns

Notes : 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.

6. TGHQZ, TEHQZ and TWLQZ are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ± 220 mV from steady-state voltage.

7. At any given temperature and voltage condition, TEHQZ is less than TELQX for any given device.

8. The internal write time of the memory id defined by the overlap of $\overline{CE_1}$, LOW, CE_2 HIGH and $\overline{WE}$ LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

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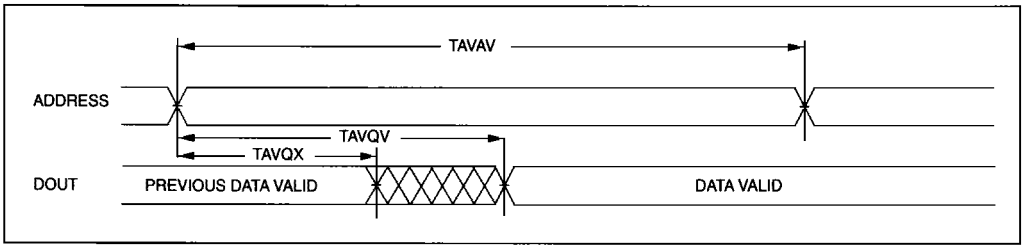
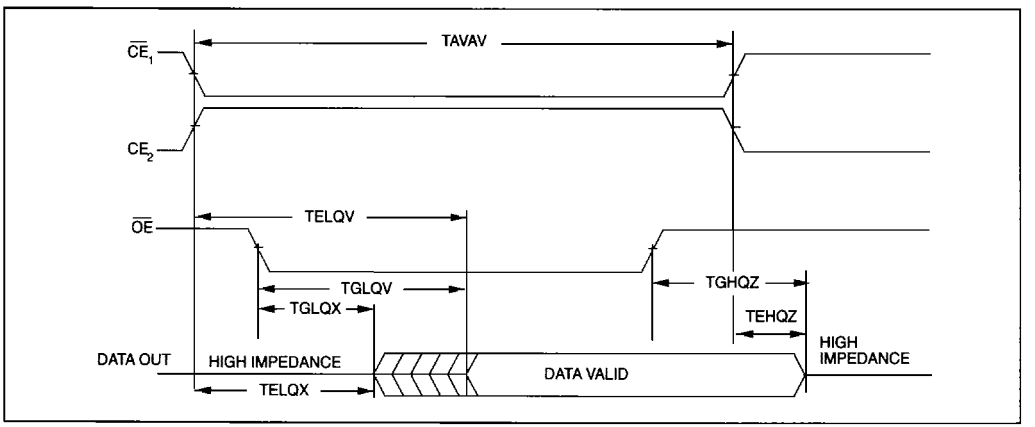
READ CYCLE N°.1 (9, 10)



READ CYCLE N°.2 (9, 11)



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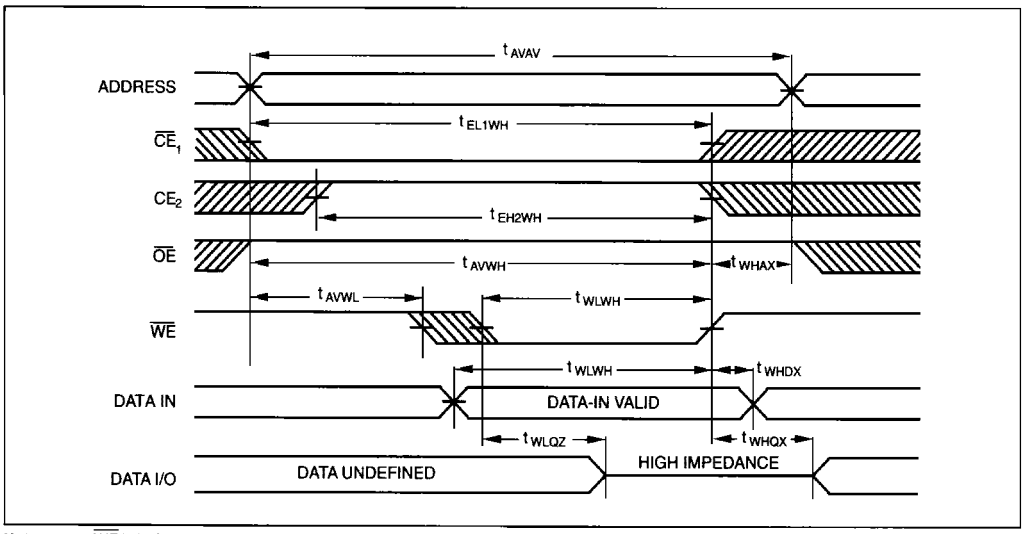
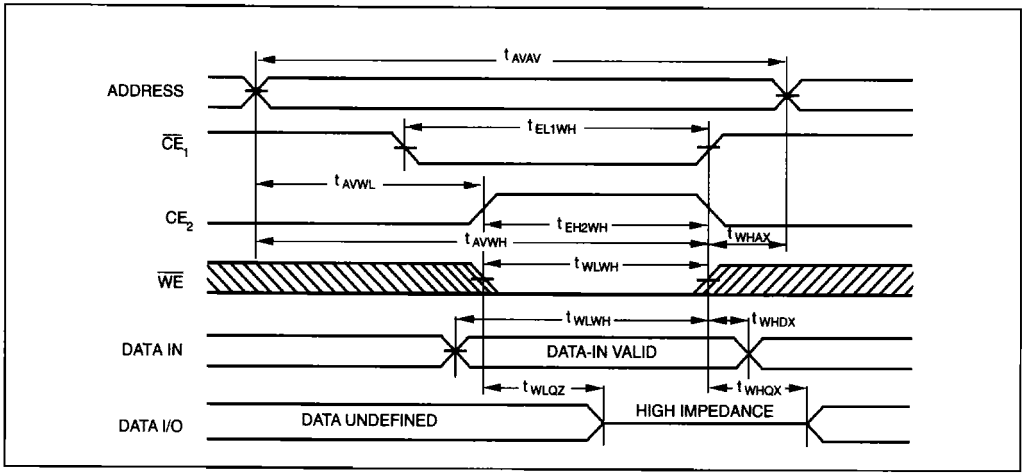
WRITE CYCLE N°.1 ($\overline{WE}$ CONTROLLED) (12, 13)



Notes : 9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{OE}$, $\overline{CE}_1$ = V_{IL}. CE_2 = V_{IH}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
13. When data input is applied to the devicel/O, the device output should be in the high impedance state.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

WRITE CYCLE N° 2 ($\overline{CE}$ CONTROLLED) (11, 13, 14)



TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{WE}$	$\overline{OE}$	INPUTS/ OUTPUTS	MODE
H	X	X	X	High Z	Deselect/ Power Down
L	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselected

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ORDERING INFORMATION

TEMPERATURE RANGE	PACKAGE	DEVICE	SPEED
C M	UI	65864	12
C = Commercial 0°C to + 70°C M = Military – 55° to + 125°C	0 : chip form 1P : ceramic 28 pins 3P : Plastic 28 pins UI : SOJ 28 pins	8K x 8 HIGH SPEED STATIC RAM	09 : 9 ns 10 : 10 ns 12 : 12 ns 15 : 15 ns

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