1M x 16Bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 1,048,576 x16 bit Extended Data Out CMOS DRAMs. Dxtended Data Out mode offers high speed random access of memory cells within the same row, so called Hyper Page Mode. Power supply voltage (+5.0V or +3.3V), refresh cycle (1K Ref. or 4K Ref.), access time (-5, -6, -7 or -8), power consumption (Normal or Low power) and package type (SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Furthermore, self-refresh operation is available in L-version.

This 1Mx16 Extended Data Out mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memroy unit for microcomputer, personal computer and portable machines.

FEATURES

- Part Identification
  - KM416C1004B/B-L (5V, 4K Ref.)
  - KM416C1204B/B-L (5V, 1K Ref.)
  - KM416V1004B/B-L (3.3V, 4K Ref.)
  - KM416V1204B/B-L (3.3V, 1K Ref.)

- Active Power Dissipation

Unit : mW

Speed	3.3V		5V	
	4K	1K	4K	1K
-5	-	-	605	880
-6	360	540	550	825
-7	324	504	495	770
-8	288	468	-	-

- Refresh cycles

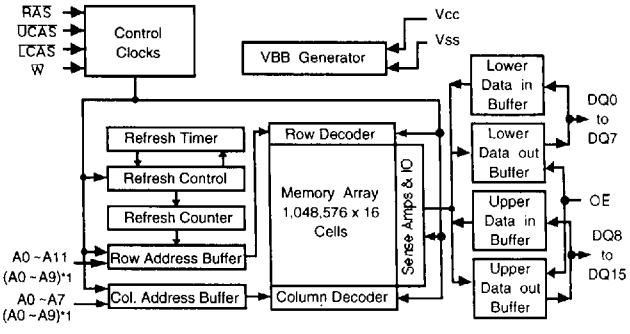
Part NO.	Vcc	Refresh cycle	Refresh period	
			Normal	L-ver
C1004B	5V	4K	64ms	128ms
V1004B	3.3V			
C1204B	5V	1K	16ms	
V1204B	3.3V			

- Performance range

Speed	tRAC	tCAC	tRC	tHPC	Remark
-5	50ns	17ns	84ns	20ns	5V
-6	60ns	17ns	114ns	25ns	5V/3.3V
-7	70ns	20ns	124ns	30ns	5V/3.3V
-8	80ns	20ns	144ns	35ns	3.3V

- Extended Data Out mode operation (Fast Page mode with Extended Data Out)
- 2$\overline{CAS}$ Byte/Word Read/Write operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- Self-refresh capability (L-ver)
- TTL(5V)/LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- Single +5V±10% power supply (5V product)
- Single +3.3V±0.3V power supply (3.3V product)

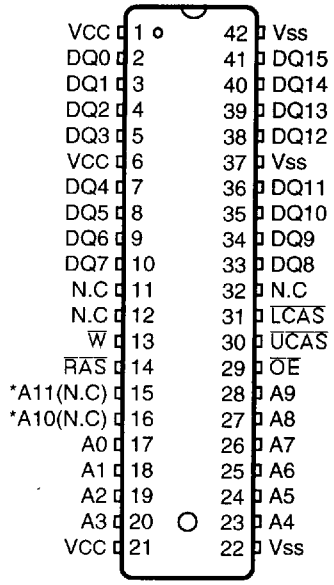
FUNCTIONAL BLOCK DIAGRAM



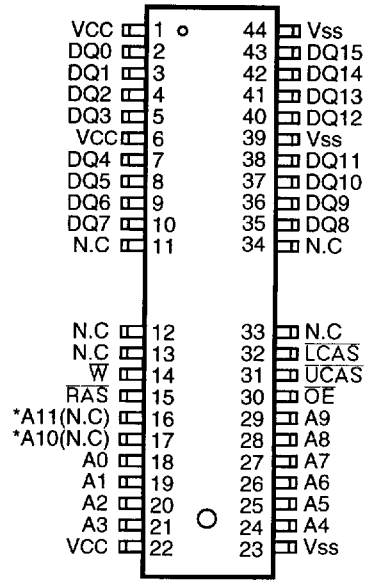
Note) *1 : 1K Refresh

PIN CONFIGURATION (Top Views)

• KM416C/V10(2)04BJ



• KM416C/V10(2)04BT



* A10 and A11 are N.C for KM416C/V1204B (5V/3.3V, 1K Ref. product)

J : 400mil 42 SOJ
T : 400mil 50(44) TSOP II

Pin Name	Pin Function
A0 - A11	Address Inputs (4K Product)
A0 - A9	Address Inputs (1K Product)
DQ0 -15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Outputs Enable
Vcc	Power (+5.0V)
	Power (+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Units
		3.3V	5V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	-1 to +7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	-55 to +150	°C
Power Dissipation	P_D	1	1	W
Short Circuit Output Current	I_{OS}	50	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A= 0 to 70 °C)

Parameter	Symbol	3.3V			5V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.1	-	Vcc+0.3 *1	2.4	-	Vcc+1 *1	V
Input Low Voltage	V_{IL}	-0.3 *2	-	0.8	-1.0 *2	-	0.8	V

*1 : Vcc+1.3V/15ns(3.3V), Vcc+2.0V/20ns(5V), Pulse width is measured at Vcc.
*2 : - 1.3V/15ns(3.3V), - 2.0V/20ns(5V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

	Parameter	Symbol	Min	Max	Units
3.3V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.3V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level (I_{OH}=-2mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=2mA)	V_{OL}	-	0.4	V
5V	Input Leakage Current (Any input 0≤V_{IN}≤Vcc+0.5V, all other pins not under test=0 volt.)	$I_{I(L)}$	- 5	5	µA
	Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤Vcc)	$I_{O(L)}$	- 5	5	µA
	Output High Voltage Level (I_{OH}=-5mA)	V_{OH}	2.4	-	V
	Output Low Voltage Level (I_{OL}=4.2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Speed	Max				Units
			KM416V1000B	KM416V1200B	KM416C1000B	KM416C1200B	
I_{CC1}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC2}	Normal	Don't care	1	1	2	2	mA
	L		1	1	1	1	mA
I_{CC3}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC4}	Don't care	-5	-	-	120	120	mA
		-6	110	110	110	110	mA
		-7	100	100	100	100	mA
		-8	90	90	-	-	mA
I_{CC5}	Normal	Don't care	0.5	0.5	1	1	mA
	L		0.2	0.2	0.2	0.2	mA
I_{CC6}	Don't care	-5	-	-	110	160	mA
		-6	100	150	100	150	mA
		-7	90	140	90	140	mA
		-8	80	130	-	-	mA
I_{CC7}	L	Don't care	400	300	450	350	μA
I_{CCS}	L	Don't care	200	200	250	250	μA

I_{CC1}* : Operating Current ($\overline{RAS}$,$\overline{UCAS}$,$\overline{LCAS}$, Address cycling @tRC=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-Only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$,Address cycling @tRC=min.)

I_{CC4}* : Hyper Page Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @tHPC=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$, $\overline{UCAS}$ or $\overline{LCAS}$ cycling @tRC=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=Vcc-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$,$\overline{LCAS}$=0.2V,
Din = Don't care, T_{RC}= 31.25μs(4K/L-ver), 125μs(1K/L-ver), T_{RAS}=T_{RAS}min~300ns

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=V_{IL}, $\overline{W}$=$\overline{OE}$=A0 ~ A11 = Vcc-0.2V or 0.2V,
DQ0 ~ DQ15= Vcc-0.2V, 0.2V or Open

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle time, tHPC.

CAPACITANCE (T_A=25°C, Vcc=5V or 3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance [A0 - A11]	C_{IN1}	-	5	pF
Input capacitance [$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$, $\overline{OE}$]	C_{IN2}	-	7	pF
Output Capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5*1		-6		-7		-8*2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		124		144		ns	
Read-modify-write cycle time	tRWC	115		140		170		190		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70		80	ns	3,4,9
Access time from $\overline{CAS}$	tCAC		15		17		20		20	ns	3,4
Access time from column address	tAA		25		30		35		40	ns	3,9
$\overline{CAS}$ to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	3	13	3	15	3	20	3	20	ns	5,12
$\overline{OE}$ to output in Low-Z	tOLZ	3		3		3		3		ns	3
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		60		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	80	10K	ns	
$\overline{RAS}$ hold time	tRSH	13		17		20		20		ns	
$\overline{CAS}$ hold time	tCSH	40		50		60		70		ns	
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	35	20	43	20	50	20	60	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	13
Column address hold time	tCAH	8		10		15		15		ns	13
Column address to $\overline{RAS}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		0		ns	7
Read command hold time referenced to $\overline{RAS}$	tRRH	0		0		0		0		ns	7
Write command hold time	tWCH	10		10		15		15		ns	
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		20		ns	16

Note) *1 : 5V only, *2 : 3.3V only

AC CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, See note 1,2)

Test condition (5V device) : Vcc=5.0V±10%, V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V
Test condition (3.3V device) : Vcc=3.3V±0.3V, V_{ih}/V_{il}=2.1/0.8V, V_{oh}/V_{ol}=2.0/0.8V

Parameter	Symbol	-5 *1		-6		-7		-8 *2		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		0		ns	8, 19
Data hold time	tDH	8		10		15		15		ns	8, 19
Refresh period (1K, Normal)	tREF		16		16		16		16	ms	
Refresh period (4K, Normal)	tREF		64		64		64		64	ms	
Refresh period(L-ver)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	6
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	32		36		44		44		ns	6, 15
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	67		79		94		104		ns	6
Column address to $\overline{W}$ delay time	tAWD	42		49		59		64		ns	6
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	47		54		64		69		ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	5		5		5		10		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		28		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		25		30		35		ns	10
Hyper Page read-modify-write cycle time	tHPRWC	47		56		71		81		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	tCP	8		10		10		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{OE}$ access time	tOEA		13		15		20		20	ns	3
$\overline{OE}$ to data delay	tOED	13		15		20		20		ns	
Out put buffer turn off delay time from $\overline{OE}$	tOEZ	3	13	3	15	3	20	3	20	ns	6
$\overline{OE}$ command hold time	tOEH	13		15		20		20		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	3	20	ns	5, 12
Output buffer turn off delay from $\overline{W}$	tWEZ	3	13	3	15	3	20	3	20	ns	5
$\overline{W}$ to data delay	tWED	15		15		20		20		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		5		ns	
$\overline{W}$ pulth width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
$\overline{RAS}$ pulse width ($\overline{C}$-B-$\overline{R}$ self refresh)	tRASS	100		100		100		100		us	11
$\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh)	tRPS	90		110		130		150		ns	11
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh)	tCHS	-50		-50		-50		-50		ns	11

Note) *1 : 5V only, *2 : 3.3V only

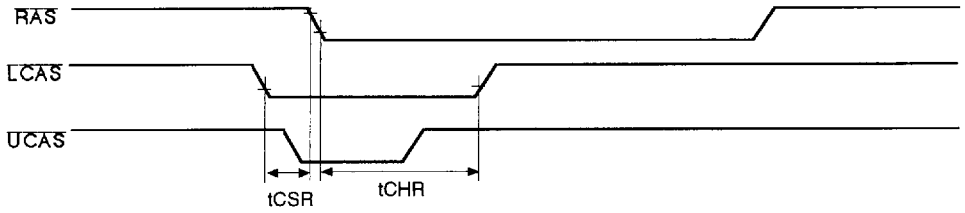
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
6. tWCS, tRWD, tCWD, tAWD and tCPWD are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥tCWD(min), tRWD≥tRWD(min), tAWD≥tAWD(min) and tCPWD≥tCPWD(min) then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
7. Either tRCH or tRRH must be satisfied for a read cycle.
8. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
9. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

KM416C/V10(2)04B/B-L Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ0 -DQ7	DQ8- DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

10. tASC≥ 6 ns, Assume tT = 2.0 ns
11. For all of the refresh modes except for distributed $\overline{CAS}$-Before-$\overline{RAS}$ refresh, 4096(4K Ref.)/1024(1K Ref.) of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification(L-version).
12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
13. tASC, tCAH are referenced to the earlier $\overline{CAS}$ falling edge.
14. tCP is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.
15. tCWD is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.
16. tCWL is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. tCSR is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.
18. tCHR is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. tDS, tDH is independently specified for lower byte D_{IN}(0~7), upper byte D_{IN}(8~15).