PRELIMINARY

CY7C1019D

1-Mbit (128K x 8) Static RAM

Features

- **Pin- and function-compatible with CY7C1019B**
- **High speed**
  - **— t_{AA} = 10 ns**
- **CMOS for optimum speed/power**
- **Low active power**
  - **— I_{CC} = 60 mA @ 10 ns**
- **Low CMOS standby power**
  - **— I_{SB2} = 1.2 mA ('L' Version only)**
- **Data Retention at 2.0V**
- **Center power/ground pinout**
- **Automatic power-down when deselected**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options**
- **Functionally equivalent to CY7C1019B**
- **Available in Pb-Free Packages**

Functional Description[1]

The CY7C1019D is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and tri-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

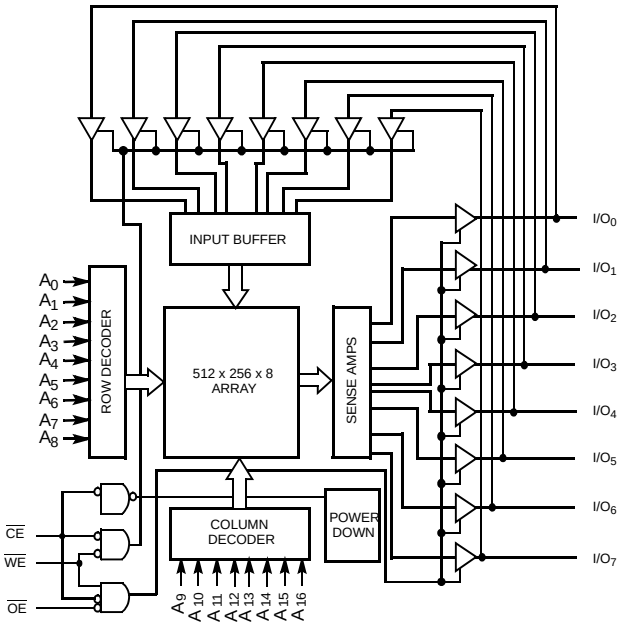
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

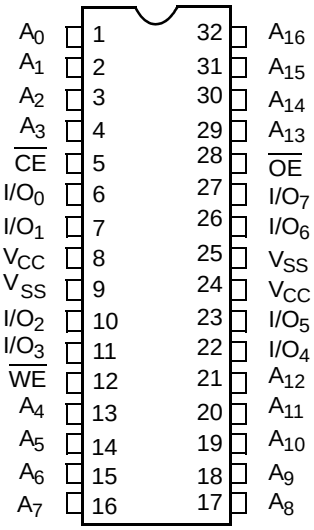
The CY7C1019D is available in standard 32-pin TSOP Type II and 400-mil-wide SOJ Pb-Free packages.

Logic Block Diagram



Pin Configurations

SOJ/TSOPII
Top View



Note:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Selection Guide

		CY7C1019D-10	CY7C1019D-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current		60	50	mA
Maximum Standby Current		3	3	mA
	L	1.2	1.2	

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[2].....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C1019D-10 Min.	7C1019D-10 Max.	7C1019D-12 Min.	7C1019D-12 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			60		50	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			10		10	mA
			L		10		10	
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			3.0		3.0	mA
			L		1.2		1.2	

Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

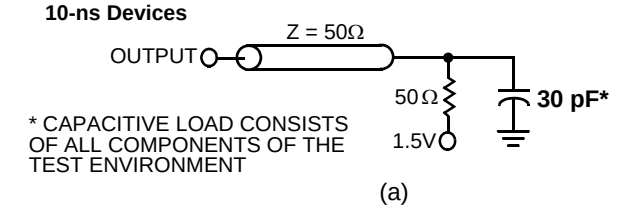
Thermal Resistance[3]

Parameter	Description	Test Conditions	All - Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[3]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[3]		TBD	°C/W

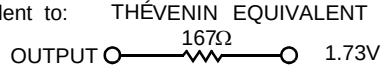
Notes:
2. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

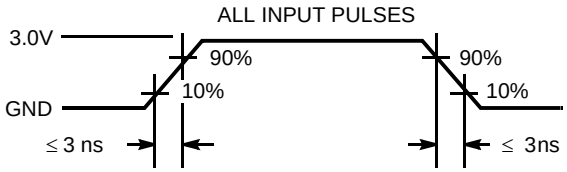
AC Test Loads and Waveforms

10-ns Devices

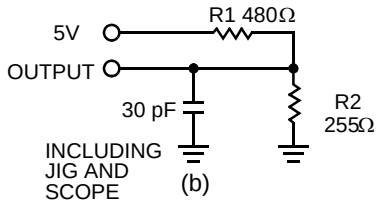


Equivalent to: THÉVENIN EQUIVALENT

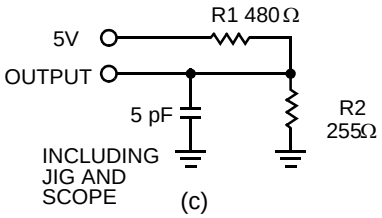




12 -ns Devices



High-Z characteristics:



Switching Characteristics Over the Operating Range [5]

Parameter	Description	7C1019D-10		7C1019D-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}[4]	V_{CC}(typical) to the first access	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12	ns
Write Cycle[8, 9]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		9		ns
t_{AW}	Address Set-Up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-Up to Write End	5		6		ns

Notes:

4. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

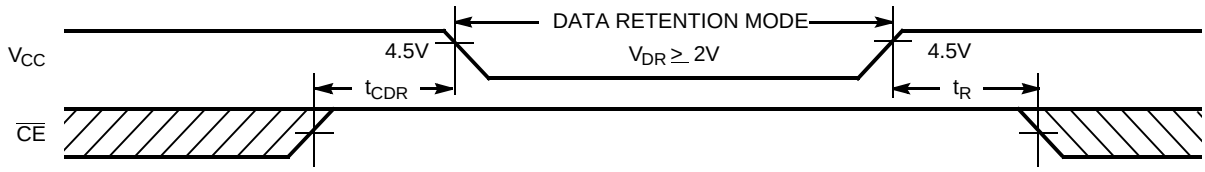
Switching Characteristics Over the Operating Range (continued)[5]

Parameter	Description	7C1019D-10		7C1019D-12		Unit
		Min.	Max.	Min.	Max.	
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		5		6	ns

Data Retention Characteristics Over the Operating Range

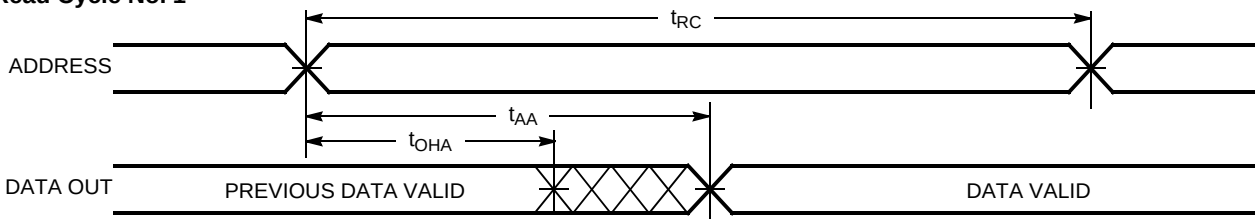
Parameter	Description		Conditions	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		$\overline{V_{CC}} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current	Non-L, Com'l/Ind'l			3	mA
		L-Version Only			1.2	mA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0		ns
t_R[10]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform

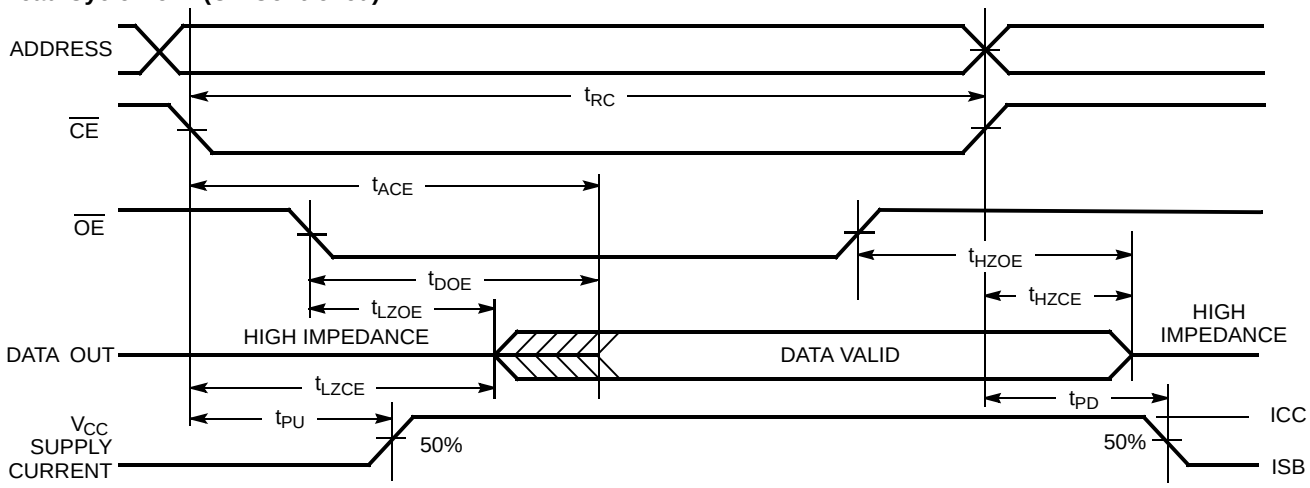


Switching Waveforms

Read Cycle No. 1[11, 12]



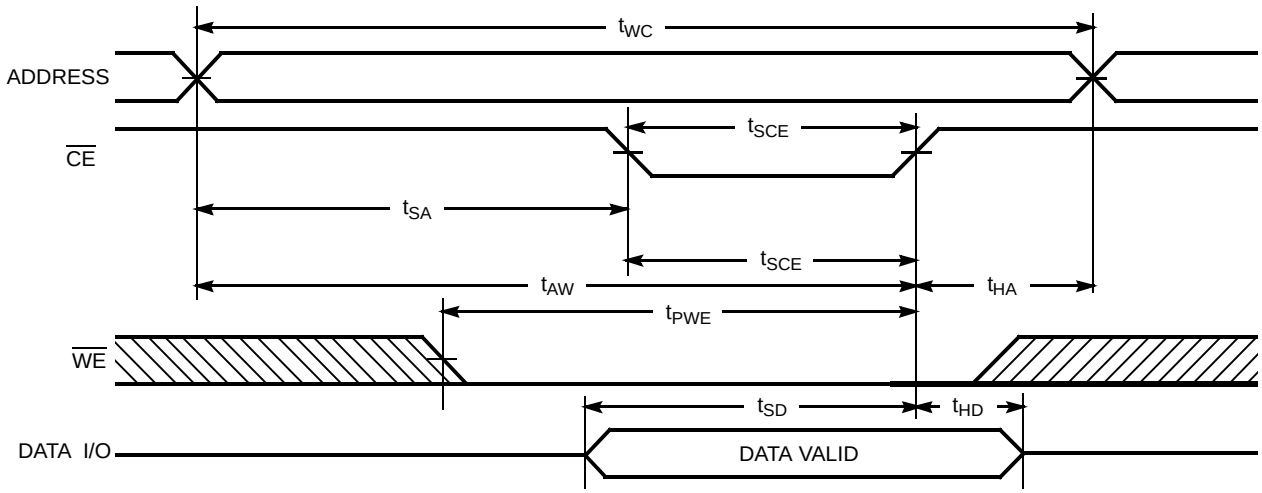
Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]



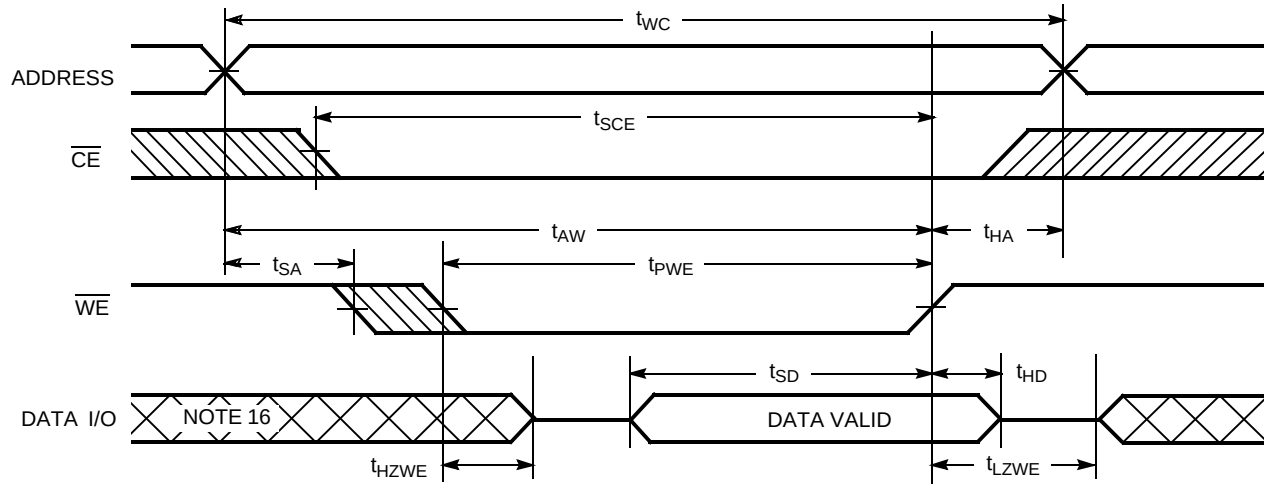
Notes:
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50\ \mu s$ or stable at $V_{CC(min.)} \geq 50\ \mu s$.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[14, 15]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[15]



Notes:
14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
X	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

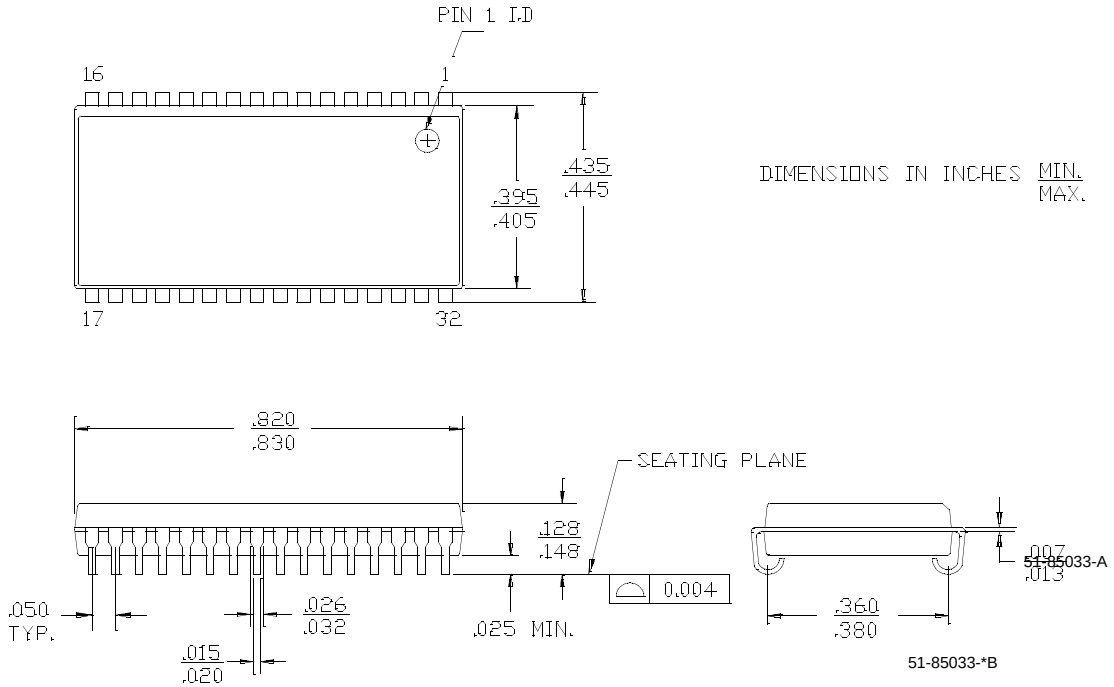
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1019D-10VXC	V33	32-Lead 400-Mil Molded SOJ (Pb-Free)	Commercial
	CY7C1019D-10VXI	V33	32-Lead 400-Mil Molded SOJ (Pb-Free)	Industrial
	CY7C1019D-10ZXC	ZS32	32-Lead TSOP Type II (Pb-Free)	Commercial
	CY7C1019D-10ZXI	ZS32	32-Lead TSOP Type II (Pb-Free)	Industrial
12	CY7C1019D-12VXC	V33	32-Lead 400-Mil Molded SOJ (Pb-Free)	Commercial
	CY7C1019D-12VXI	V33	32-Lead 400-Mil Molded SOJ (Pb-Free)	Industrial
	CY7C1019D-12ZXC	ZS32	32-Lead TSOP Type II (Pb-Free)	Commercial
	CY7C1019D-12ZXI	ZS32	32-Lead TSOP Type II (Pb-Free)	Industrial

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

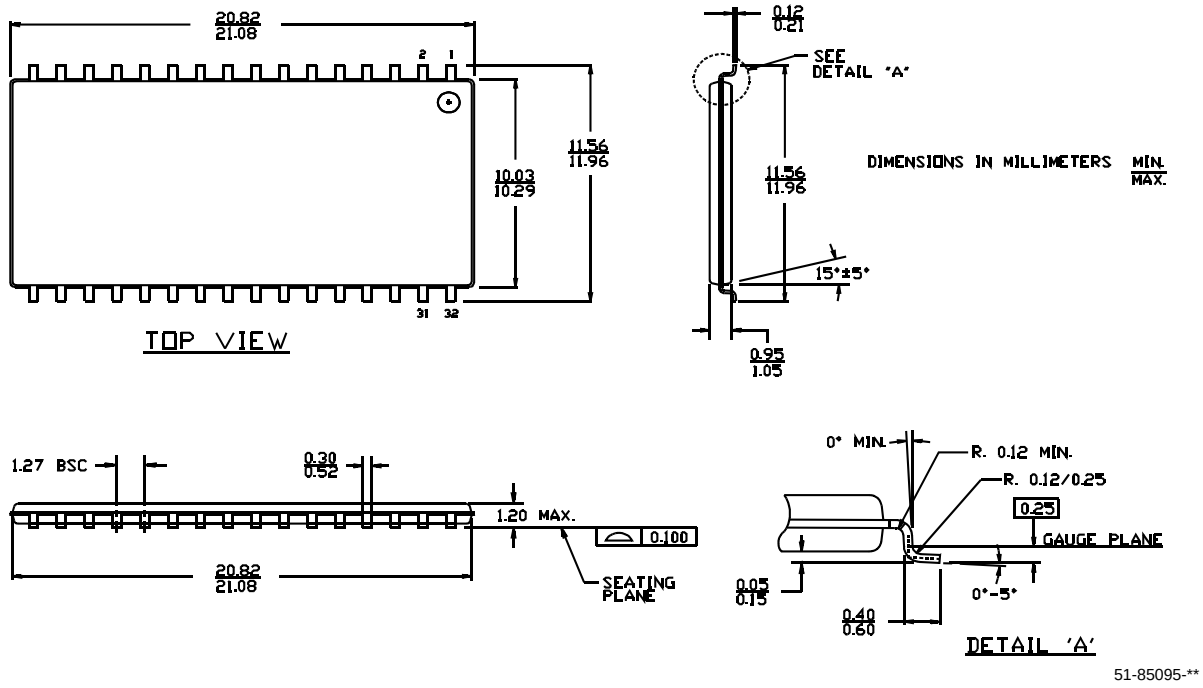
Package Diagrams

32-Lead (400-Mil) Molded SOJ V33



Package Diagrams (continued)

32-Lead TSOP II ZS32



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Document History Page

Document Title: CY7C1019D 1-Mbit (128K x 8) Static RAM (Preliminary) Document Number: 38-05464				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233715	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in the Ordering Information
*B	262950	See ECN	RKF	Added T_{power} Spec in Switching Characteristics table Added Data Retention Characteristics table and waveforms Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -10 and -12 ns