DESCRIPTION

This family is a 16M bit dynamic RAM organized 1,048,576 x 16-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode is a kind of page mode which is useful for the read operation. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60, 70 or 80ns) and refresh cycle(1K ref. or 4K ref.) and power consumption (Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page mode operation
- Read-modify-write Capability
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- JEDEC standard pinout
- 42-pin Plastic SOJ (400mil)
  44/50-pin plastic TSOP-II (400mil)
- Single power supply of 3.3V ± 0.3V
- Early write or output enable controlled write

- Max. Active power dissipation

Speed	1K refresh	4K refresh
60	540mW	324mW
70	468mW	288mW
80	432mW	252mW

- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- Refresh cycle

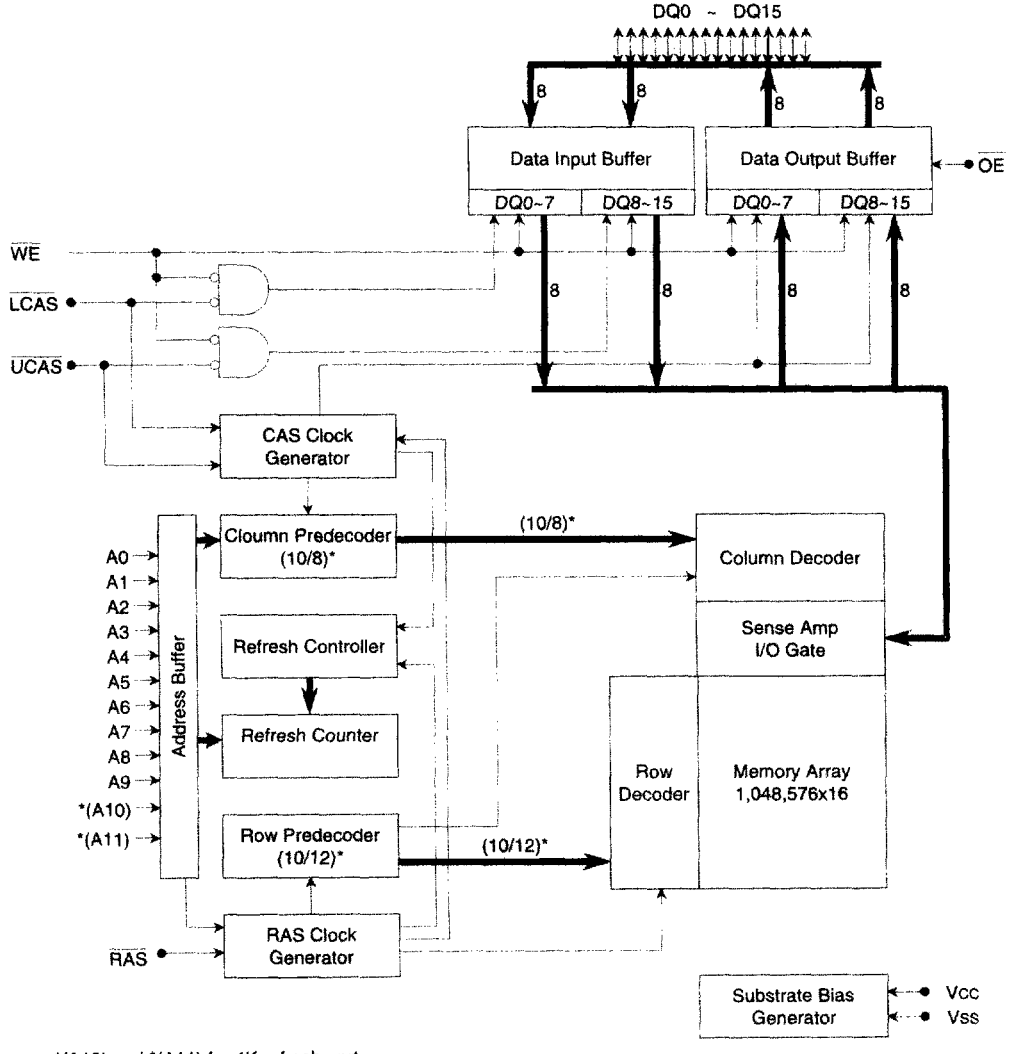
Part number	Refresh	Normal	SL-part
HY51V18160B	1K	16ms	256ms
HY51V16160B	4K	64ms	

ORDERING INFORMATION

Part Name	Refresh	Power	Package
HY51V18160BJC	1K		42Pin SOJ
HY51V18160BSLJC	1K	SL-part	42Pin SOJ
HY51V18160BTC	1K		44/50Pin TSOP-II
HY51V18160BSLTC	1K	SL-part	44/50Pin TSOP-II
HY51V16160BJC	4K		42Pin SOJ
HY51V16160BSLJC	4K	SL-part	42Pin SOJ
HY51V16160BTC	4K		44/50Pin TSOP-II
HY51V16160BSLTC	4K	SL-part	44/50Pin TSOP-II

*SL : Low power with self refresh

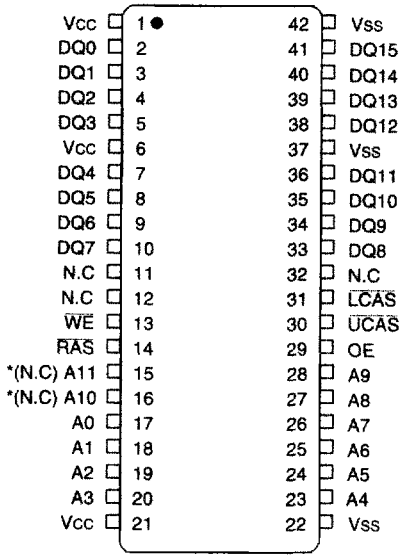
FUNCTIONAL BLOCK DIAGRAM



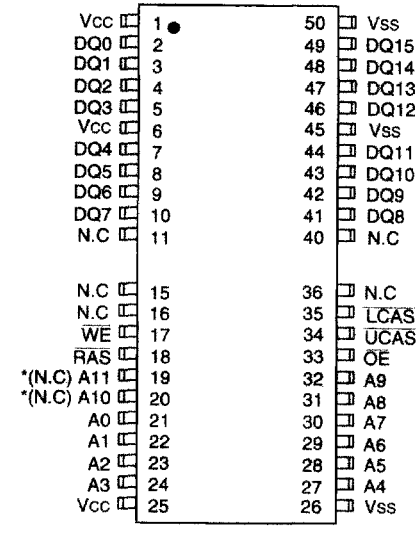
*(A10) and *(A11) for 4K refresh part

(1K Refresh / 4K Refresh)*

PIN CONFIGURATION (Marking Side)



42Pin Plastic SOJ (400mil)



44/50Pin Plastic TSOP- II (400mil)

*(N.C) : For 1K refresh product

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A11	Address Input (4K Refresh Product)
A0~A9	Address Input (1K Refresh Product)
DQ0~DQ15	Data In/Out
Vcc	Power (3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-0.5 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTIC

Symbol	Parameter	Test condition	Min	Max	Unit
I_{LI}	Input Leakage Current (Any input)	$V_{SS} \le V_{IN} \le V_{CC} + 0.3$ All other pins not under test = V_{SS}	-10	10	μA
I_{LO}	Output Leakage Current (Any input)	$V_{SS} \le V_{OUT} \le V_{CC}$ /RAS & /CAS at V_{IH}	-10	10	μA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2.0mA	2.4	-	V

DC CHARACTERISTICS

(T_A = 0°C to 70°C , V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max. Current		Unit
				1K Ref	4K Ref	
I_{CC1}	Operating Current	/RAS, /CAS Cycling t_{RC} = t_{RC}(min.)	60 70 80	140 130 120	100 90 80	mA
I_{CC2}	LVTTL Standby Current	/RAS, /CAS ≥ V_{IH} Other inputs ≥ V_{SS}	 SL-part	1 1	1 1	mA
I_{CC3}	/RAS-only Refresh Current	/RAS Cycling,/CAS = V_{IH} t_{RC} = t_{RC}(min.)	60 70 80	140 130 120	100 90 80	mA
I_{CC4}	Fast Page mode Current	/CAS Cycling, /RAS = V_{IL} t_{PC} = t_{PC}(min.)	60 70 80	110 100 90	100 90 80	mA
I_{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V_{CC} - 0.2V	 SL-part	500 200	500 200	µA µA
I_{CC6}	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V t_{RC} = t_{RC}(min.)	60 70 80	140 130 120	100 90 80	mA
I_{CC7}	Battery Back-up Current (SL-part)	tRC=250µs (1K Ref), 62.5µs (4K Ref) /CAS = CBR Cycling or 0.2V /OE & /WE = V_{CC} - 0.2V Address = Vcc-0.2V or 0.2V DQ0~DQ15 = Vcc-0.2, 0.2V or Open	tRAS ≤ 300ns	350	350	µA
			tRAS ≤ 1µs	450	450	
I_{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I_{CC7}		350	350	µA

Note

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{PC}).
2. Specified values are obtained with output unloaded.
3. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one Fast Page mode cycle time t_{PC}.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tRC	Random read or write cycle time	110	-	130	-	150	-	ns	
tRWC	Read-modify-write cycle time	155	-	170	-	200	-	ns	
tPC	Fast Page mode cycle time	40	-	45	-	50	-	ns	
tPRWC	Fast Page mode read-modify-write cycle time	80	-	95	-	105	-	ns	
tRAC	Access time from /RAS	-	60	-	70	-	80	ns	4,5,6
tCAC	Access time from /CAS	-	15	-	20	-	20	ns	4,5
tAA	Access time from column address	-	30	-	35	-	40	ns	4,6
tCPA	Access time from column precharge	-	35	-	40	-	40	ns	4
tCLZ	/CAS to output low impedance	0	-	0	-	0	-	ns	4
tOFF	Output buffer turn-off delay from /CAS	0	15	0	15	0	15	ns	7
tT	Transition time(rise and fall)	3	50	3	50	3	50	ns	2
tRP	/RAS precharge time	40	-	50	-	60	-	ns	
tRAS	/RAS pulse width	60	10K	70	10K	80	10K	ns	
tRASP	/RAS pulse width(Fast Page mode)	60	100K	70	100K	80	100K	ns	
tRSH	/RAS hold time	15	-	20	-	20	-	ns	
tCSH	/CAS hold time	60	-	70	-	80	-	ns	
tCAS	/CAS pulse width	15	10K	15	10K	20	10K	ns	
tRCD	/RAS to /CAS delay time	20	45	20	50	20	60	ns	5
tRAD	/RAS to column address delay time	15	30	15	35	15	40	ns	6
tCRP	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	
tCP	/CAS precharge time	10	-	10	-	10	-	ns	
tASR	Row address set-up time	0	-	0	-	0	-	ns	
tRAH	Row address hold time	10	-	10	-	10	-	ns	
tASC	Column address set-up time	0	-	0	-	0	-	ns	
tCAH	Column address hold time	15	-	15	-	15	-	ns	
tRAL	Column address to /RAS lead time	30	-	35	-	40	-	ns	
tRCS	Read command set-up time	0	-	0	-	0	-	ns	
tRCH	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	8
tRRH	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	8
tWCH	Write command hold time	15	-	15	-	15	-	ns	
tWP	Write command pulse width	10	-	10	-	10	-	ns	
tRWL	Write command to /RAS lead time	20	-	20	-	20	-	ns	
tCWL	Write command to /CAS lead time	20	-	20	-	20	-	ns	14

AC CHARACTERISTICS

Continued

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tDS	Data-in set-up time	0	-	0	-	0	-	ns	9
tDH	Data-in hold time	15	-	15	-	15	-	ns	9
tREF	Refresh period(1024 cycles)	-	16	-	16	-	16	ms	
	Refresh period(4096 cycles)	-	64	-	64	-	64	ms	
	Refresh period(SL-part)	-	256	-	256	-	256	ms	
tWCS	Write command set-up time	0	-	0	-	0	-	ns	10
tCWD	/CAS to /WE delay time	45	-	50	-	50	-	ns	10,13
tRWD	/RAS to /WE delay time	85	-	95	-	105	-	ns	10
tAWD	Column address to /WE delay time	55	-	60	-	65	-	ns	10
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	15
tCHR	/CAS hold time(CBR cycle)	10	-	10	-	10	-	ns	16
tRPC	/RAS to /CAS precharge time	5	-	5	-	5	-	ns	9
tCPT	/CAS precharge time(CBR counter test)	30	-	35	-	40	-	ns	12
tROH	/RAS hold time referenced to /OE	10	-	10	-	10	-	ns	
tOEA	/OE access time	-	15	-	20	-	20	ns	
tOED	/OE to data delay time	15	-	20	-	20	-	ns	
tOEZ	Output buffer turn-off delay time from /OE	0	15	0	15	0	15	ns	7
tOEH	/OE command hold time	15	-	20	-	20	-	ns	
tCPWD	/WE delay time from /CAS precharge	55	-	65	-	75	-	ns	10
tRHCP	/RAS hold time from /CAS precharge	40	-	40	-	50	-	ns	
tWRP	/WE to /RAS precharge time(CBR cycle)	10	-	10	-	10	-	ns	
tWRH	/WE to /RAS hold time(CBR cycle)	10	-	10	-	10	-	ns	
tRASS	/RAS pulse width(self refresh)	100K	-	100K	-	100K	-	ns	
tRPS	/RAS Precharge Time (Self refresh)	110	-	130	-	150	-	ns	
tCHS	/CAS Hold Time (Self refresh)	-50	-	-50	-	-50	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA=0 to 70°C) is assured.
4. Measured at V_{OH}=2.0V and VOL=0.8V with a load equivalent to 1TTL loads and 100pF.
5. Operation within the $t_{RCD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
6. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
7. t_{OFF} and t_{OEZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to /LCAS or /UCAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles .
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, $t_{AWD} \geq t_{AWD(min)}$, and $t_{CPWD} \geq t_{CPWD(min.)}$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. t_{ASC},t_{CAH} are referenced to the earlier /CAS falling edge.
12. t_{CP} and t_{CPT} are measured when both /LCAS and /UCAS are high state.
13. t_{CWD} is referenced to the later /CAS falling edge at word read-modifiy-write cycle.
14. t_{CWL} must be satisfied by both /LCAS and /UCAS for 16-bit access cycles.
15. t_{CSR} is referenced to the earlier /CAS falling before /RAS transition low.
16. t_{CHR} is referenced to the later /CAS rising high after /RAS transition low.
17. t_{DS}, t_{DH} is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).

CAPACITANCE

(T_A = 25°C, V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
C_{IN1}	Input Capacitance (A0~A11)	-	5	pF
C_{IN2}	Input Capacitance (/RAS, /LCAS,/UCAS, /WE, /OE)	-	7	pF
C_{DQ}	Data Input / Output Capacitance (DQ0~DQ15)	-	7	pF