CY54/74FCT646T
CY54/74FCT648T
8-BIT REGISTERED TRANSCEIVERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Independent Register for A and B Buses**
- **3-State Output**

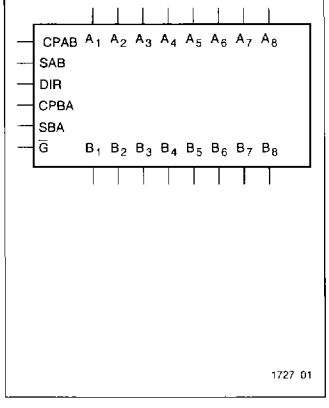
2

DESCRIPTION

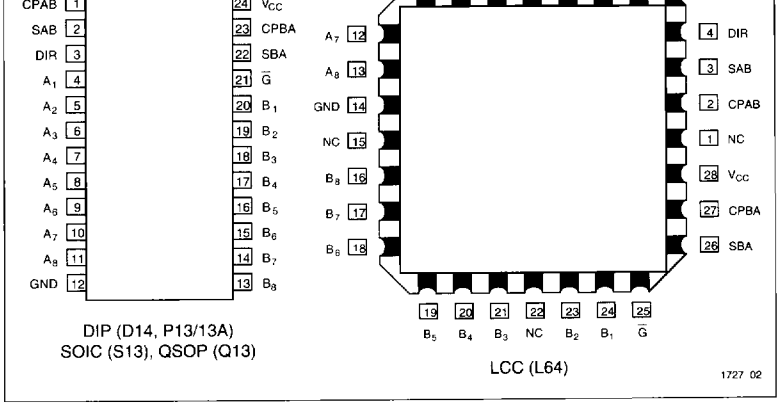
The 'FCT646T and 'FCT648T consist of a bus tranceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function.

In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

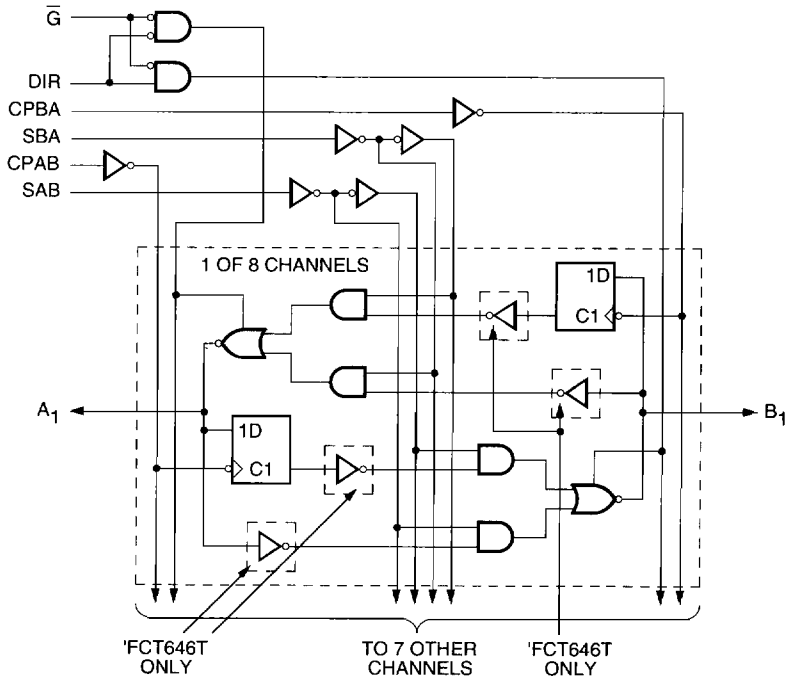
LOGIC SYMBOL



PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM

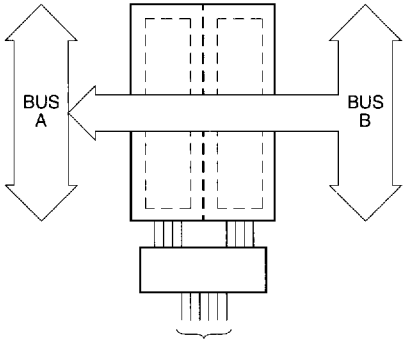


1727 03

PIN DESCRIPTION

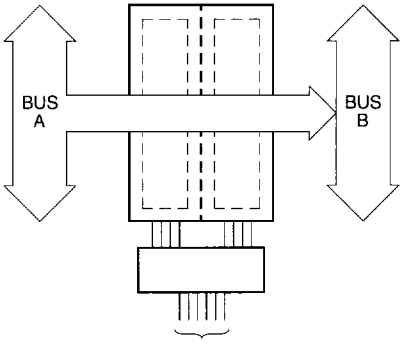
Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

1727 Tbl 01



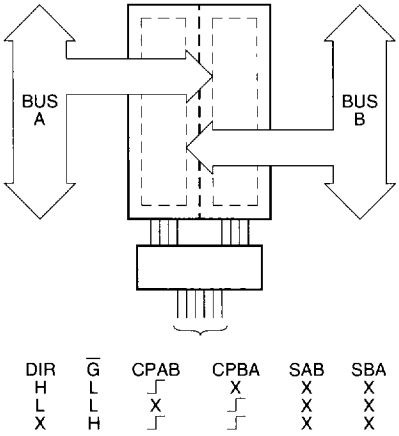
REAL-TIME TRANSFER BUS B TO BUS A

1727 04



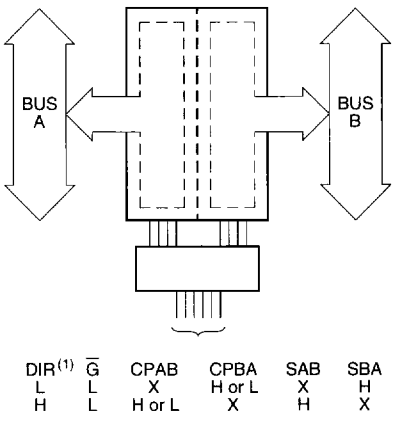
REAL-TIME TRANSFER BUS A TO BUS B

1727 05



STORAGE FROM A AND/OR B

1727 06



TRANSFER STORED DATA TO A AND/OR B

1727 07

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLE

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT646T	'FCT648T
H H	X X	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

1727 Tbl 02

Notes:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are alwaysenabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↓ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1727 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1727 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1727 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1727 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1727 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1727 Tbl 08

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT646T/648T				'FCT646AT/648AT				'FCT646CT/648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A or B	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

1727 Tbl 09

Notes:

* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

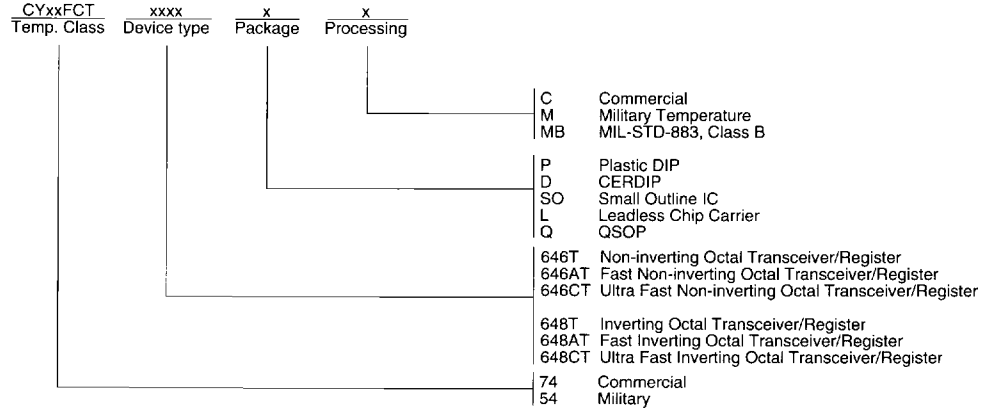
Symbol	Parameter	'FCT646T/648T				'FCT646AT/648AT				'FCT646CT/648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	5

1727 Tbl 10

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



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