1,048,576 WORD X 16 BIT DYNAMIC RAM

DESCRIPTION

The TC5116160AJ/AFT is the new generation dynamic RAM organized 1,048,576 word by 16 bit. The TC5116160AJ/AFT utilizes Toshiba's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC5116160AJ/AFT to be packaged in a standard 42 pin plastic SOJ, and 50/44 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 16 bit organization
- Fast access time and cycle time
- Single power supply of 5V± 10% with a built-in V_{BB} generator
- Low Power
  523mW MAX. Operating
  (TC5116160AJ/AFT-60)
  440mW MAX. Operating
  (TC5116160AJ/AFT-70)
  385mW MAX. Operating
  (TC5116160AJ/AFT-80)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 4096 refresh cycles/16ms
- Package TC5116160AJ : SOJ42-P-400
  TC5116160AFT : TSOP20-P-400

KEY PARAMETERS

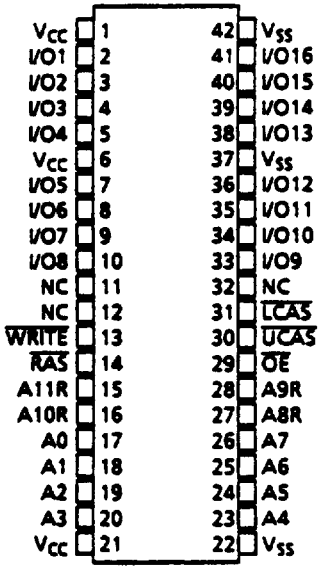
ITEM		TC5116160AJ/AFT		
		-60	-70	-80
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns	20ns
t_{RC}	Cycle Time	110ns	130ns	150ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	50ns

PIN NAME

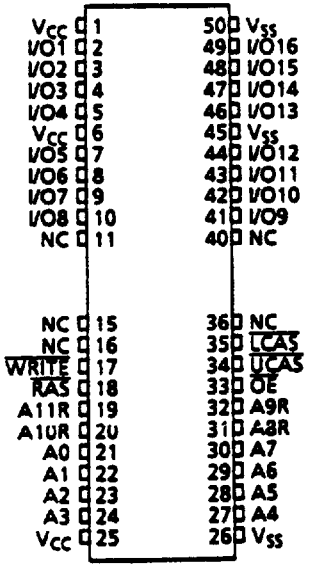
A0~A11	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe /Upper Byte Control
$\overline{LCAS}$	Column Address Strobe /Lower Byte Control
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01~I/016	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

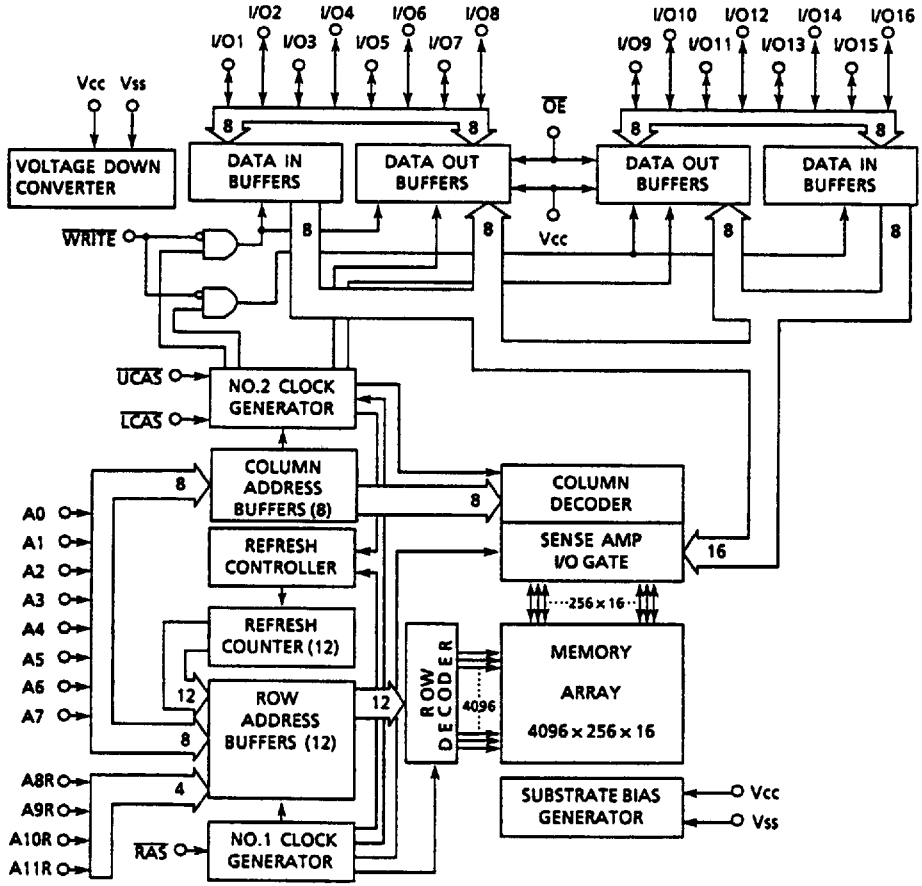
Plastic SOJ



Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	V_{CC}+0.5*	V	2
V_{IL}	Input LowVoltage	-0.5**	-	0.8	V	2

*V_{CC}+2.0V at pulse width ≤20ns (pulse width measured at V_{CC}).
**-2.0V at pulse width ≤20ns (pulse width measured at V_{CC}).

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3,4 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})			2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3, 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	75	mA	3,4 5
		TC511610AJ/AZ/AFTAFTR-70	-	65		
		TC511610AJ/AZ/AFTAFTR-80	-	55		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC}=t_{RC} MIN.)	TC511610AJ/AZ/AFTAFTR-60	-	95	mA	3, 5
		TC511610AJ/AZ/AFTAFTR-70	-	80		
		TC511610AJ/AZ/AFTAFTR-80	-	70		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (OV≤V_{IN}≤0.5V, All Other Pins Not Under Test=OV)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, (OV≤V_{OUT}≤5.5V),		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (V_{CC} = 5V ± 10%, Ta = 0~70°C)(Notes 6,7,8)

SYMBOL	PARAMETER	TC511610AJ/AZ/AFTAFTR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
t_{RMW}	Read-Modify-Write Cycle	135	-	155	-	175	-	ns	
t_{PC}	Fast Page Mode Cycle Time	45	-	45	-	50	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	70	-	70	-	75	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	9,14, 15
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	-	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Presharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	200,000	70	200,000	80	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	45	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5		5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Uup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	0	ns	
t_{CAH}	Column Address Hold Time	10	-	15	-	15	-	ns	
t_{RAL}	Column Address To $\overline{RAS}$ Lead Time	30	-	35	-	40		ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS (CONT)

SYMBOL	PARAMETER	TC511610AJ/AZ/AFTAFTR						UNIT	NOTE
		-60		-70		-80			
		MIN	MAX.	MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	10	-	15	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	12
t_{DH}	Data Hold Time	10	-	15	-	15	-	ns	12
t_{REF}	Refresh Period	-	64	-	64	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	40	-	45	-	45	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	-	95	-	105	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	55	-	60		65	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	60	-	65	-	70	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	5	-	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	15	-	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle	20	-	30	-	30	-	ns	
t_{ROH}	RAS Hold Time referenced to $\overline{OE}$	10	-	10	-	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	15	-	20	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	15	-	15	-	15	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	10
t_{OEH}	Output Hold Time	15	-	15	-	15		ns	
t_{ODS}	Output Disable Set-up Time	0	-	0	-	0		ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

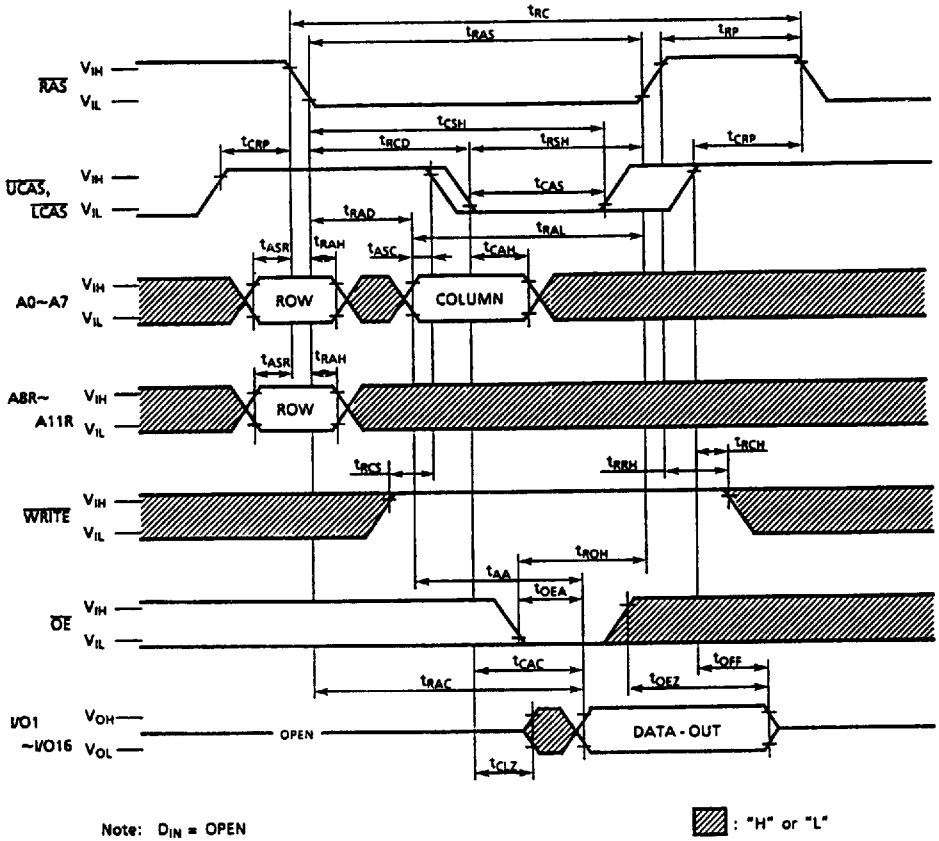
SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0~A11)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Input Capacitance (I/O1~I/O16)	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed one or less while $\overline{RAS}=V_{IL}$. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume t_T=5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data output will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.), $t_{AWD} \geq t_{AWD}$ (min.) and $t_{CPWP} \geq t_{CPWD}$ (min.), (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condifition is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

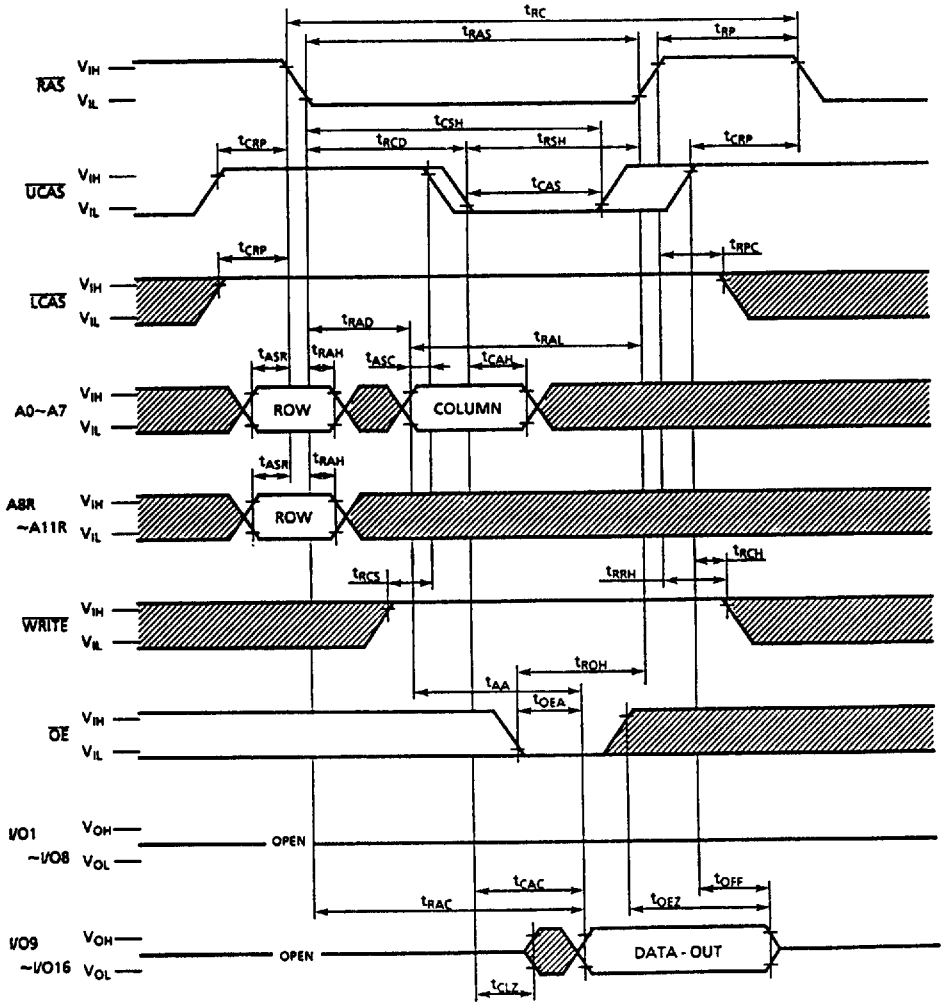
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

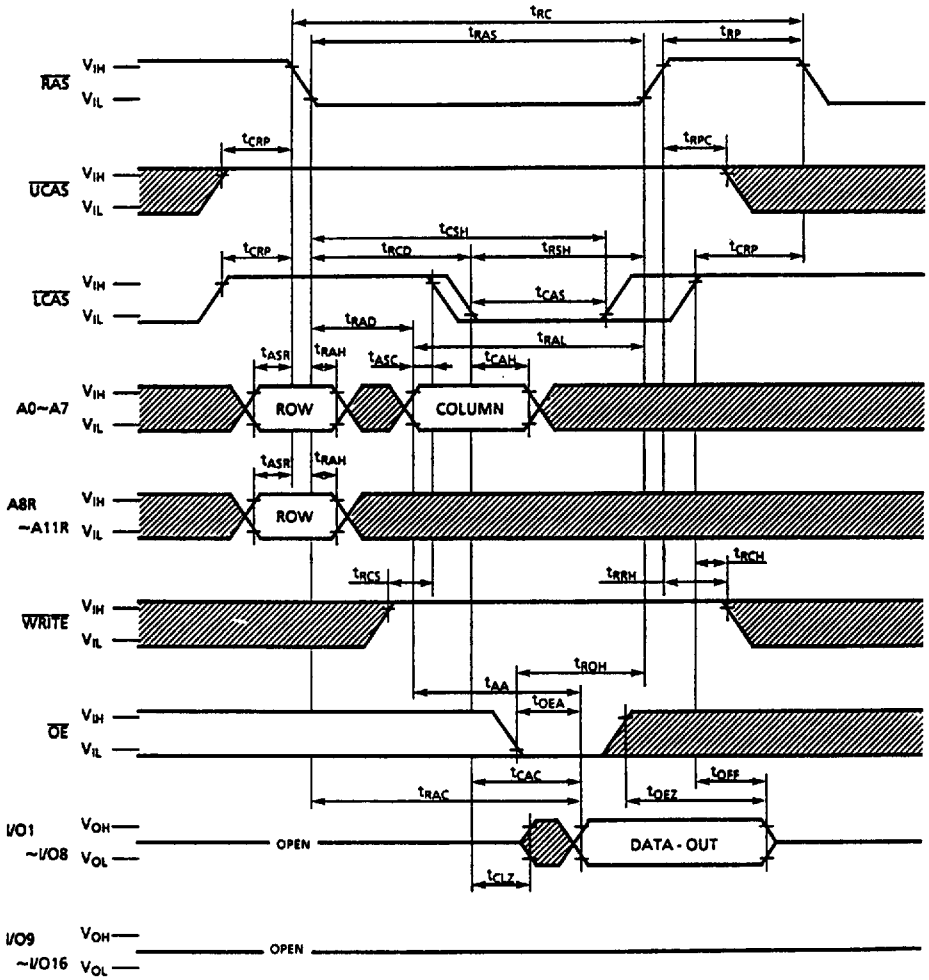
UPPER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{IN} (I/O9~I/O16) = OPEN

▨ : "H" or "L"

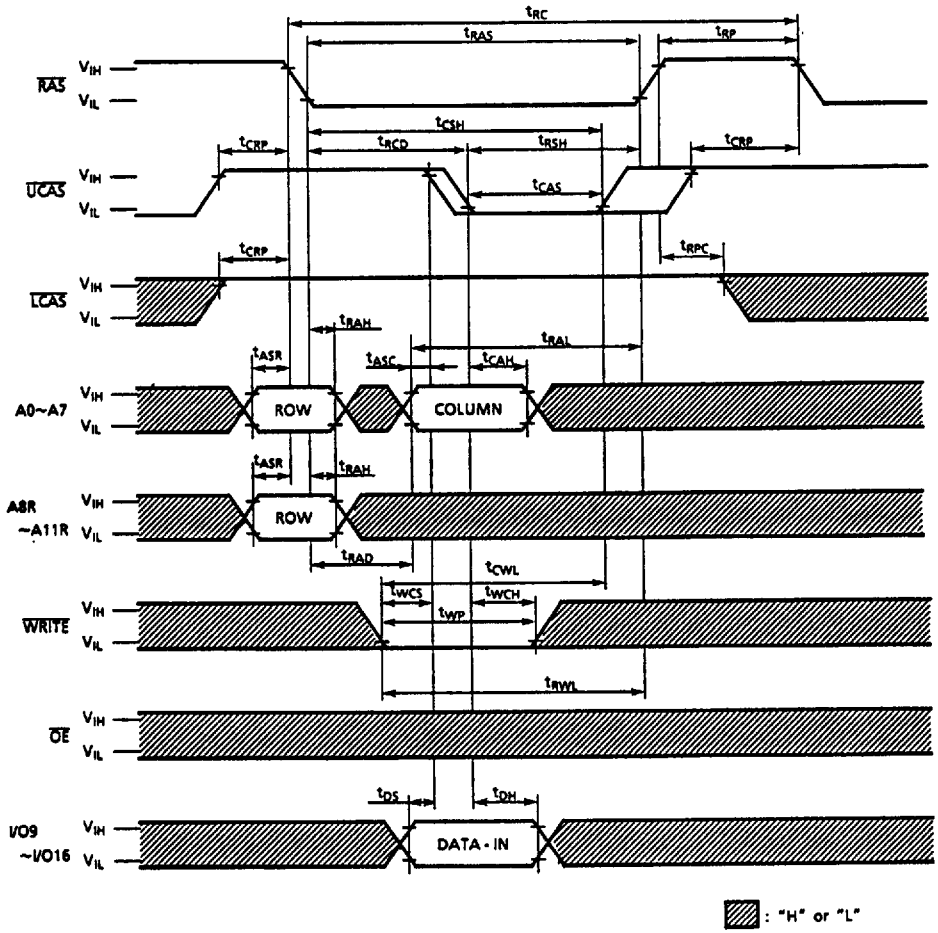
LOWER BYTE READ CYCLE



Note: D_{IN} (I/O1~I/O8) = OPEN
D_{IN} (I/O9~I/O16) = Don't Care

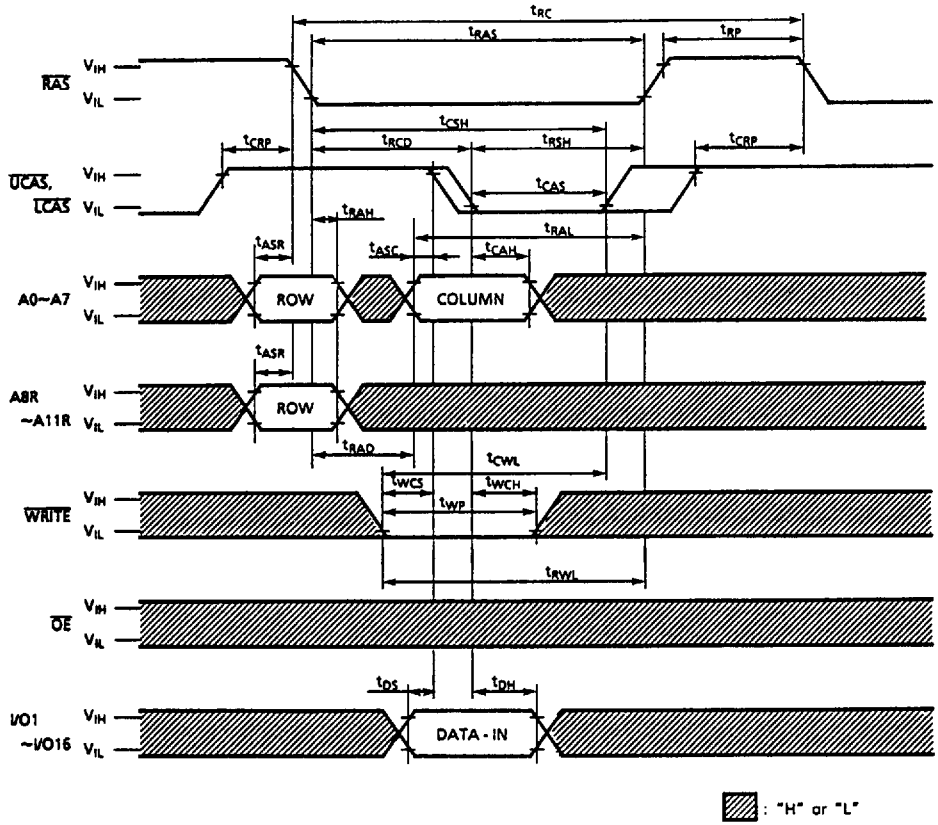
▨ : "H" or "L"

UPPER BYTE WRITE CYCLE (EARLY WRITE)



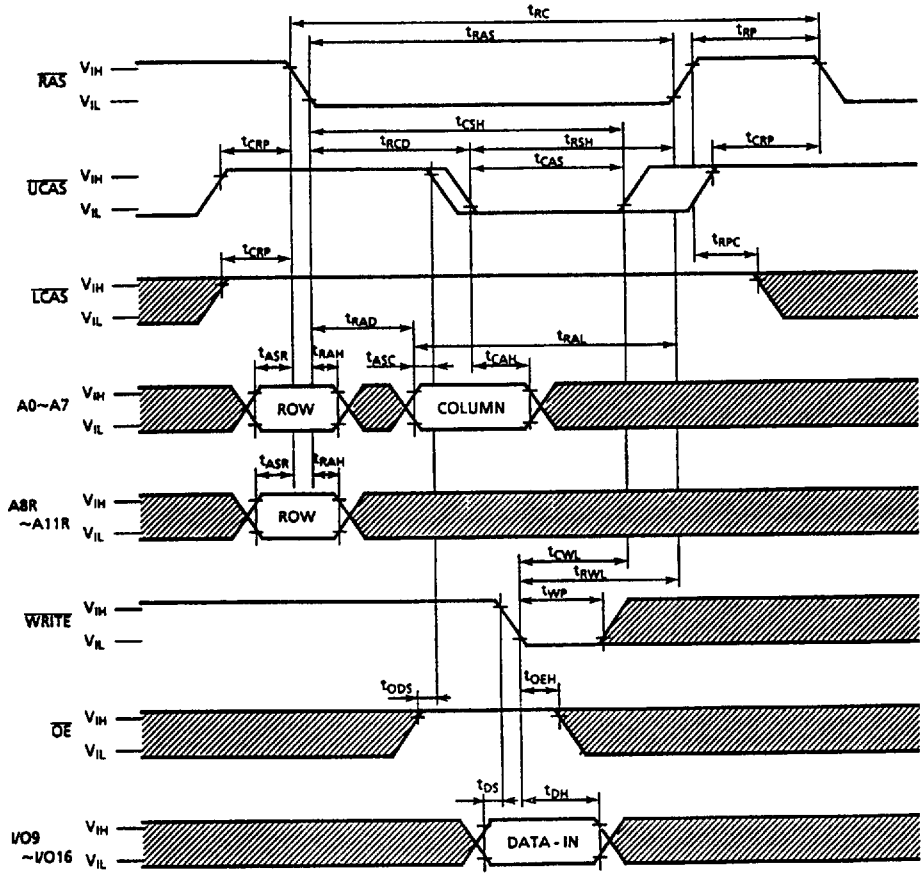
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

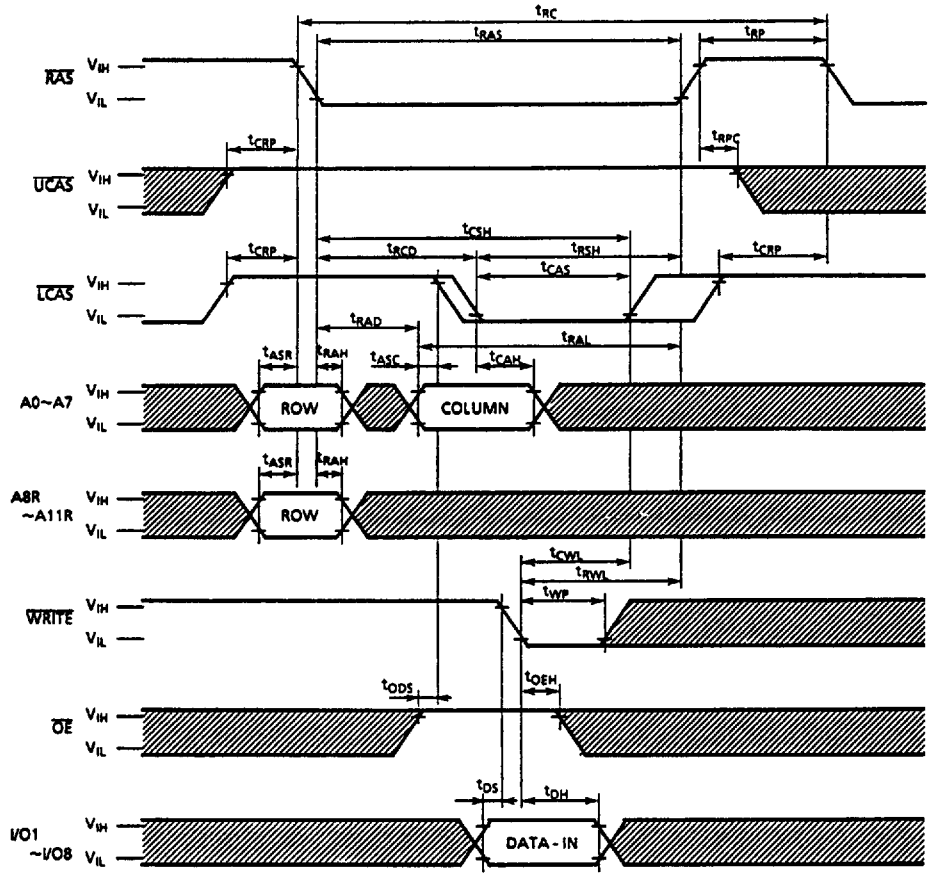
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

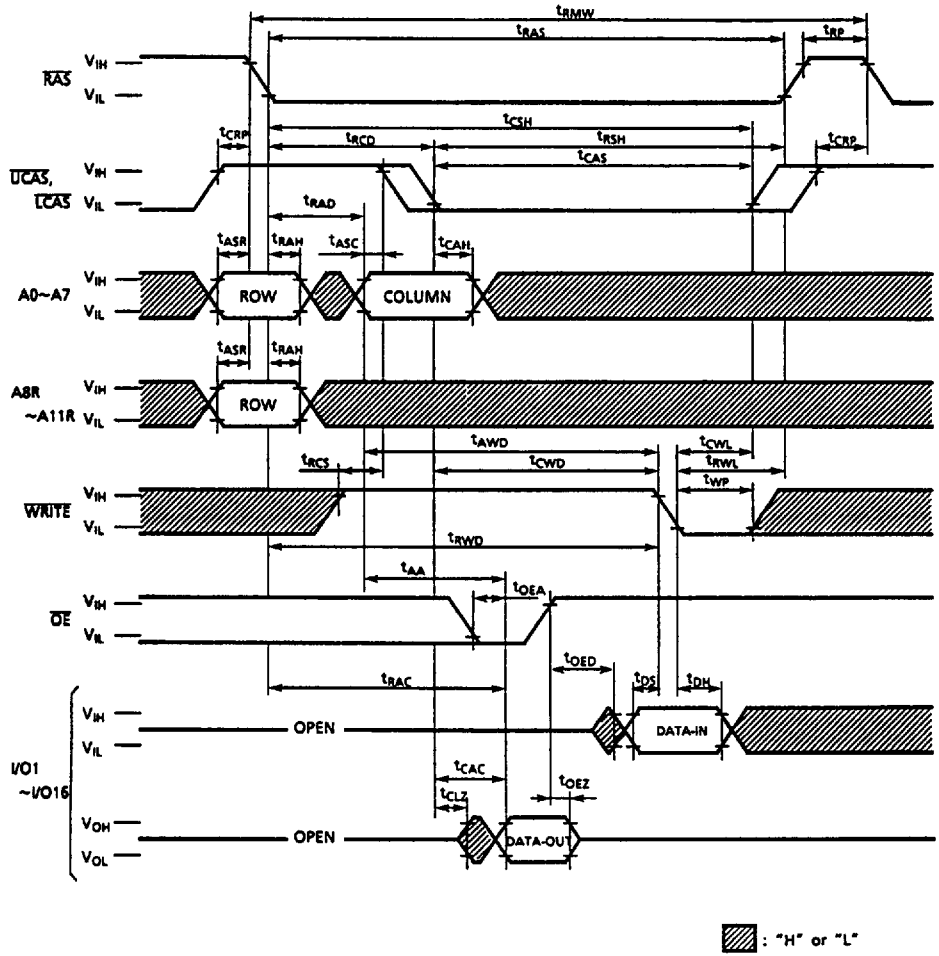
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



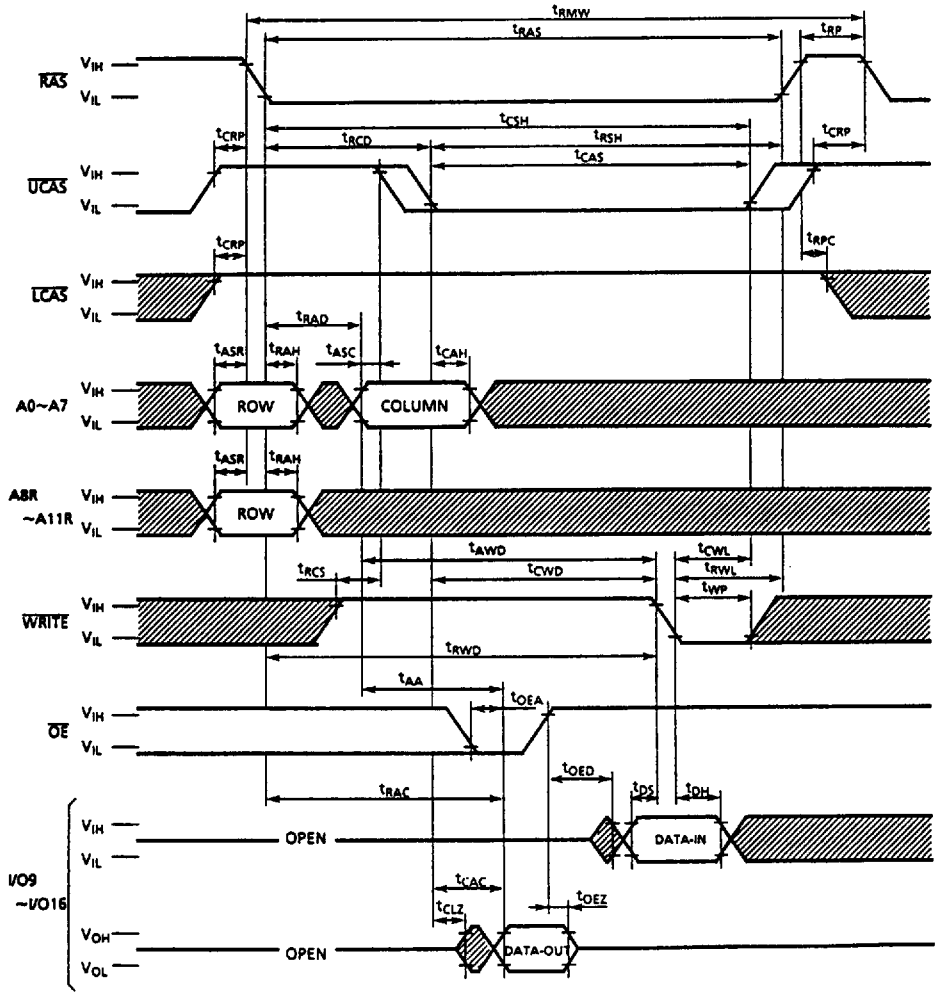
Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

READ-MODIFY-WRITE CYCLE

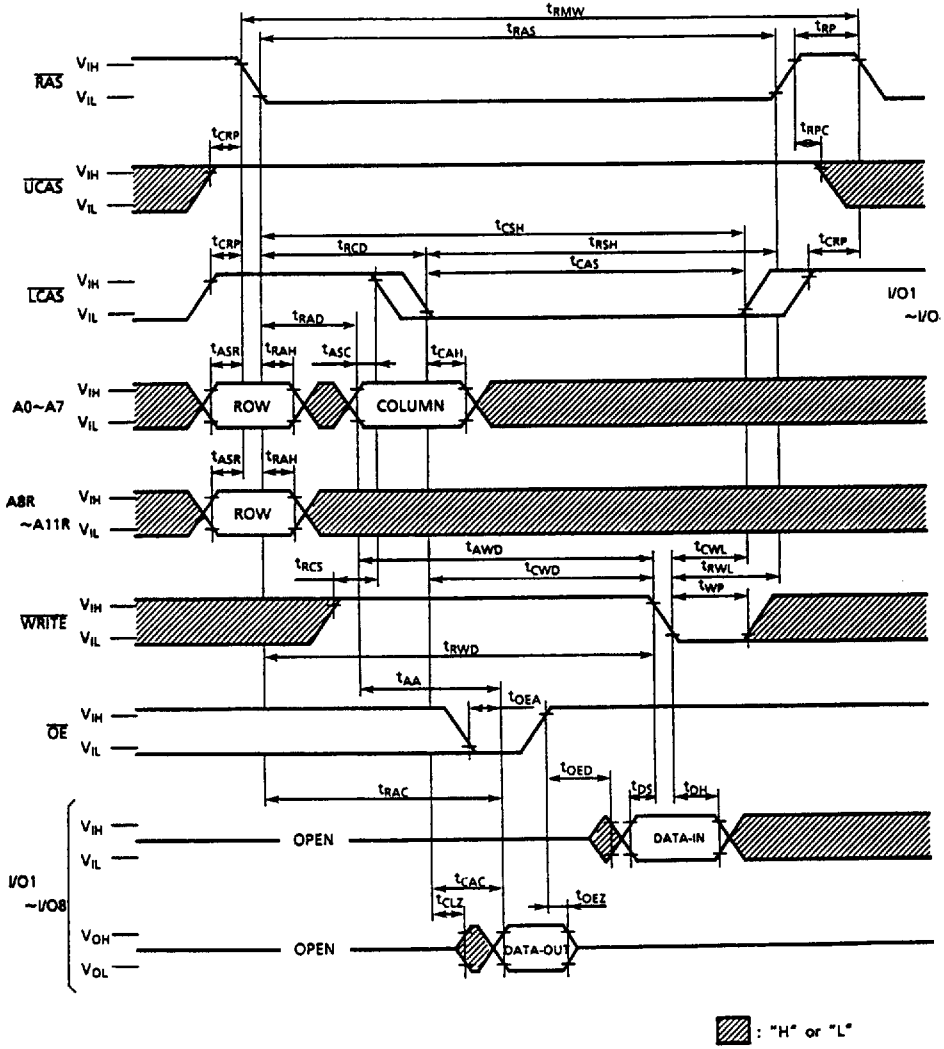


UPPER BYTE READ-MODIFY-WRITE CYCLE



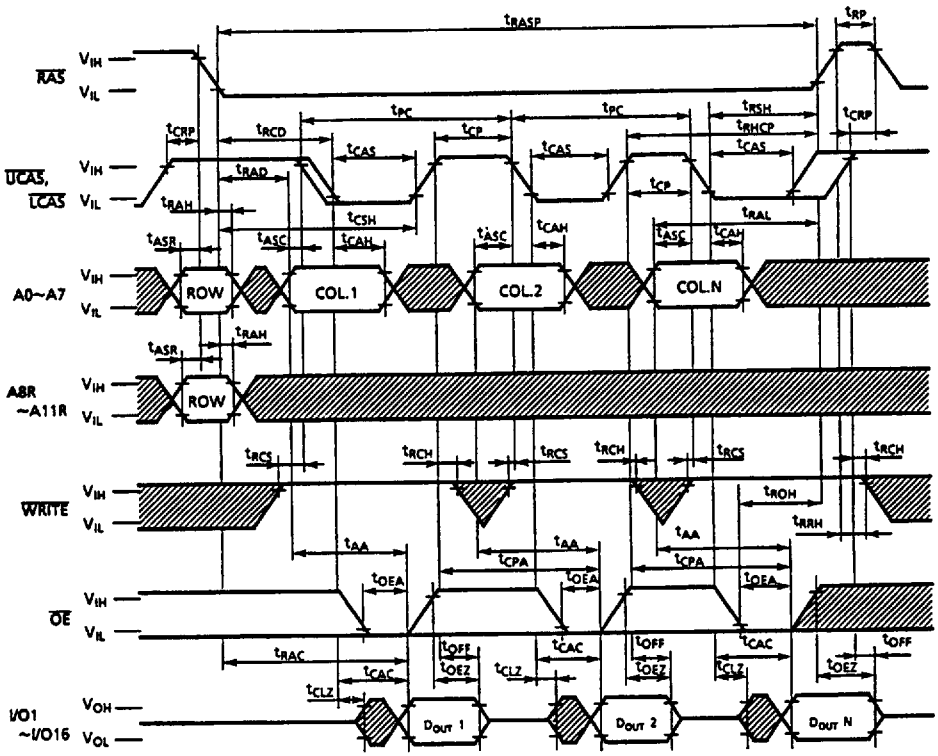
Note: D_{IN} (I/O1~I/O8) = Don't Care
D_{OUT} (I/O1~I/O8) = OPEN

LOWER BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O9~I/O16) = Don't Care
D_{OUT} (I/O9~I/O16) = OPEN

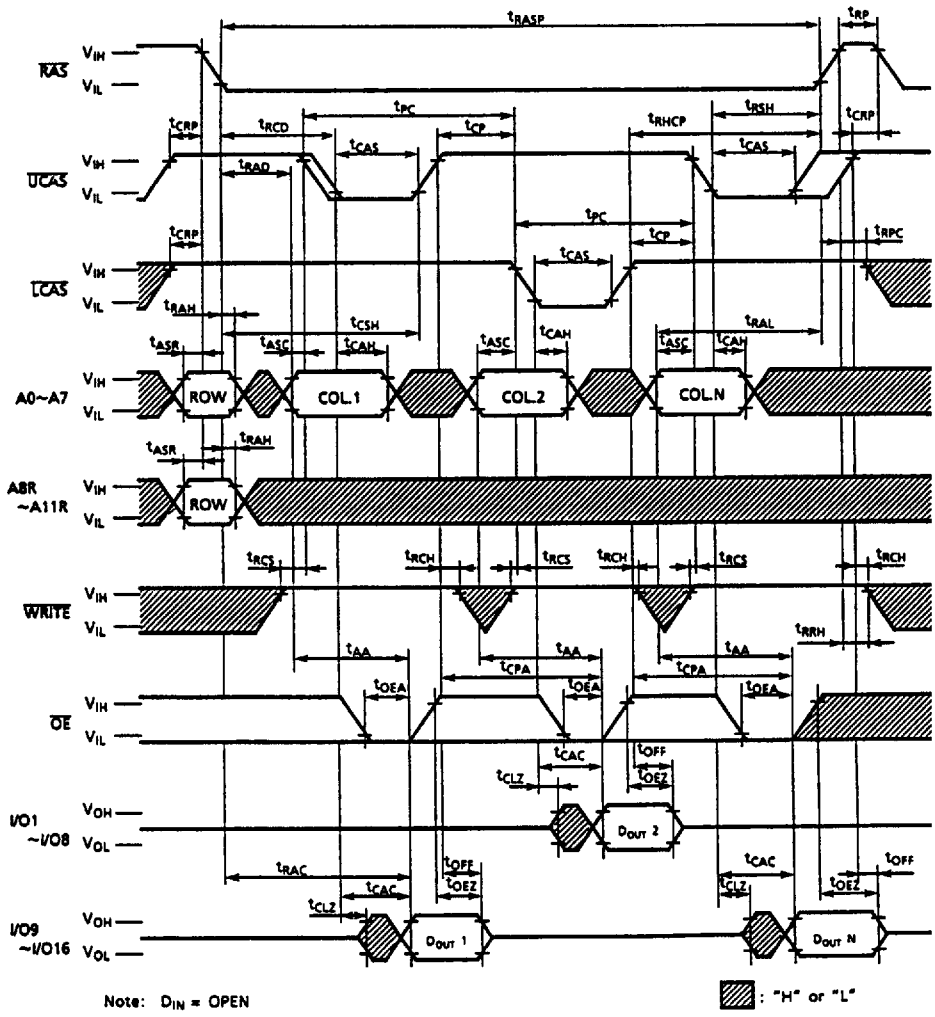
FAST PAGE MODE READ CYCLE



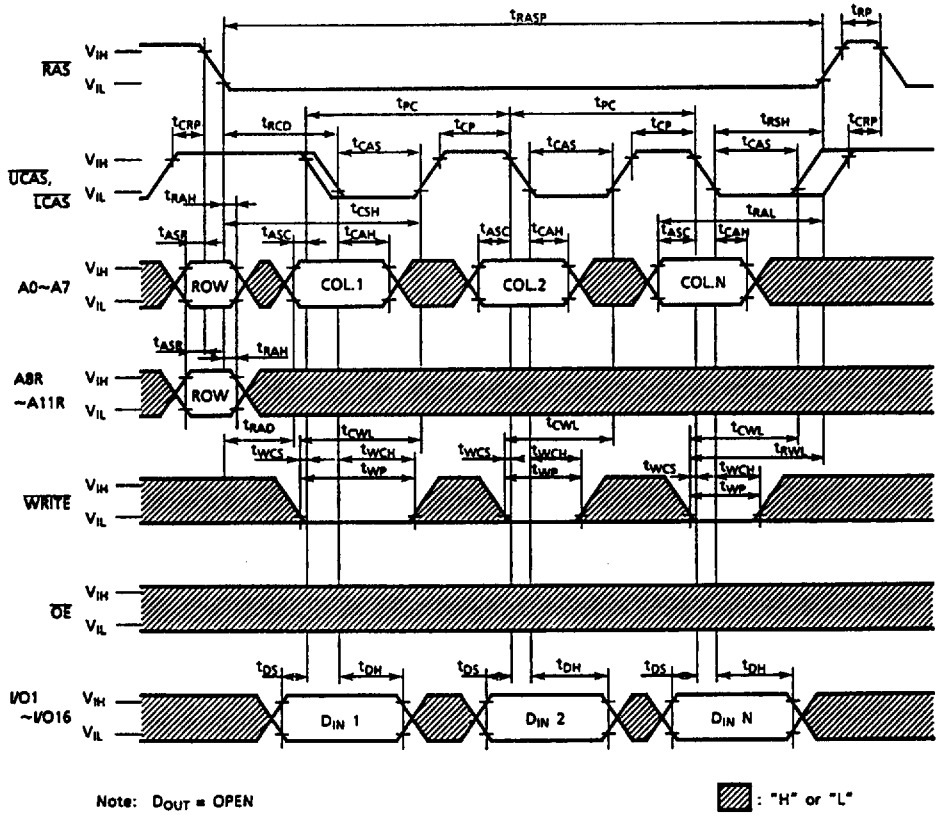
Note: D_{IN} = OPEN

▨ : "H" or "L"

FAST PAGE MODE BYTE READ CYCLE



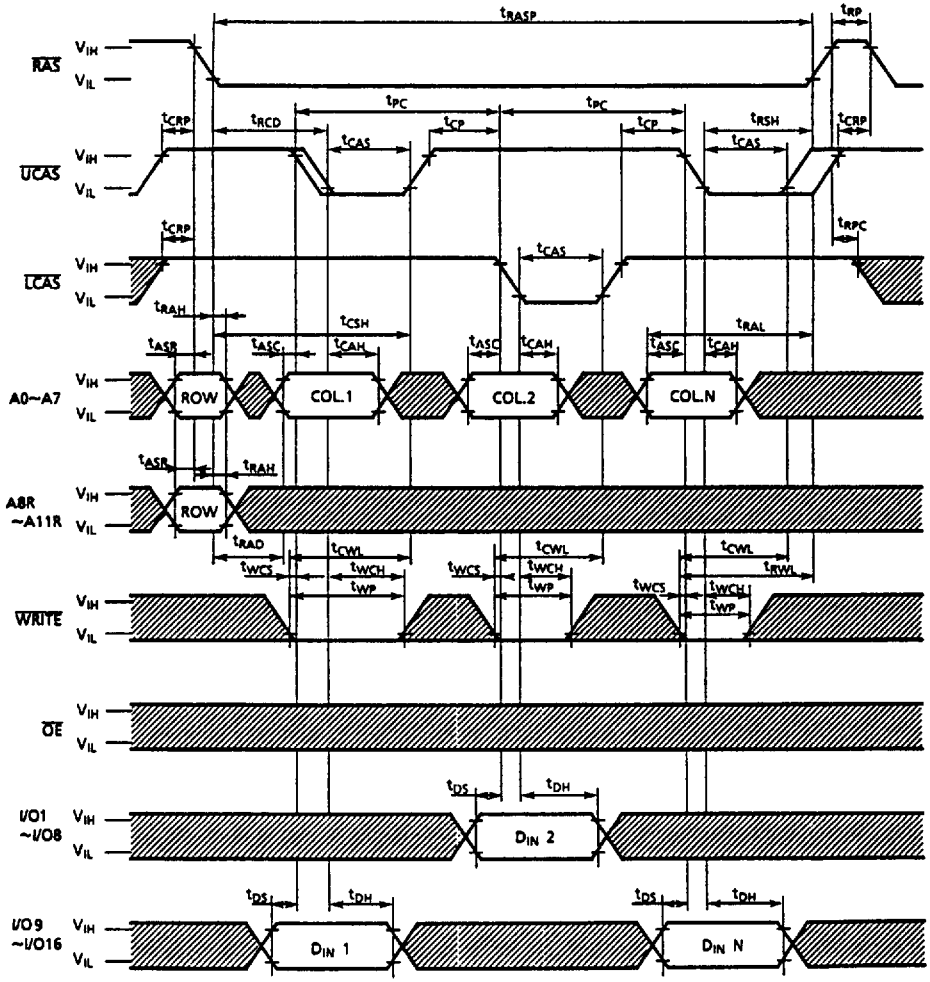
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

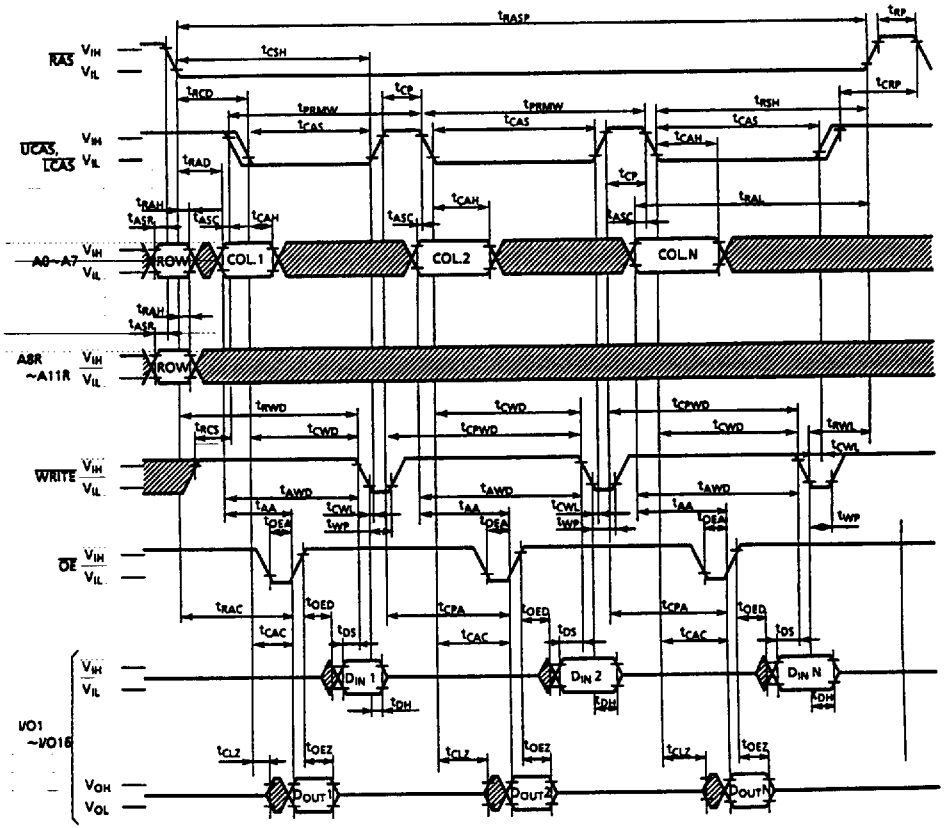
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



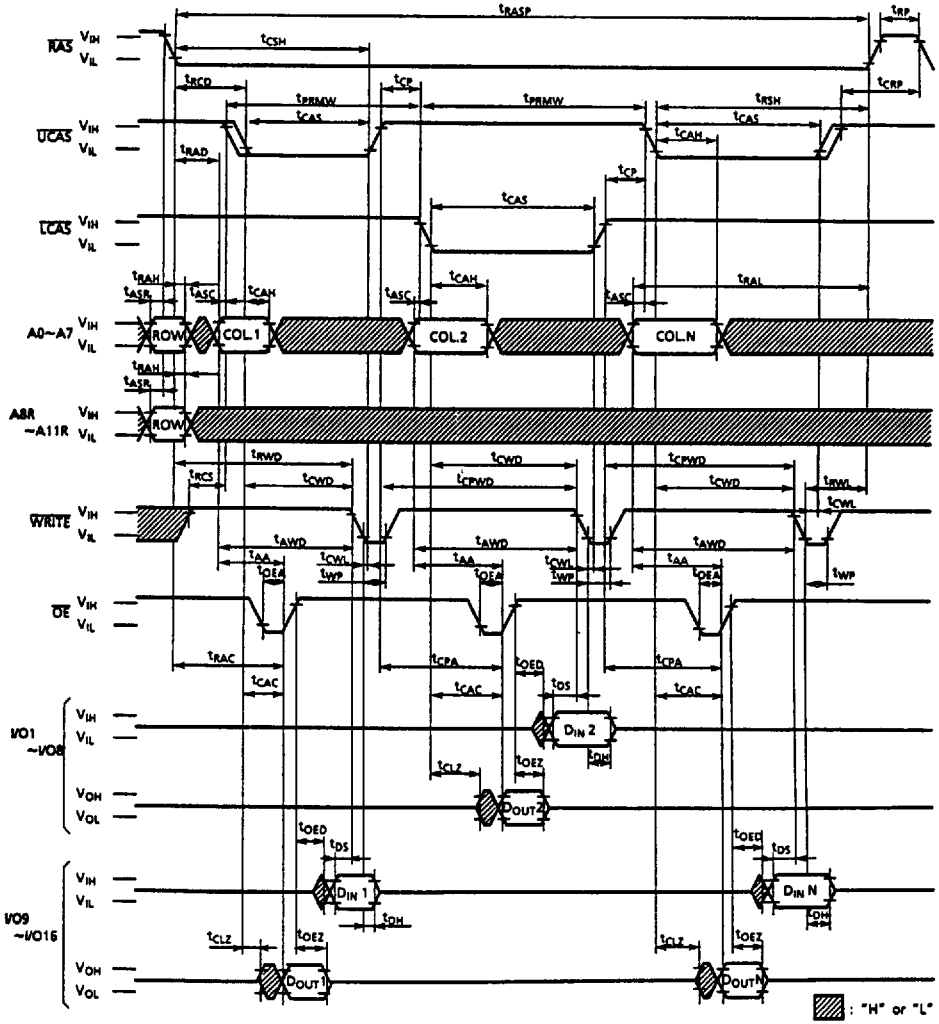
Note: D_{OUT} = OPEN

▨: "H" or "L"

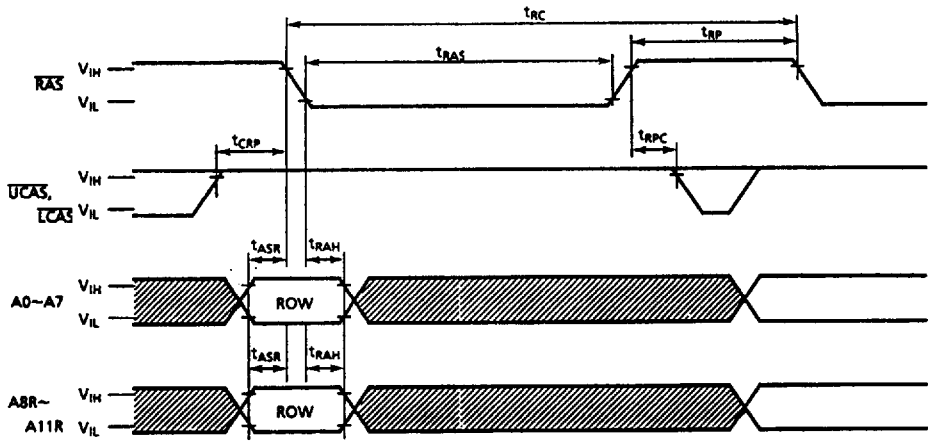
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



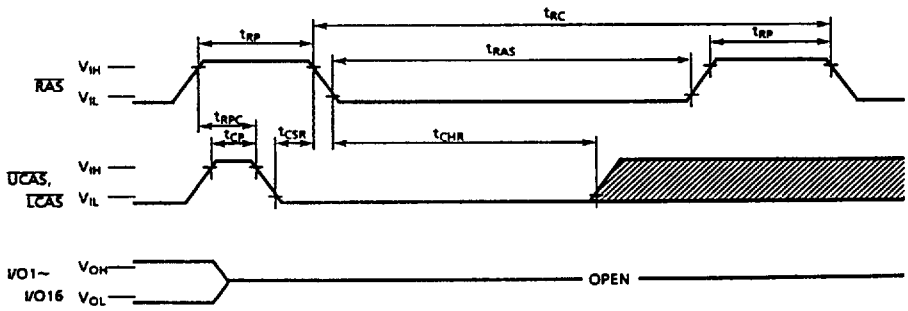
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"
D_{IN} = Don't Care
D_{OUT} = OPEN

▨ : "H" or "L"

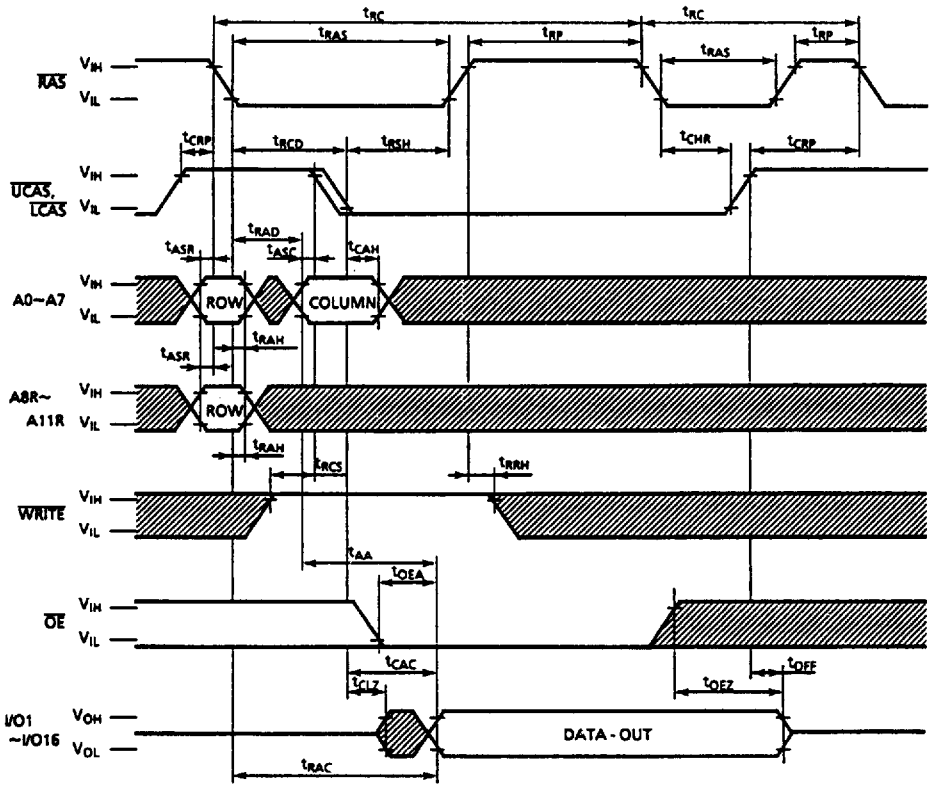
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



▨ : "H" or "L"

Note: $\overline{WRITE}$, $\overline{OE}$, A0~A7, A8R~A11R = "H" or "L"
D_{IN} = Don't Care
$\overline{CAS}$ before $\overline{RAS}$ refresh is performed when either $\overline{UCAS}$ or $\overline{LCAS}$ meets this timing.

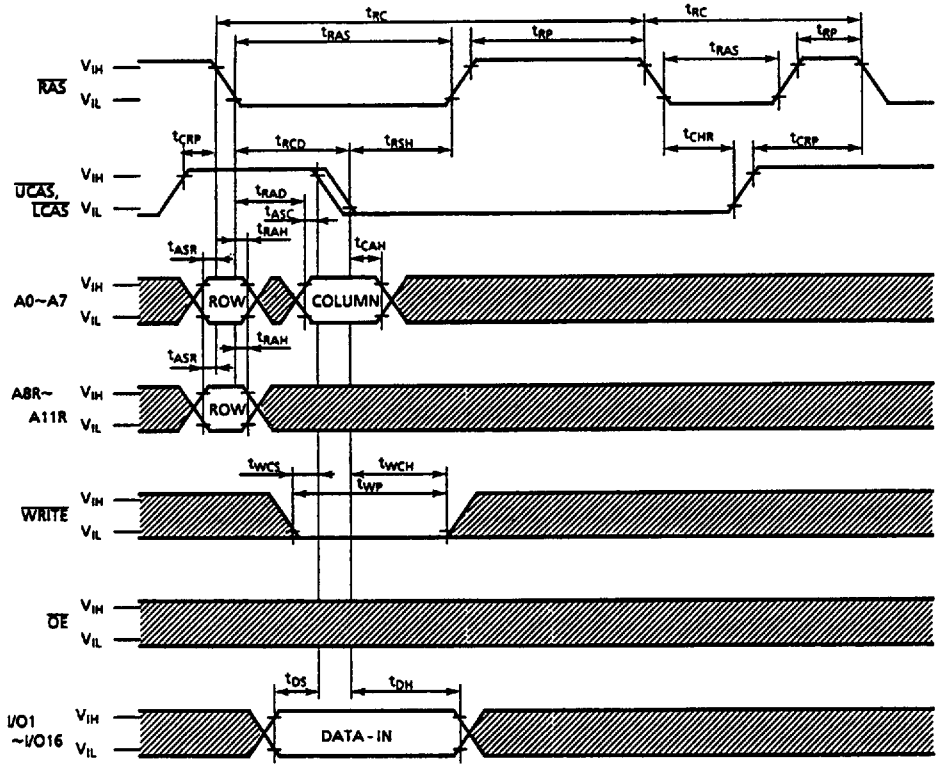
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨: "H" or "L"

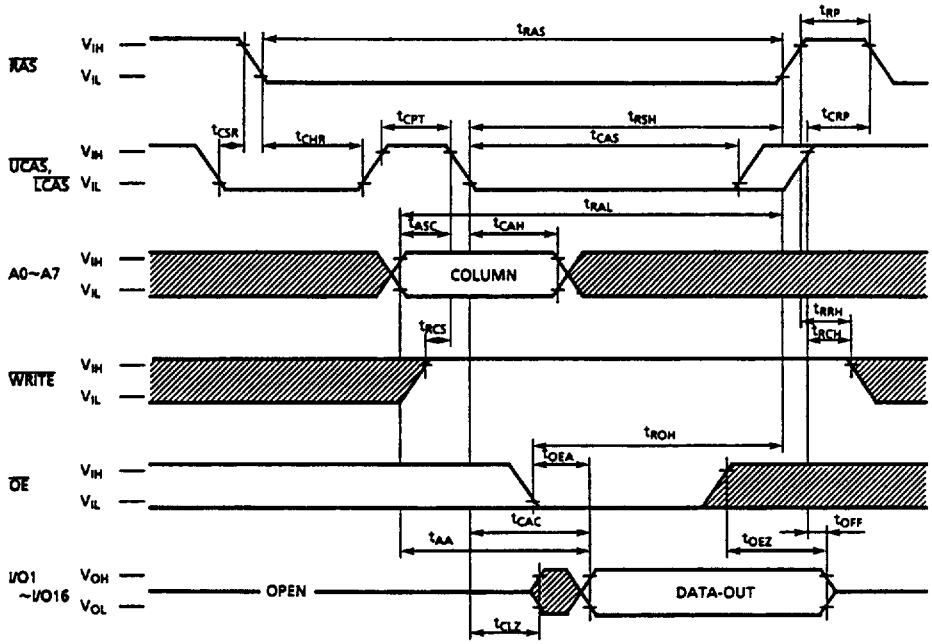
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

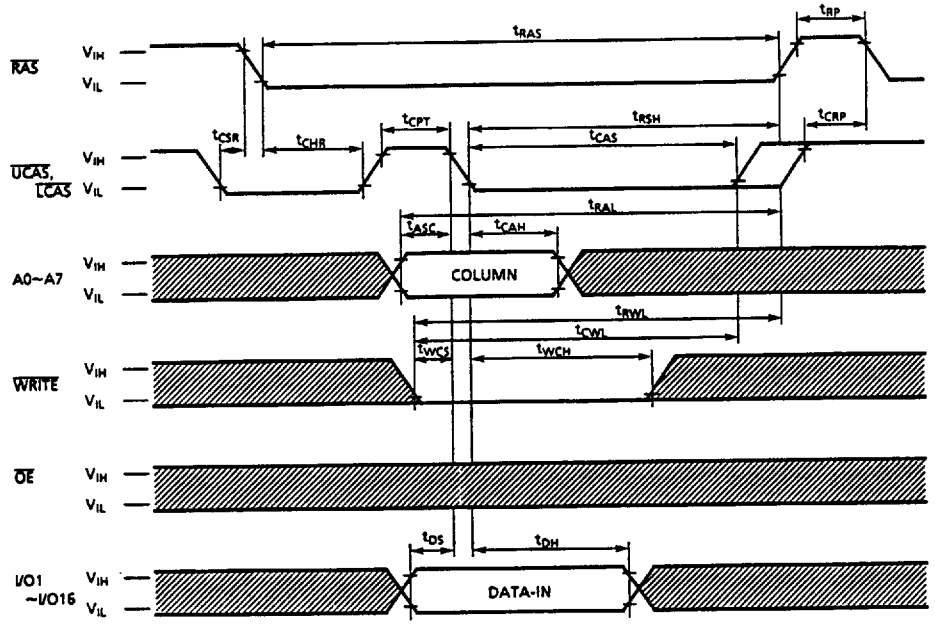
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



Note: A8R~A11R = "H" or "L"
D_{IN} = OPEN

▨ : "H" or "L"

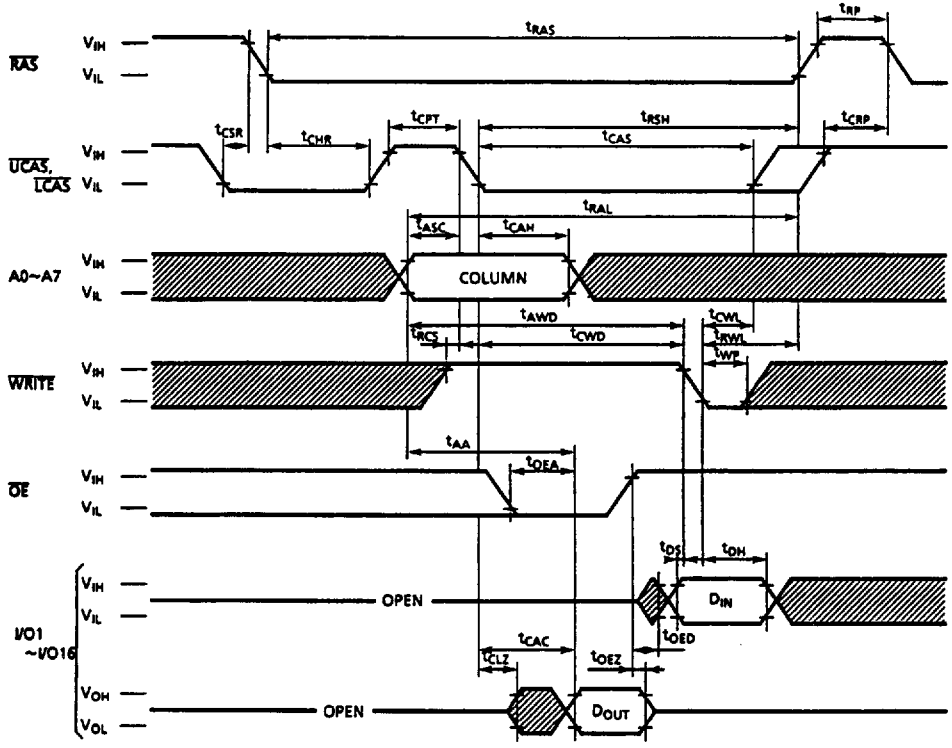
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: A8R~A11R = "H" or "L"
D_{OUT} = OPEN

▨ : "H" or "L"

CAS BEFORE RAS REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



Note: A8R~A11R = "H" or "L"

▨ : "H" or "L"