54F/74F646 • 54F/74F648

Octal Transceiver/Register With 3-State Outputs

PRELIMINARY

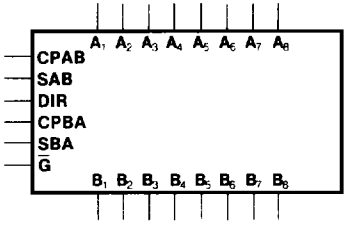
Description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

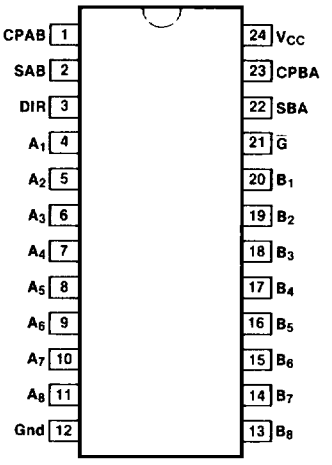
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs**
- **300 mil Slim Package**

Ordering Code: See Section 5

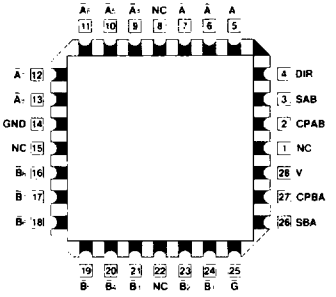
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC

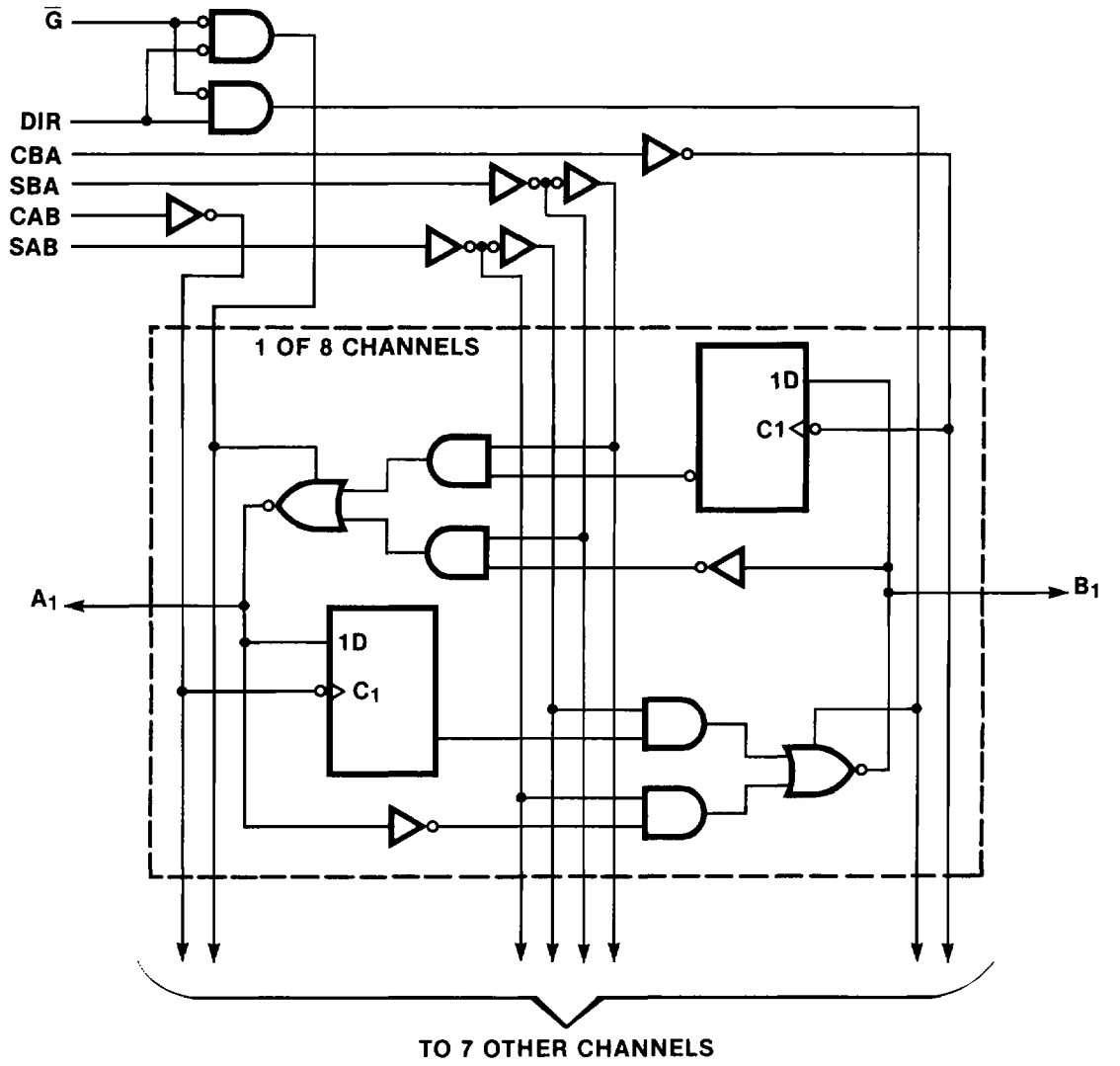


Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_1-A_8	Data Register Inputs	0.5/0.375
	Data Register A Outputs	75/15 (12.5)
B_1-B_8	Data Register B Inputs	0.5/0.375
	Data Register B Outputs	75/40 (30)
CPAB, CPBA	Clock Pulse Inputs	0.5/0.375
SAB, SBA	Transmit/Receive Inputs	0.5/0.375
DIR,$\overline{G}$	Output Enable Inputs	1.0/0.75

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs						Data I/O*		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1-A_8	B_1-B_8	'F646	'F648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current				mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$	T_A, V_{CC} = Mil $C_L = 50\ pF$	T_A, V_{CC} = Com $C_L = 50\ pF$		
		Min Typ Max	Min Max	Min Max		
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	13.0 13.0			ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	11.0 11.0			ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	13.0 13.0			ns	3-1, 3-3 3-4
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	13.0 13.0			ns	3-1, 3-3 3-4
t_{PZH} t_{PZL}	Enable to Bus	12.5 12.5			ns	3-1 3-12 3-13
t_{PZH} t_{PZL}	Direction to Bus DIR to A or B	12.5 12.5				
t_{PHZ} t_{PLZ}	Enable to Bus	10.5 10.5			ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Direction to Bus	10.5 10.5				

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Bus to Clock	3.0 3.0			ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Bus to Clock	1.0 1.0			ns	3-5
$t_w(H)$ $t_w(L)$	Clock Pulse Width HIGH or LOW	4.0 4.0			ns	3-7

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