PREPROGRAMMED STEREO CODEC's CLOCK SYNTHESIZER

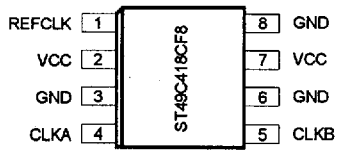
DESCRIPTION

The ST49C418 is a mask programmable monolithic analog CMOS device, designed to replace existing dual crystals/oscillators with single frequency clock input. The ST49C418 provides high speed and low jitter clock outputs for multi-media stereo codecs.

The ST49C418 interfaces to Analog Devices's AD1848 and Crystal Semiconductor's CS4231 stereo codecs. The ST49C418 provides 16.934 and 24.576 MHz clock outputs utilizing the 14.318 MHz clock input.

ST49C418 is designed in a 1.2μ process to achieve upto 50 MHz output frequency.

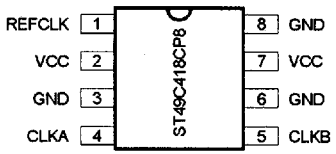
SOIC Package



FEATURES

- Mask programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 pin DIP or SOIC package
- Programmable input/output frequencies
- TTL compatible outputs
- No external components besides decoupling capacitors

Dip Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C418CP8	Plastic-DIP	0 ° C to +70° C
ST49C418CF8	SOIC	0° C to +70° C

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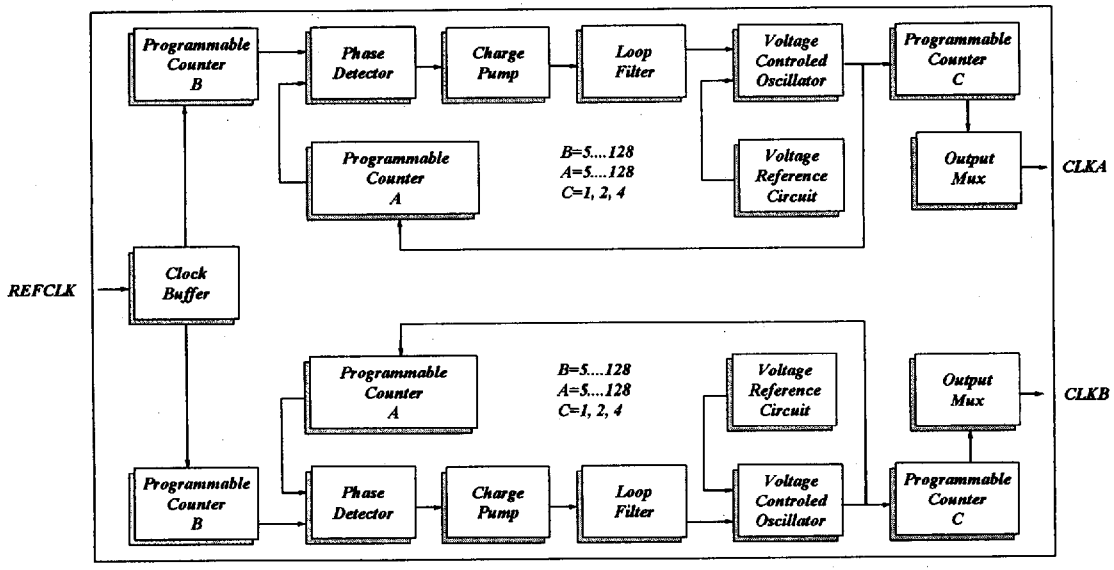
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
REFCLK	1	I	External Reference Clock input. REFCLK is used as internal phase locked loop reference clock.
VCC	2	I	Supply voltage. Single +5 volts.
GND	3	O	Supply ground.
CLKA	4	O	Programmable output clock. Programmed for 16.9344 MHz output.
CLKB	5	O	Programmable output clock. Programmed for 24.576 MHz output.
GND	6	O	Supply ground.
VCC	7	I	Supply voltage. Single +5 volts.
GND	8	O	Supply ground.

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.01 to 0.047μF capacitor to REFCLK, and keep the lead length of the capacitor to REFCLK to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C418 contains an analog phase locked loop circuit with digital closed loop dividers and a final output divider to achieve the desired dividing ratios for the clock output.

The accuracy of the frequencies produced by the ST49C418 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLOCK = (Reference clock) X A/(B X C)

where A=5, 6, 7,.....128
B=5, 6, 7,.....128
C=2

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.5	V	I_{OL} = 25 mA
V_{OH}	Output high level	2.8			V	I_{OH} = 25 mA
I_{IH}	Input high current			1	.µA	
I_{CC}	Operating current		20	35	mA	No load.

AC ELECTRICAL CHARACTERISTICS

T_A=25° C, V_{CC}=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	CLOCK rise time		1.5	3	ns	0.5V - 2.8V, 15pF
T_2	CLOCK fall time		1.5	3	ns	2.8V - 0.5V, 15pF
T_4	Duty cycle	40	48/52	60	%	1.4V switch point
T_5	Duty cycle	45	48/52	55	%	VCC/2 switch point
T_3	Jitter 1 sigma		±0.5	±2	%	
T_3	Jitter absolute		±2	±5	%	
T	Input frequency	5	10	40	MHz	
T_6	CLOCK frequency change		0.01		%	

TIMING DIAGRAM